



勝特力材料 886-3-5753170  
勝特力电子(上海) 86-21-34970699  
勝特力电子(深圳) 86-755-83298787  
Http://www.100y.com.tw

# <1 $\Omega$ CMOS 1.8 V to 5.5 V, Dual SPST Switches

## ADG821/ADG822/ADG823

### FEATURES

- 0.8  $\Omega$  Max On Resistance @125°C
- 0.28  $\Omega$  Max On Resistance Flatness @125°C
- 1.8 V to 5.5 V Single Supply
- 200 mA Current Carrying Capability
- Automotive Temperature Range: -40°C to +125°C
- Rail-to-Rail Operation
- 8-Lead MSOP Package
- 33 ns Switching Times
- Typical Power Consumption (<0.01  $\mu$ W)
- TTL/CMOS Compatible Inputs
- Pin Compatible with ADG721/722/723

### APPLICATIONS

- Power Routing
- Battery-Powered Systems
- Communication Systems
- Data Acquisition Systems
- Audio and Video Signal Routing
- Cellular Phones
- Modems
- PCMCIA Cards
- Hard Drives
- Relay Replacement

### GENERAL DESCRIPTION

The ADG821, ADG822, and ADG823 are monolithic CMOS SPST (single pole, single throw) switches. These switches are designed on an advanced submicron process that provides low power dissipation, yet gives high switching speed, low on resistance, and low leakage currents.

The ADG821, ADG822, and ADG823 are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments.

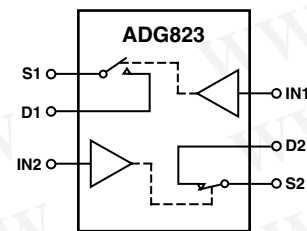
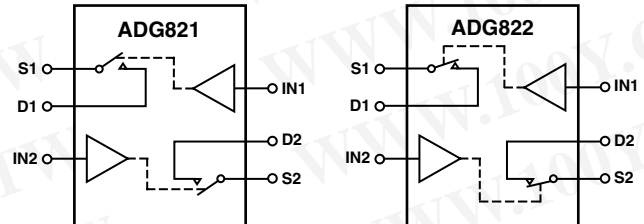
Each switch of the ADG821/ADG822/ADG823 conducts equally well in both directions when on. The ADG821, ADG822, and ADG823 contain two independent SPST switches. The ADG821 and ADG822 differ only in that both switches are normally open and normally closed, respectively. In the ADG823, Switch 1 is normally open and Switch 2 is normally closed. The ADG823 exhibits break-before-make switching action.

The ADG821, ADG822, and ADG823 are available in an 8-lead MSOP package.

### REV. 0

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### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "0" INPUT

### PRODUCT HIGHLIGHTS

1. Very Low On Resistance (0.5  $\Omega$  typ)
2. On Resistance Flatness ( $R_{FLAT(ON)}$ ) (0.15  $\Omega$  typ)
3. Automotive Temperature Range -40°C to +125°C
4. 200 mA Current Carrying Capability
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. 8-Lead MSOP Package

# ADG821/ADG822/ADG823—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ . All specifications $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	25°C	-40°C to +85°C	-40°C to +125°C <sup>2</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.5			$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
	0.6	0.7	0.8	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.16			$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = 100\text{ mA}$
	0.2	0.25	0.28	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.15			$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = 100\text{ mA}$
	0.23	0.26	0.3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 25$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 25$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ , or $V_S = V_D = 4.5\text{ V}$ ; Test Circuit 3
	$\pm 0.25$	$\pm 3$	$\pm 25$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>					
$t_{ON}$	33			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ ; Test Circuit 4
	45	48	52	ns max	
$t_{OFF}$	11			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ ; Test Circuit 4
	16	19	21	ns max	
Break-Before-Make Time Delay, $t_{BBM}$ (ADG823 Only)	32			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3\text{ V}$ ; Test Circuit 5
			1	ns min	
Charge Injection	15			pC typ	$V_S = 2.5\text{ V}$ ; $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 6
Off Isolation	-52			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Channel-to-Channel Crosstalk	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
Bandwidth -3 dB	24			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (OFF)	85			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	98			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	230			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	2.0	$\mu\text{A}$ max	

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## NOTES

<sup>1</sup>Temperature range: Automotive range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

<sup>2</sup>On resistance parameters tested with  $I_S = 10\text{ mA}$ .

<sup>3</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG821/ADG822/ADG823

( $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ , unless otherwise noted.)<sup>1</sup>

Parameter	25°C	-40°C to +85°C	-40°C to +125°C <sup>2</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.7			$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Test Circuit 1
	1.4	1.5	1.6	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.16			$\Omega$ typ	
	0.2	0.25	0.28	$\Omega$ max	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.3		0.33	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 15$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = 3.3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3.3\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 3$	$\pm 25$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ , or $3.3\text{ V}$ ; Test Circuit 3
	$\pm 0.25$	$\pm 3$	$\pm 25$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>					
$t_{ON}$	48			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 1.5\text{ V}$ ; Test Circuit 4
	67	74	78	ns max	
$t_{OFF}$	12			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 1.5\text{ V}$ ; Test Circuit 4
	18	20	23	ns max	
Break-Before-Make Time Delay, $t_{BBM}$ (ADG823 Only)	40			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 1.5\text{ V}$ ; Test Circuit 5
			1	ns min	
Charge Injection	$\pm 2$			pC typ	$V_S = 1.5\text{ V}$ ; $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 6
Off Isolation	-52			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Channel-to-Channel Crosstalk	-82			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 9
Bandwidth -3 dB	24			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (OFF)	85			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	98			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	230			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$ Digital Inputs = 0 V or 3.6 V
		1.0	2.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range: Automotive range:  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ .

<sup>2</sup>On resistance parameters tested with  $I_S = 10\text{ mA}$ .

<sup>3</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG821/ADG822/ADG823

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>DD</sub> to GND	-0.3 V to +7 V
Analog Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Digital Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	400 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	200 mA
Operating Temperature Range	
Automotive	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T <sub>J</sub> max)	150°C
Package Power Dissipation	(T <sub>J</sub> max - T <sub>A</sub> )/θ <sub>JA</sub>
8-Lead MSOP Package	
θ <sub>JA</sub> Thermal Impedance	206°C/W

θ <sub>JC</sub> Thermal Impedance	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

## NOTES

<sup>1</sup> Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup> Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

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Table I. Truth Table for the ADG821/ADG822

ADG821 IN <sub>x</sub>	ADG822 IN <sub>x</sub>	Switch x Condition
0	1	OFF
1	0	ON

Table II. Truth Table for the ADG823

IN1	IN2	Switch S1	Switch S2
0	0	OFF	ON
0	1	OFF	OFF
1	0	ON	ON
1	1	ON	OFF

## ORDERING GUIDE

Model Option	Temperature Range	Brand*	Package Description	Package
ADG821BRM	-40°C to +125°C	SQB	MSOP (microSmall Outline IC)	RM-8
ADG822BRM	-40°C to +125°C	SRB	MSOP (microSmall Outline IC)	RM-8
ADG823BRM	-40°C to +125°C	SSB	MSOP (microSmall Outline IC)	RM-8

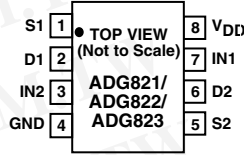
\*Branding on MSOP packages is limited to three characters due to space constraints.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG821/ADG822/ADG823 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION 8-Lead MSOP (RM-8)

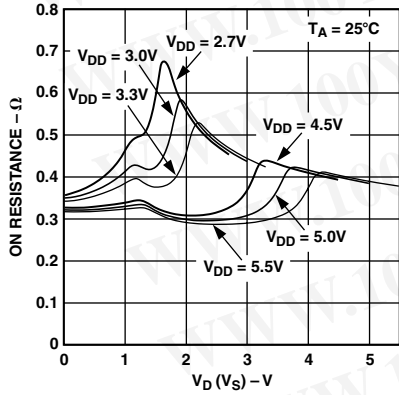


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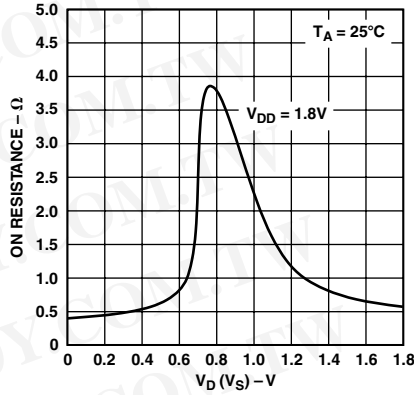
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential
GND	Ground (0 V) Reference
$I_{DD}$	Positive Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
$R_{ON}$	Ohmic Resistance between D and S
$\Delta R_{ON}$	On Resistance Match between any Two Channels (i.e., $R_{ON\ max} - R_{ON\ min}$ )
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the Switch OFF
$I_D$ (OFF)	Drain Leakage Current with the Switch OFF
$I_D, I_S$ (ON)	Channel Leakage Current with the Switch ON
$V_D$ ( $V_S$ )	Analog Voltage on Terminals D and S
$V_{INL}$	Maximum Input Voltage for Logic "0"
$V_{INH}$	Minimum Input Voltage for Logic "1"
$I_{INL}$ ( $I_{INH}$ )	Input Current of the Digital Input
$C_S$ (OFF)	OFF Switch Source Capacitance
$C_D$ (OFF)	OFF Switch Drain Capacitance
$C_D, C_S$ (ON)	ON Switch Capacitance
$t_{ON}$	Delay between Applying the Digital Control Input and the Output Switching ON
$t_{OFF}$	Delay between Applying the Digital Control Input and the Output Switching OFF
$t_{BBM}$	OFF time or ON time measured between the 90% points of both switches, when switching from one address state to another.
Charge Injection	It is a measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	It is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A Measure of Unwanted Signal Coupling through an OFF Switch
Bandwidth	The Frequency at which the Output Is Attenuated by -3 dBs
On Response	The Frequency Response of the ON Switch
Insertion Loss	The Loss due to the On Resistance of the Switch

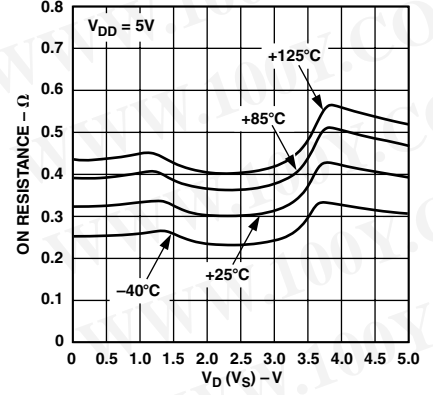
# ADG821/ADG822/ADG823—Typical Performance Characteristics



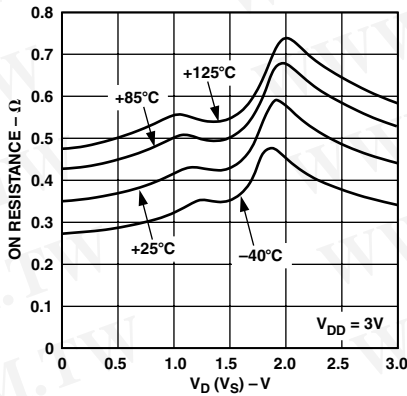
TPC 1. On Resistance vs.  $V_D$  ( $V_S$ )



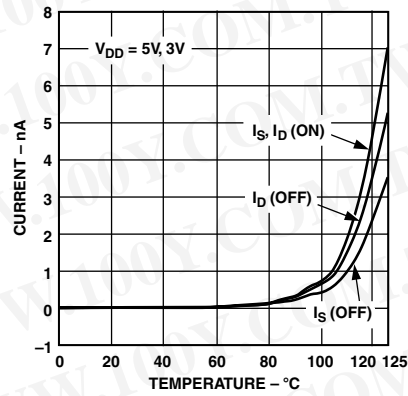
TPC 2. On Resistance vs.  $V_D$  ( $V_S$ )



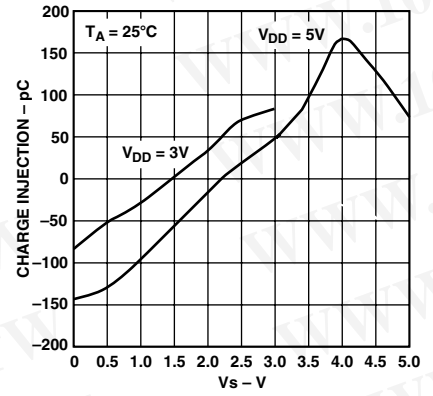
TPC 3. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures



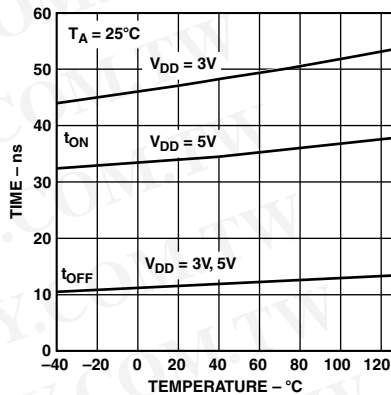
TPC 4. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures



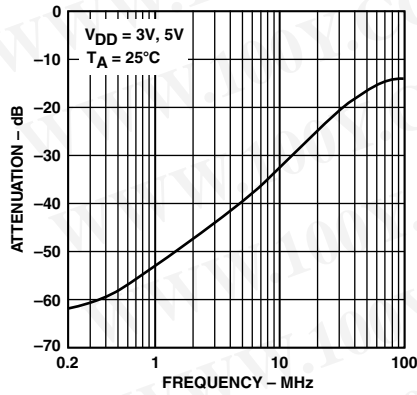
TPC 5. Leakage Currents vs. Temperature



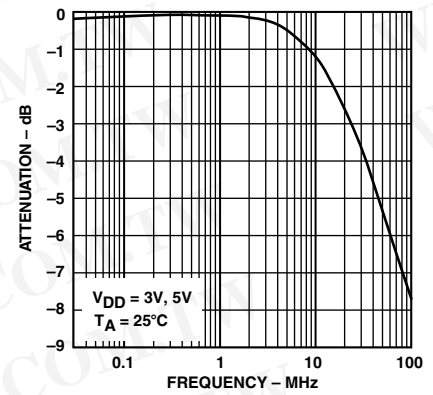
TPC 6. Charge Injection vs. Source Voltage



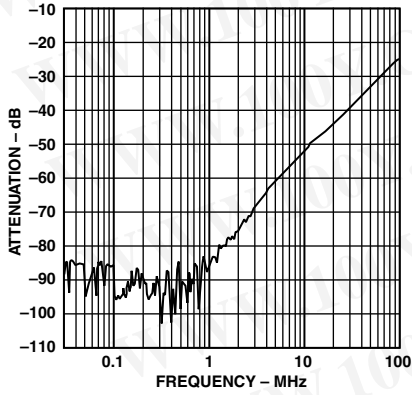
TPC 7.  $t_{ON}/t_{OFF}$  vs. Temperature



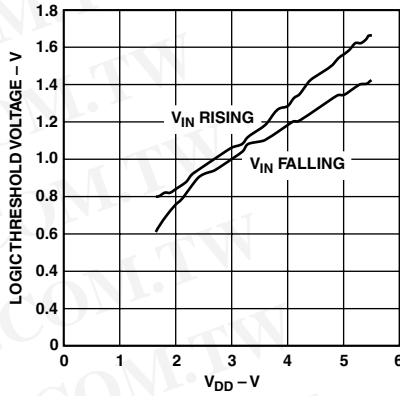
TPC 8. Off Isolation vs. Frequency



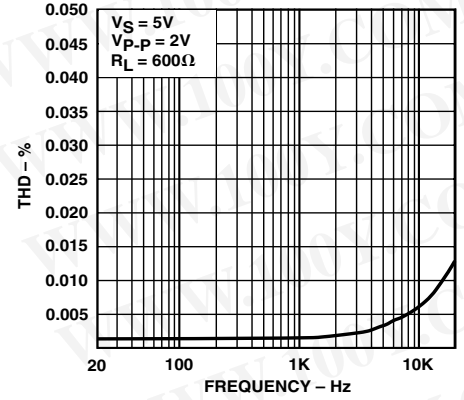
TPC 9. On Response vs. Frequency



TPC 10. Crosstalk vs. Frequency



TPC 11. Logic Threshold Voltage vs. Supply Voltage



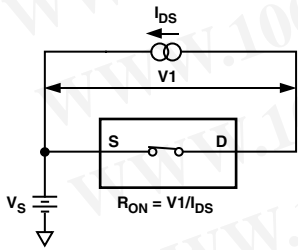
TPC 12. THD

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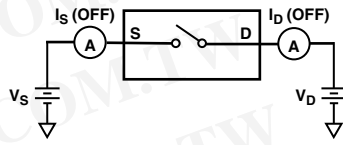
# ADG821/ADG822/ADG823

## Test Circuits

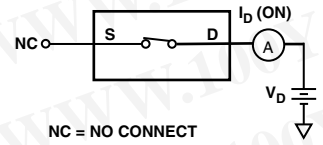
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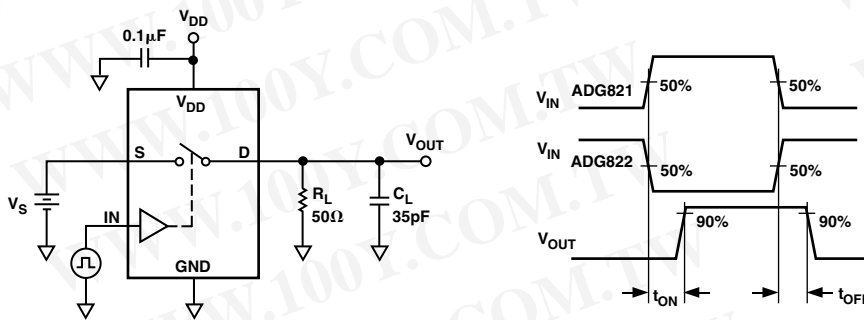
Test Circuit 1. On Resistance



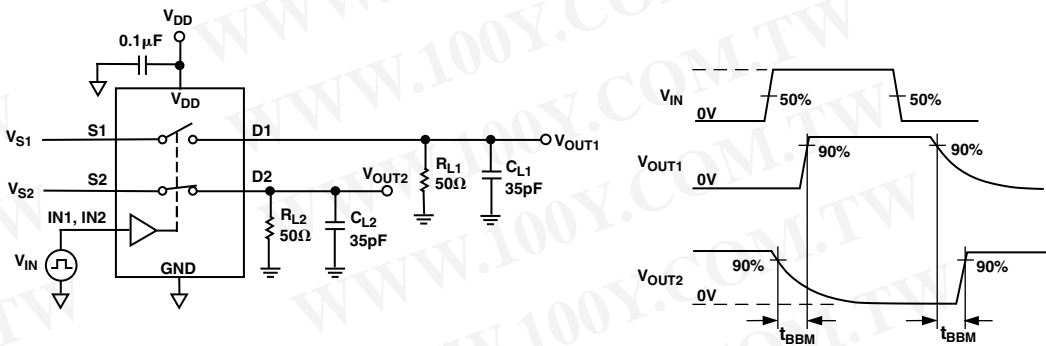
Test Circuit 2. Off Leakage



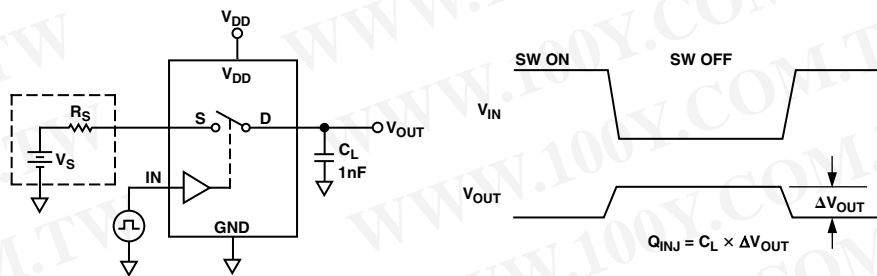
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

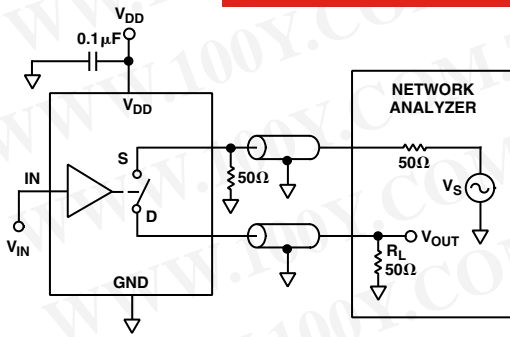


Test Circuit 5. Break-Before-Make Time Delay,  $t_{BBM}$  (ADG823 only)



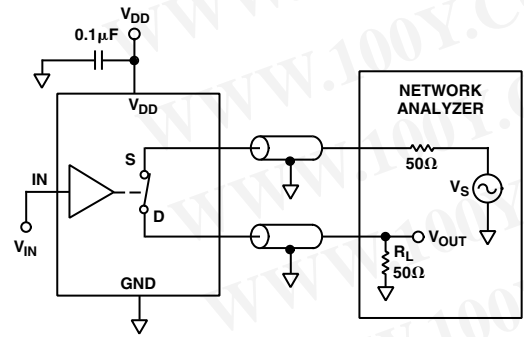
Test Circuit 6. Charge Injection





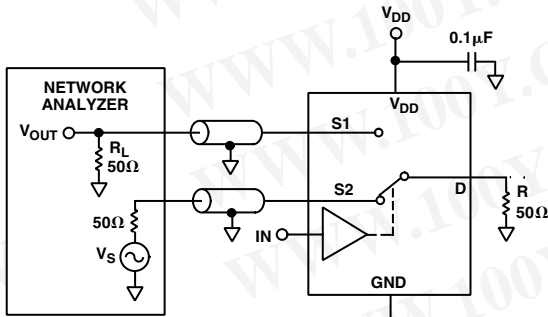
$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_{\text{S}}}$$

Test Circuit 7. Off Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Test Circuit 8. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_{\text{S}}}$$

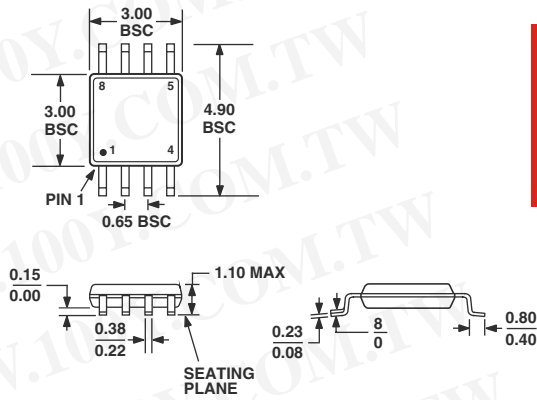
Test Circuit 9. Channel-to-Channel Crosstalk

# ADG821/ADG822/ADG823

## OUTLINE DIMENSIONS

### 8-Lead MSOP Package [MSOP] (RM-8)

Dimensions shown in millimeters



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C02851-0-8(02/0)

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