

勝特力電材超市-龍山店 886-3-5773766
 勝特力電材超市-光復店 886-3-5729570
 胜特力电子(上海) 86-21-34970699
 胜特力电子(深圳) 86-755-83298787
<http://www.100y.com.tw>

MIC2550A

Micrel, Inc.



MIC2550A

Universal Serial Bus Transceiver

General Description

The MIC2550A is a single-chip transceiver that complies with the physical layer specifications for Universal Serial Bus (USB). The MIC2550A supports full-speed (12Mbps) and low-speed (1.5Mbps) operation and introduces superior edge rate control to produce crisper eye diagrams. As a result, the task of passing USB compliance testing is made easier.

A unique, patented, dual supply voltage operation allows the MIC2550A to reference the system I/F I/O signals to a supply voltage down to 2.5V while independently powered by the USB V_{BUS}. This allows the system interface to operate at its core voltage without addition of buffering logic and also reduce system operating current.

Features

- Compliant to USB Specification Revision 2.0 for low-speed (1.5Mbps) and full-speed (12Mbps) operation
- Compliant to IEC-61000-4.2 (Level 2)
- Operation down to 2.5V
- Dual supply voltage operation
- Integrated speed-select termination supply
- Very low power consumption meets USB suspend-current requirements
- Small 14-pin TSSOP and 16-pin MLF™ packages

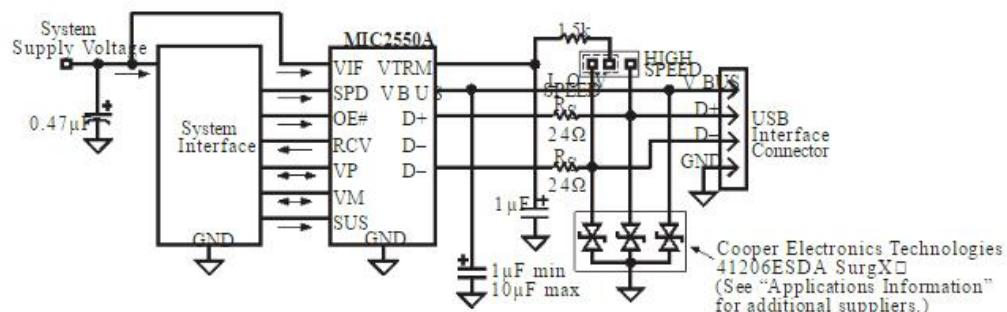
Applications

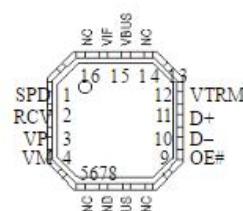
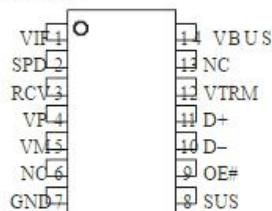
- Personal digital assistants (PDA)
- Palmtop computers
- Cellular telephones

Ordering Information

Part Number	Pb-Free	Package
Standard		
MIC2550ABTS	MIC2550AYTS	14-Pin TSSOP
MIC2550ABML	MIC2550AYML	16-Pin MLF™

System Diagram



Pin Configuration**Pin Description**

Pin Name	Pin Number MIC2550ABTS	Pin Number MIC2550ABML	Pin Function
VIF	1	15	System Interface Supply Voltage (Input): Determines logic voltage levels for system interface signaling to logic controller.
SPD	2	1	Speed (Input): Edge rate control. Logic high selects full-speed edge rates. Logic low selects low-speed edge rates.
RCV	3	2	Receive Data (Output): System interface receive data interface to logic controller.
VP	4	3	Plus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VP is a receiver output (+); If OE# is logic 0, VP is a driver input (+).
VM	5	4	Minus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VM is a receiver output (-); If OE# is logic 0, VM is a driver input (-).
NC	6, 13	5, 8, 13, 16	Not internally connected
GND	7	6	Ground: Power supply return and signal reference.
SUS	8	7	Suspend (Input): Logic high turns off internal circuits to reduce supply current.
OE#	9	9	Output Enable (Input): Active low system interface input signal from controller. Logic low causes transceiver to transmit data onto the bus; logic high causes the transceiver to receive data from the bus.
D-	10	10	USB Differential Data Line - (Input/Output)
D+	11	11	USB Differential Data Line + (Input/Output)
VTRM	12	12	Termination Supply (Output): 3.3V speed termination resistor supply output
VBUS	14	14	USB Supply Voltage (Input): Transceiver supply.

Absolute Maximum Ratings (Note 1)				Operating Ratings (Note 2)			
Supply Voltage (V_{IF})	+6.5V		Supply Voltage (V_{BUS})	4.0V to 5.25V	
Input Voltage (V_{BUS})	-0.5V(min)/5.5V(max)		Temperature Range (T_A)	-40°C to +85°C	
Output Current ($D+, ID-$)	±50mA		Junction Temperature (T_J)	160°C	
Output Current (all others)	±15mA		Package Thermal Resistance			
Input Current	±50mA		TSSOP (θ _{JA})	100°C/W	
Storage Temperature (T_S)	-65° to +150°C					
ESD, Note 3							
$V_{BUS}, D+, D-$		=10kV					
All other pins		=2kV					
Electrical Characteristics (Note 8)							
$T_A = 25^\circ\text{C}$, bold values indicate $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$; typical values at $V_{BUS} = 5.0\text{V}$, $V_{IF} = 3.0\text{V}$; minimum and maximum values at $V_{BUS} = 4.0\text{V}$ to 5.25V/ $V_{IF} = 2.5\text{V}$ to 3.6V, unless noted.							
Symbol	Parameter	Condition			Min	Typ	Max
System and USB Interface DC Characteristics							
V_{BUS}	USB Supply Voltage				4.0		5.25
V_{IF}	System I/F Supply Voltage				2.5		5.25
V_{IL}	Low-Level Input Voltage, Note 4						0.15 V_{IF}
V_{IH}	High-Level Input Voltage, Note 4				0.85 V_{IF}		
V_{OH}	High-Level Output Voltage, Note 4				0.9 V_{IF}		
V_{OL}	Low-Level Output Voltage, Note 4						0.1
I_{IL}	Input Leakage Current, Note 4						±5 μA
Symbol	Parameter	Conditions			Min	Typ	Max
		SPD	SUS	OE#	Voltage	Load	Units
I_{IF}	VIF Supply Current	101			VBUS = 5.25V VIF = 3.6V $f = 6\text{MHz}$ CLOAD = 50 pF, Note 7 $f = 750\text{kHz}$ CLOAD = 600 pF Note 7		1
		100					5 μA
		001					5 μA
		0	0	0			5 μA
		01		0			5 μA
		10		0f		325	650 μA
		00		0		40	75 μA
I_{VBUS}	VBUS Supply Current	10		1	VBUS = 5.25V VIF = 3.6V $f = 6\text{MHz}$ CLOAD = 50 pF, Note 7 $f = 750\text{kHz}$ CLOAD = 600 pF Note 7		800
		10		0			3000 5000 μA
		001					230 350 μA
		000					400 700 μA
		0	1	0			130 200 μA
		10		0			7.3 10 mA
		00		0			3.6 5 mA
V_{TRM}	Termination Voltage	$I_{TRM} = 2.5\text{mA}$				3.0	3.6 V
ESD Protection							
IEC-1000-4-2	Air Discharge	10 pulses				± 6 kV	
(D+, D-, V_{BUS} only)	Contact Discharge	10 pulses				± 6 kV	

Symbol	Parameter	Condition	Min	Typ	Max	Units
Transceiver DC Characteristics						
I_{LO}	Hi-Z State Data Line Leakage	$0V \leq V_{BUS} \leq 3.3V, D+, D-, OE\# = 1$ pins only	-10		+10	μA
V_{DI}	Differential Input Sensitivity	$ D+ - D- _{IN} = 0.8V - 2.5V$	0.2			V
V_{CM}	Differential Common-Mode Range	Includes V_I range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis, Note 6			200		mV
V_{OL}	Static Output Low, Note 5	$OE\# = 0, R = 1.5k\Omega$ to 3.6V			0.3	V
V_{OH}	Static Output High, Note 5	$OE\# = 0, R = 1.5k\Omega$ to GND	2.8		3.6	V
V_{CRS}	Output Signal Crossover Voltage, Note 6		1.3		2.0	V
C_{IN}	Transceiver Capacitance, Note 6	Bin to GND			20	pF
Z_{DRV}	Driver Output Resistance	Steady state drive, Note 6	6	8		Ω
Low-Speed Driver Characteristics, Note 7						
t_R	Transition Rise Time	$C_L = 50pF$ $C_L = 600pF$	75		300	ns ns
t_F	Transition Fall Time	$C_L = 50pF$ $C_L = 600pF$	75		300	ns ns
t_{R+F}	Rise and Fall Time Matching	$T_R = T_F$	80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Full-Speed Driver Characteristics, Note 7						
t_R	Transition Rise Time	$C_L = 50pF$	4		20	ns
t_F	Transition Fall Time	$C_L = 50pF$	4		20	ns
t_{R+F}	Rise and Fall Time Matching	$T_R = T_F$	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
Transceiver Timing, Note 7						
t_{PVZ}	OE# to RCVR Tri-state Delay	Figure 1			15	ns
t_{PZD}	Receiver Tri-state to Transmit Delay	Figure 1	15			ns
t_{PDZ}	OE# to DRVR Tri-state Delay	Figure 1			15	ns
t_{PZV}	Driver Tri-state to Receiver Delay	Figure 1	15			ns
t_{PLH}	$V+/V-$ to $D+/D-$ Propagation Delay	Figure 4			15	ns
t_{PHL}	$V+/V-$ to $D+/D-$ Propagation Delay	Figure 4			15	ns
t_{PLH}	$D+/D-$ to RCV Propagation Delay	Figure 3			15	ns
t_{PHL}	$D+/D-$ to RCV Propagation Delay	Figure 3			15	ns
t_{PLH}	$D+/D-$ to $V+/D-$ Propagation Delay	Figure 3			8	ns
t_{PHL}	$D+/D-$ to $V+/D-$ Propagation Delay	Figure 3			8	ns

Note 1.Exceeding the absolute maximum rating may damage the device.

Note 2.The device is not guaranteed to function outside its operating rating.

Note 3.Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4.Applies to the VP, VM, RCV, OE#, SPD, and SUS pins.

Note 5.Applies to D+, D-.

Note 6.Not production tested. Guaranteed by design.

Note 7.Characterized specification(s), but not production tested.

Timing Diagrams

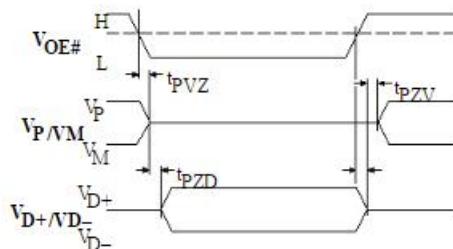


Figure 1. Enable and Disable Times

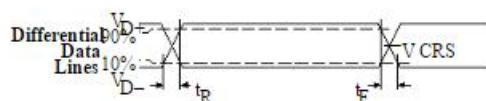
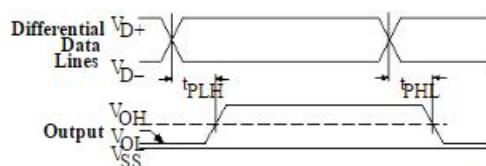
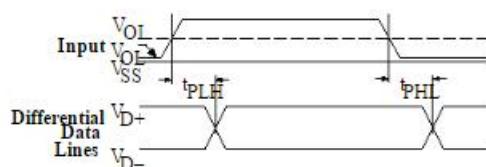


Figure 2. Rise and Fall Times

Figure 3. Receiver Propagation Delay $V_{D+}/D-$ to RCV, V_P , and V_M Figure 4. Driver Propagation Delay V_P and V_M to $D+/D-$

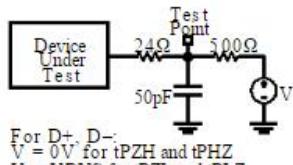
OE# = 0 (Transmit):					Result
VM	V+	D-	DV	RC	
0000				X	SE0
01010					Logic 0
10101					Logic 1
1111				X	Undefined

OE# = 1 (Receive):					Result
D+	DP	VM	VV	RC	
0000				X	SE0
01010					Logic 0
10101					Logic 1
1111				X	Undefined

Note. X = undefined.

Table 1. Truth Table

Test Circuits



For D+, D-:
V = 0V for tPZH and tPHZ
V = VBUS for tPZL and tPLZ

Figure 5. Load for Enable and Disable Time (D+, D-)

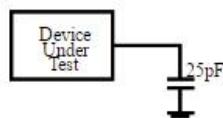
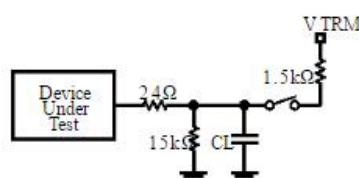
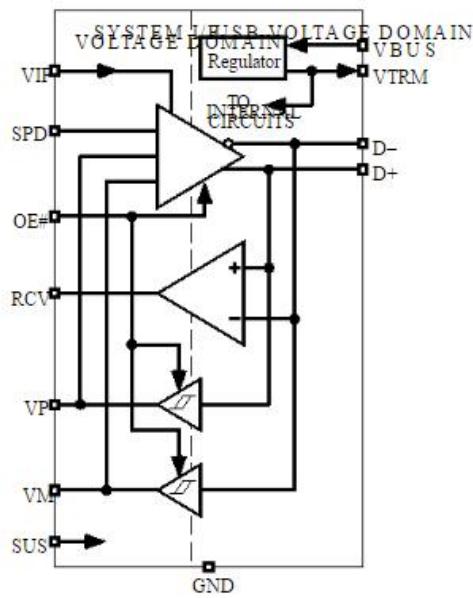


Figure 6. V_P, VM and RCV Load



CL = 50pF, full speed
CL = 50pF, low speed (minimum timing)
CL = 600pF, low speed (maximum timing)
*1.5k on D- for low speed or D+ for high speed

Figure 7. D+ and D- Load

Block Diagram

Applications Information

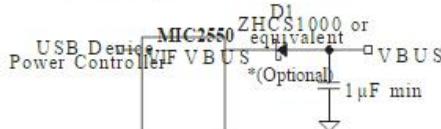
The MIC2550A is designed to provide USB connectivity in mobile systems where system supply voltages are not available to satisfy USB requirements. The MIC2550A can operate down to supply voltages of 2.5V and still meet USB physical layer specifications. As shown in the system diagram, the MIC2550A takes advantage of USB's supply voltage, V_{BUS} , to operate the transceiver. The system voltage, V_{IF} , is used to set the reference voltage used by the digital I/O lines (V_IF, V_M, RCV, OE#, SPD, and SUS pins) interfacing to the system. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the system.

In addition, a 3.3V, 10% termination supply voltage, V_{TRM} , is provided to support speed selection. A 0.47μF (minimum) capacitor from V_{TRM} to ground is required to ensure stability. A 1.5K resistor is required between this pin and the D_{+D}- or D_{-D} lines to respectively specify full-speed or low-speed operation.

Power Supply Configurations

V_{IF}/V_{BUS} Switched

When the V_{BUS} input pin is pulled to ground a low impedance path between V_{IF} and V_{BUS} can cause a high current flow from V_{IF} to V_{BUS} thereby damaging the MIC2550A. This issue can arise in systems where V_{BUS} is driven from a power supply that can be switched off such as in the case of a desktop PC. Adding a Schottky diode, such as the ZHCS1000 by Zetex, in series with V_{BUS} will prevent any current flow during this condition. A solution is shown in Figure 8 below. If the V_{IF} source is current limited to less than 50mA, then diode D1 is not necessary.



Note: *(Optional) See Text - Power Supply Configurations

Figure 8. Solution to V_{IF}/V_{BUS} Switching

I/O Interface Using 3.3V

In systems where the I/O interface utilizes a 3.3V USB controller, an alternate solution is shown in Figure 9. This configuration has the advantage over Figure 8, in that no extra components are needed. Ensure that the load on V_{TRM} does not exceed 1mA total.

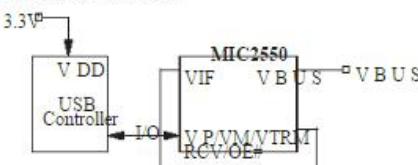


Figure 9. I/O Interface Using 3.3V

Internal 3.3V Source

If the device is self-powered and has 3.3V available, the circuit in Figure 10 is yet another power supply configuration option. In this configuration, the internal regulator is disabled and the 3.3V source and not V_{BUS} powers the entire chip.



Figure 10. Powering Chip from Internal 3.3V Source

Suspend

When the suspend pin (SUS) is high, power consumption is reduced to a minimum. V_{TRM} is not disabled, RCV, VP and VM are still functional to enable the device to detect USB activity. For minimal current consumption in suspend mode, it is recommended that OE# = 1, and SPD = 0.

Speed

The speed pin (SPD) sets D_{+D}- output edge rates by increasing or decreasing biasing current sources within the output drivers. For low speed, SPD = 0. For full speed, SPD = 1. By setting SPD = 0 during idle periods, in conjunction with suspend (SUS), the lowest quiescent current can be obtained. However, designers must provide a 300ns delay between changing SPD from 0 to 1 and transmission of data at full speed. This delay ensures the output drivers have arrived at their proper operating conditions. Failure to do so can result in leading edge distortion on the first few data bits transmitted.

External ESD Protection

The use of ESD transient protection devices is not required for operation, but is recommended. We recommend the following devices or the equivalent:

Cooper Electronics Technologies (www.cooperet.com)
41206ESDA SurgX®
0805ESDA SurgX®

Littelfuse (www.littelfuse.com)

V0402MHS05
SP0503BAHT

Non-multiplexed Bus

To save pin count for the USB logic controller interface, the MIC2550A was designed with VP and VM as bidirectional pins. To interface the MIC2550A with a non-multiplexed data bus, resistors can be used for low cost isolation as shown in Figure 11.

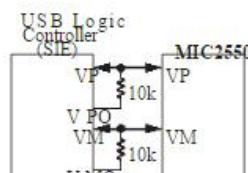


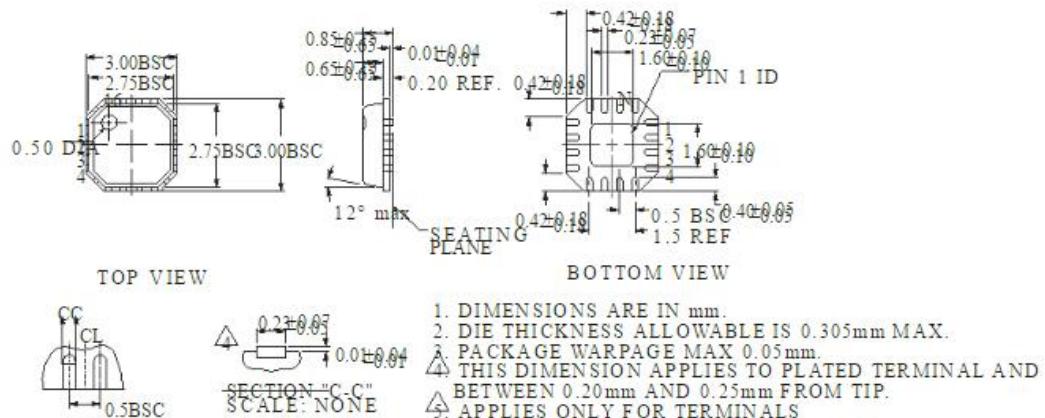
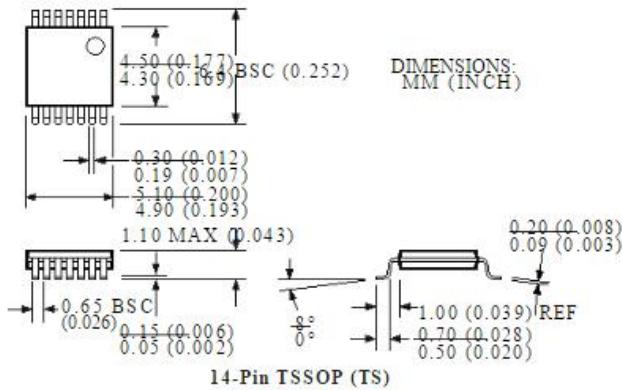
Figure 11. MIC2550A Interface to Non-multiplexed Data Bus

PCB Layout Recommendations

Although the USB standard and applications are not based in an impedance controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

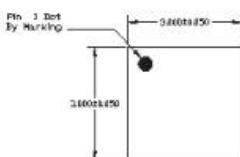
- Match signal line traces (VP/VM, D+, D-) to 40ps, approximately $\frac{1}{4}$ inch if possible. FR-4 PCB material propagation is about 150ps/inch, so to minimize skew try to keep VP/VM, D+/D- traces as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5–2 widths. Place all other traces at $>2w$ from all signal line traces.
- Maintain the same number of vias on each differential trace, keeping traces approximately at same separation distance along the line.
- Control signal line impedances to $\pm 10\%$.
- Keep R_s as close to the IC as possible, with equal distance between R_s and the IC for both D+ and D-.

Package Information

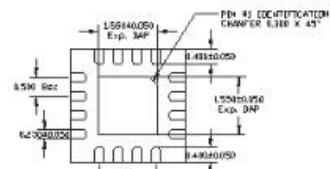


Rev. 02

16-Pin MLF™ (ML)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS .005 MM.
3. MAXIMUM ALLOWABLE BURPS IS .0075 MM IN ALL DIRECTIONS.
4. PIN 1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin MLF™ (ML)