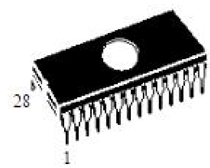
M27512

NMOS 512 Kbit (64Kb x 8) UV EPROM

NOT FOR NEW DESIGN

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V



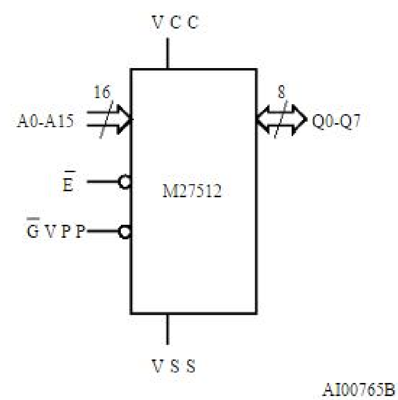
FDIP28W (F)

DESCRIPTION

The M27512 is a 524,288 bit UV erasable and electrically programmable memory EPROM. It is organized as 65,536 words by 8 bits.

The M27512 is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Figure 1. Logic Diagram



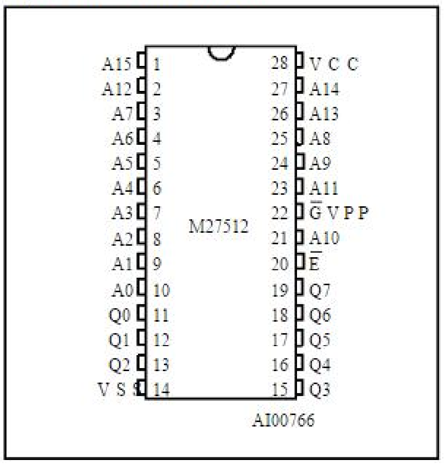
This is information on a product still in production but not recommended for new designs.

Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
TA	Ambient Operating Temperature	Grade 1 Grade 6	0 to 70 –40 to 85	°C
TBIAS	Temperature Under Bias	Grade 1 Grade 6	–10 to 80 –50 to 95	°C
TSTG	Storage Temperature		–65 to 125	°C
V IO	Input or Output Voltages		–0.6 to 6.5	V
V CC	Supply Voltage		–0.6 to 6.5	V
V A9	A9 Voltage		–0.6 to 13.5	V
V PP	Program Supply		–0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratin permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions a indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions fo may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for GVPP and 12V on A9 for Electronic Signature.

Read Mode

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (E) is the power control and should be used for device selection. Output Enable (G) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (tAVQV) is equal to the delay from E to output (tELQV). Data is available at the outputs after delay of tGLQV from the falling edge of G, assuming that E has been low and the addresses have been stable for at least tAVQV-tGLQV.

Standby Mode

The M27512 has a standby mode which reduces the maximum active power current from 125mA to 40mA. The M27512 is placed in the standby mode by applying a TTL high signal to the E input. When in the standby mode, the outputs are in a high impedance state, independent of the GVPP input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a. the lowest possible memory power dissipation,

b. complete assurance that output bus contention will not occur.

DEVICE OPERATION (cont'd)

For the most efficient use of these two control lines, E should be decoded and used as the primary device selecting function, while GVPP should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of fast EPROMs require careful decoupling of the devices.

The supply current, ICC, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of E. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommenced that a 1 µF ceramic capacitor be used on every device between VCC and VSS. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between VCC and VSS for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when GVPP input is at 12.5V and E is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO Programming Algorithm that drastically reduces the programming time (typically less than 50 seconds). Nevertheless to achieve compatibility with all programming equipment, the standard Fast Programming Algorithm may also be used.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in Figure 8.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$VPP	A9	Q0 - Q7
Read	VIL	VIL	X	Data Out
Output Disable	VIL	VIH	X	Hi-Z
Program	VIL Pulse	VPP	X	Data In
Verify	VIH	VIL	X	Data Out
Program Inhibit	VIH	VPP	X	Hi-Z
Standby	VIH	X	X	Hi-Z
Electronic Signature	VIL	VIL	VID	Codes

Note: X = VIH or VIL, VID = 12V ± 0.5V

Table 4. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	VIL	00100					00		0	20h
Device Code	VIH	00001					10		1	0Dh

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.45V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

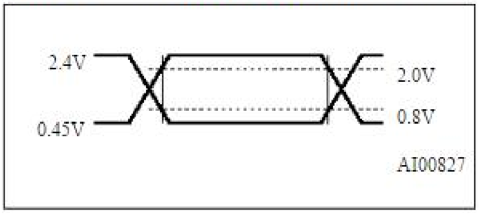


Figure 4. AC Testing Load Circuit

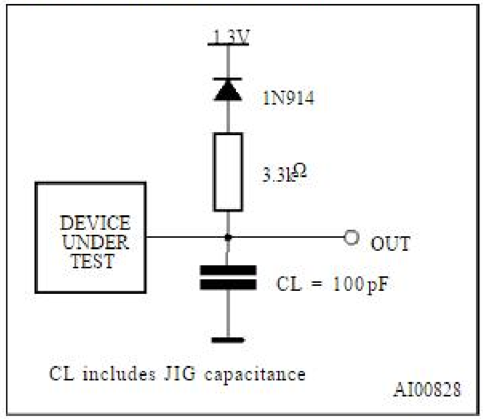


Table 5. Capacitance **(1)** (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Figure 5. Read Mode AC Waveforms

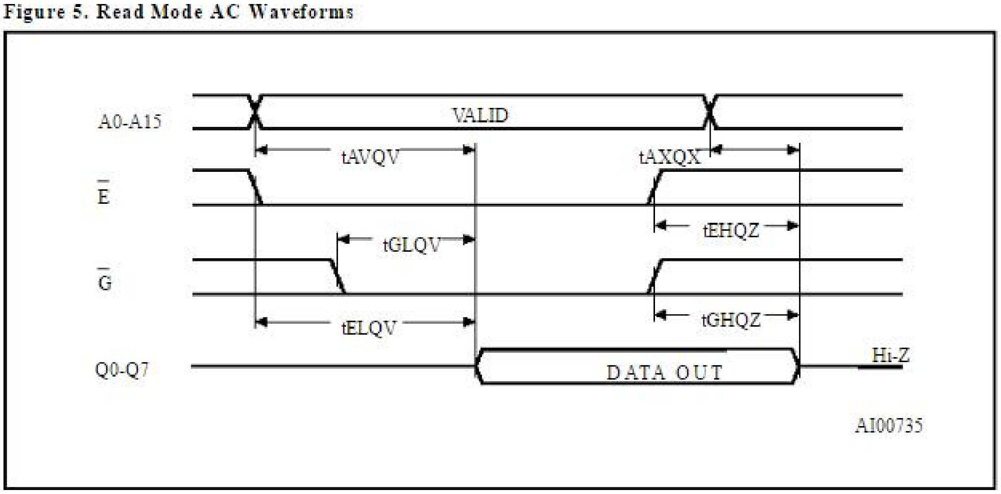


Table 6. Read Mode DC Characteristics (1)
(TA = 0 to 70 °C or –40 to 85 °C; VCC = 5V ± 5% or 5V ± 10%; VPP = VCC)

Symbol	Parameter	Test Condition	Min	Max	Unit
ILI	Input Leakage Current	0 ≤ VIN ≤ VCC		±10	µA
ILO	Output Leakage Current	VOUT = VCC		±10	µA
ICC	Supply Current	$\overline{E}$ = VIL, $\overline{G}$ = VIL		125	mA
ICC1	Supply Current (Standby)	$\overline{E}$ = VIH		40	mA
VIL	Input Low Voltage		–0.1	0.8	V
VIH	Input High Voltage		2	VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1mA		0.45	V
VOH	Output High Voltage	IOH = –400µA	2.4		V

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

Table 7. Read Mode AC Characteristics (1)
(TA = 0 to 70 °C or –40 to 85 °C; VCC = 5V ± 5% or 5V ± 10%; VPP = VCC)

Symbol	Alt	Parameter	Test Condition	M27512						Unit
				-2, -20		blank, -25		-3		
				Min	Max	Min	Max	Min	Max	
tAVQV	tACC	Address Valid to Output Valid	$\overline{E}$ = VIL, $\overline{G}$ = VIL		200		250		300	ns
tELQV	tCE	Chip Enable Low to Output Valid	$\overline{G}$ = VIL		200		250		300	ns
tGLQV	tOE	Output Enable Low to Output Valid	$\overline{E}$ = VIL		75		100		120	ns
tEHQZ (2)	tDF	Chip Enable High to Output Hi-Z	$\overline{G}$ = VIL	0	55	0	60	0	105	ns
tGHQZ (2)	tDF	Output Enable High to Output Hi-Z	$\overline{E}$ = VIL	0	55	0	60	0	105	ns
tAXQX	tOH	Address Transition to Output Transition	$\overline{E}$ = VIL, $\overline{G}$ = VIL	00				0		ns

Notes: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.
2. Sampled only, not 100% tested.

Table 8. Programming Mode DC Characteristics (1)
(TA = 25 °C; VCC = 6.25V ± 0.25V; VPP = 12.75V ± 0.25V)

Symbol	Parameter	Test Condition	Min	Max	Unit
ILI	Input Leakage Current	VIL ≤ VIN ≤ VIH		±10	µA
ICC	Supply Current			150	mA
IPP	Program Current	$\overline{E}$ = VIL		50	mA
VIL	Input Low Voltage		–0.1	0.8	V
VIH	Input High Voltage		2	VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1mA		0.45	V
VOH	Output High Voltage	IOH = –400µA	2.4		V
VID	A9 Voltage		11.5	12.5	V

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

Table 9. MARGIN MODE AC Characteristics (1)
(TA = 25 °C; VCC = 6.25V ± 0.25V; VPP = 12.75V ± 0.25V)

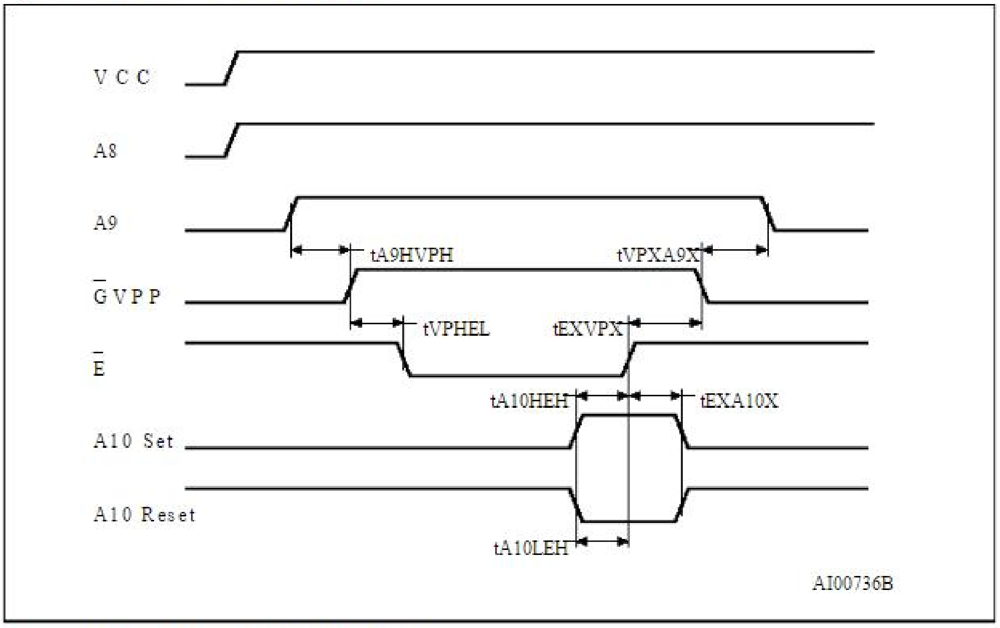
Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
tA9HVPH	tAS9	VA9 High to VPP High		2		μs
tVPHEL	tVPS	VPP High to Chip Enable Low		2		μs
tA10HEH	tAS10	VA10 High to Chip Enable High (Set)		1		μs
tA10LEH	tAS10	VA10 Low to Chip Enable High (Reset)		1		μs
tEXA10X	tAH10	Chip Enable Transition to VA10 Transition		1		μs
tEXVPX	tVPH	Chip Enable Transition to VPP Transition		2		μs
tVPXA9X	tAH9	VPP Transition to VA9 Transition		2		μs

Note: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.

Table 10. Programming Mode AC Characteristics (1)
(TA = 25 °C; VCC = 6.25V ± 0.25V; VPP = 12.75V ± 0.25V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
tAVEL	tAS	Address Valid to Chip Enable Low		2		μs
tQVEL	tDS	Input Valid to Chip Enable Low		2		μs
tVCHEL	tVCS	VCC High to Chip Enable Low		2		μs
tVPHEL	tOES	VPP High to Chip Enable Low		2		μs
tVPLVPH	tPRT	VPP Rise Time		50		ns
tELEH	tPW	Chip Enable Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
tELEH	tOPW	Chip Enable Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
tEHQX	tDH	Chip Enable High to Input Transition		2		μs
tEHVPX	tOEH	Chip Enable High to VPP Transition		2		μs
tVPLEL	tVR	VPP Low to Chip Enable Low		2		μs
tELQV	tDV	Chip Enable Low to Output Valid			1	μs
tEHQZ (4)	tDF	Chip Enable High to Output Hi-Z		0	130	ns
tEHAX	tAH	Chip Enable High to Address Transition		0 n	s	

Figure 6. MARGIN MODE AC Waveform



Note: A8 High level = 5V; A9 High level = 12V.

Figure 7. Programming and Verify Modes AC Waveforms

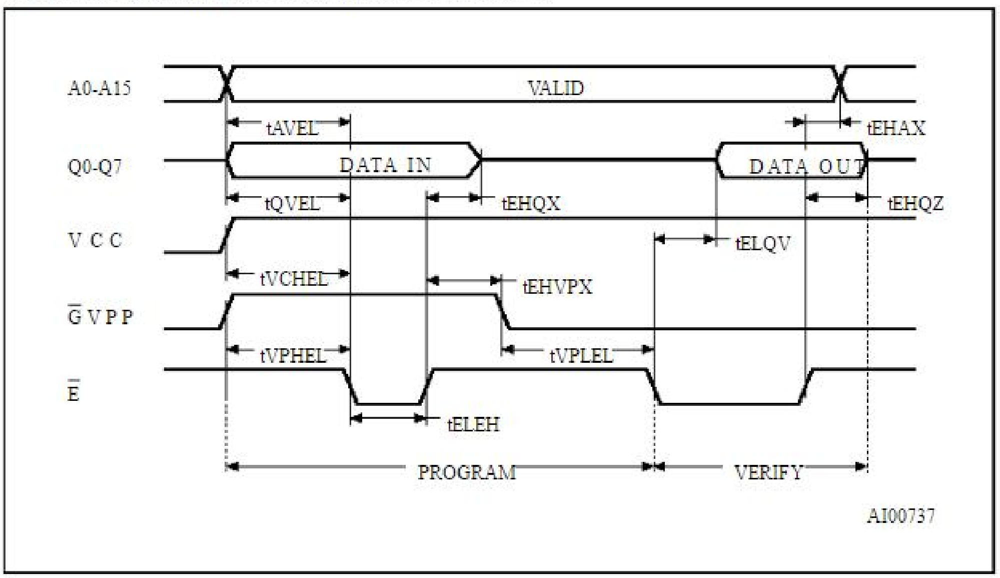


Figure 8. Fast Programming Flowchart

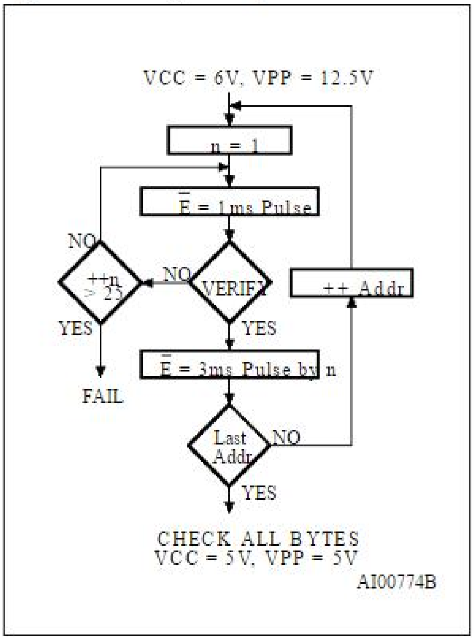
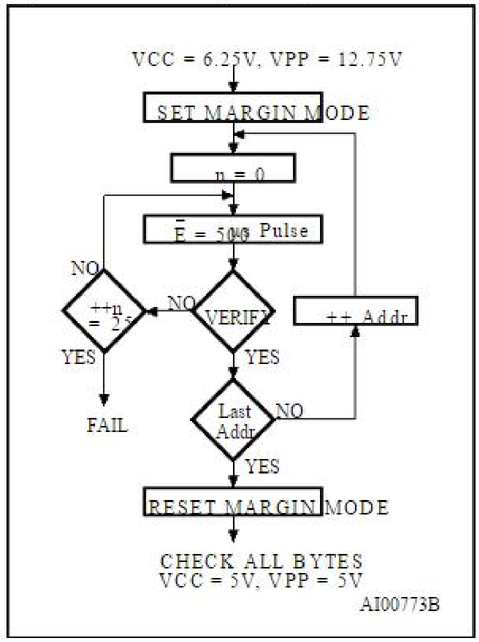


Figure 9. PRESTO Programming Flowchart



DEVICE OPERATION (cont'd)

The Fast Programming Algorithm utilizes two different pulse types : initial and overprogram. The duration of the initial E pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.
The entire sequence of program pulses is performed at VCC = 6V and GVPP = 12.5V (byte verifications at VCC = 6V and GVPP = VIL). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with VCC = 5V.

PRESTO Programming Algorithm

PRESTO Programming Algorithm allows to program the whole array with a guaranted margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with the STMicroelectronics M27512 due to several design innovations described for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is programmed with enough margin.
Then a sequence of 500 µs program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.

Program Inhibit

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for E, all like inputs (including GVPP) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's E input, with GVpp at 12.5V, will program that M27512. A high level E input inhibits the other M27512s from being programmed.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with GVpp and E at VIL. Data should be verified tDV after the falling edge of E.

Electronic Signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25 °C ± 5 °C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during Electronic Signature mode, except for A14 and A15 which should be high. Byte 0 (A0 = VIL) represents the manufacturer code and byte 1 (A0 = VIH) the device identifier code.

ERASURE OPERATION (applies to UV EPROM)

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å.
The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm2 power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION SCHEME

Example: M27512 -2 F 1

Speed and VCC Tolerance

-2	200 ns, 5V ± 5%
blank	250 ns, 5V ± 5%
-3	300 ns, 5V ± 5%
-20	200 ns, 5V ± 10%
-25	250 ns, 5V ± 10%

Package

F	FDIP28W

Temperature Range

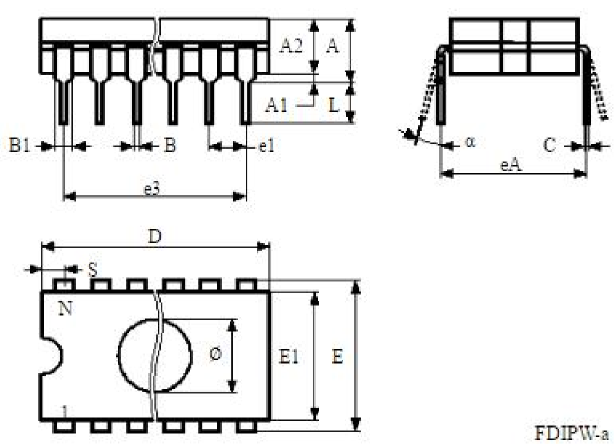
1	0 to 70 °C
6	–40 to 85 °C

For a list of available options (Speed, VCC Tolerance, Package, etc) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact STMicroelectronics Sales Office nearest to you.

FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
Ø	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N2	8			28		



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