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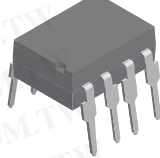
勝特力材料 886-3-5753170
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ILD1, ILD2, ILD5, ILQ1, ILQ2, ILQ5

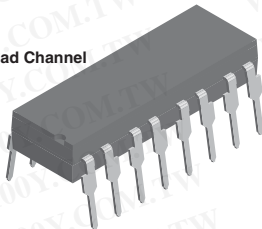
Vishay Semiconductors

Optocoupler, Phototransistor Output (Dual, Quad Channel)

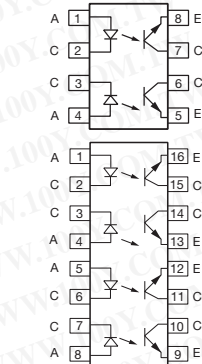
Dual Channel



Quad Channel



i179012-1



FEATURES

- Current transfer ratio at $I_F = 10 \text{ mA}$
- Isolation test voltage, $5300 \text{ V}_{\text{RMS}}$
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC



RoHS COMPLIANT

AGENCY APPROVALS

- UL1577, file no. E52744 system code H, double protection
- CSA 93751
- BSI IEC 60950; IEC 60065
- DIN EN 60747-5-2 (VDE 0884) available with option 1
- FIMKO

DESCRIPTION

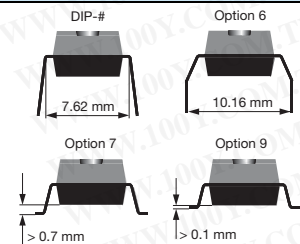
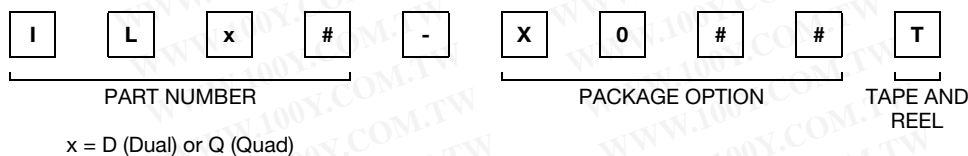
The ILD1, ILD2, ILD5, ILQ1, ILQ2, ILQ5 are optically coupled isolated pairs employing GaAs infrared LEDs and silicon NPN phototransistor. Signal information, including a DC level, can be transmitted by the drive while maintaining a high degree of electrical isolation between input and output.

The ILD1, ILD2, ILD5, ILQ1, ILQ2, ILQ5 are especially designed for driving medium-speed logic and can be used to eliminate troublesome ground loop and noise problems. Also these couplers can be used to replace relays and transformers in many digital interface applications such as CTR modulation.

The ILD1, ILD2, ILD5 has two isolated channels in a single DIP package and the ILQ1, ILQ2, ILQ5 has four isolated channels per package.

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ORDERING INFORMATION



AGENCY CERTIFIED/PACKAGE	DUAL CHANNEL			QUAD CHANNEL		
	CTR (%)					
UL, CSA, BSI, FIMKO	20 to 300	100 to 500	50 to 400	20 to 300	100 to 500	50 to 400
DIP-8	ILD1	ILD2	ILD5	-	-	-
DIP-8, 400 mil, option 6	-	ILD2-X006	-	-	-	-
SMD-8, option 7	ILD1-X007T ⁽¹⁾	ILD2-X007T ⁽¹⁾	-	-	-	-
SMD-8, option 9	ILD1-X009T ⁽¹⁾	ILD2-X009T ⁽¹⁾	ILD5-X009T ⁽¹⁾	-	-	-
DIP-16	-	-	-	ILQ1	ILQ2	ILQ5
DIP-16, 400 mil, option 6	-	-	-	ILQ1-X006	ILQ2-X006	-
SMD-16, option 7	-	-	-	ILQ1-X007	ILQ2-X007T ⁽¹⁾	-
SMD-16, option 9	-	-	-	ILQ1-X009T ⁽¹⁾	ILQ2-X009T ⁽¹⁾	ILQ5-X009T ⁽¹⁾



AGENCY CERTIFIED/PACKAGE	DUAL CHANNEL			QUAD CHANNEL		
	CTR (%)					
VDE, UL, CSA, BSI, FIMKO	20 to 300	100 to 500	50 to 400	20 to 300	100 to 500	50 to 400
DIP-8	ILD1-X001	ILD2-X001	ILD5-X001	-	-	-
DIP-8, 400 mil, option 6	-	ILD2-X016	-	-	-	-
SMD-8, option 7	-	ILD2-X017	-	-	-	-
SMD-8, option 9	ILD1-X019T	-	-	-	-	-
DIP-16	-	-	-	-	ILQ2-X001	-
DIP-16, 400 mil, option 6	-	-	-	-	ILQ2-X016	-
SMD-16, option 7	-	-	-	-	ILQ2-X017T (1)	-

Notes

- Additional options may be possible, please contact sales office.
- (1) Also available in tubes; do not put T on end.

ABSOLUTE MAXIMUM RATINGS (T _{amb} = 25 °C, unless otherwise specified)					
PARAMETER	TEST CONDITION	PART	SYMBOL	VALUE	UNIT
INPUT					
Reverse voltage			V _R	6	V
Forward current			I _F	60	mA
Surge current			I _{FSM}	2.5	A
Power dissipation			P _{diss}	100	mW
Derate linearly from 25 °C				1.3	mW/°C
OUTPUT					
Collector emitter reverse voltage		ILD1	V _{CEO}	50	V
		ILQ1	V _{CEO}	50	V
		ILD2	V _{CEO}	70	V
		ILQ2	V _{CEO}	70	V
		ILD5	V _{CEO}	70	V
		ILQ5	V _{CEO}	70	V
Collector current	t < 1 ms		I _C	50	mA
			I _C	400	mA
Power dissipation			P _{diss}	200	mW
Derate linearly from 25 °C				2.6	mW/°C
COUPLER					
Isolation test voltage between emitter and detector			V _{ISO}	5300	V _{RMS}
Creepage distance				≥ 7	mm
Clearance distance				≥ 7	mm
Isolation resistance	V _{IO} = 500 V, T _{amb} = 25 °C		R _{IO}	≥ 10 ¹²	Ω
	V _{IO} = 500 V, T _{amb} = 100 °C		R _{IO}	≥ 10 ¹¹	
Package power dissipation			P _{tot}	250	mW
Derate linearly from 25 °C				3.3	mW/°C
Storage temperature			T _{stg}	- 40 to + 150	°C
Operating temperature			T _{amb}	- 40 to + 100	°C
Junction temperature			T _j	100	°C
Soldering temperature (2)	2 mm from case bottom		T _{slid}	260	°C

Notes

- Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute maximum ratings for extended periods of the time can adversely affect reliability.
- (1) Refer to reflow profile for soldering conditions for surface mounted devices (SMD). Refer to wave profile for soldering conditions for through hole devices (DIP).



ELECTRICAL CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
INPUT						
Forward voltage	I _F = 60 mA	V _F		1.25	1.65	V
Reverse current	V _R = 6 V	I _R		0.01	10	μA
Capacitance	V _R = 0 V, f = 1 MHz	C _O		25		pF
Thermal resistance, junction to lead		T _{thJL}		750		K/W
OUTPUT						
Collector emitter capacitance	V _{CE} = 5 V, f = 1 MHz	C _{CE}		6.8		pF
Collector emitter leakage current	V _{VCE} = 10 V	I _{CEO}		5	50	nA
Saturation voltage, collector emitter	I _C = 1 mA, I _B = 20 μA	V _{CEsat}		0.25	0.4	V
DC forward current gain	V _{CE} = 10 V, I _B = 20 μA	h _{FE}	200	650	1800	
DC forward current gain saturated	V _{CE} = 0.4 V, I _B = 20 μA	h _{FEsat}	120	400	600	
Thermal resistance, junction to lead		R _{thjl}		500		K/W
COUPLER						
Capacitance (input to output)	V _{IO} = 0 V, f = 1 MHz	C _{IO}		0.8		pF

Note

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

CURRENT TRANSFER RATIO (T _{amb} = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
I _C /I _F (collector emitter saturated)	I _F = 10 mA, V _{CE} = 0.4 V	ILD1	CTR _{CEsat}		75		%
		ILQ1	CTR _{CEsat}		75		%
		ILD2	CTR _{CEsat}		170		%
		ILQ2	CTR _{CEsat}		170		%
		ILD5	CTR _{CEsat}		100		%
		ILQ5	CTR _{CEsat}		100		%
	I _F = 10 mA, V _{CE} = 10 V	ILD1	CTR _{CE}	20	80	300	%
		ILQ1	CTR _{CE}	20	80	300	%
		ILD2	CTR _{CE}	100	200	500	%
		ILQ2	CTR _{CE}	100	200	500	%
		ILD5	CTR _{CE}	50	130	400	%
		ILQ5	CTR _{CE}	50	130	400	%

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SAFETY AND INSULATION RATINGS						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Isolation test voltage between emitter and detector		V_{ISO}	5300			V_{RMS}
Isolation resistance	$V_{IO} = 500\text{ V}, T_{amb} = 25\text{ °C}$	R_{IO}	10^{12}			Ω
	$V_{IO} = 500\text{ V}, T_{amb} = 100\text{ °C}$		10^{11}			
Climatic classification (according to IEC 68 part 1)				55/100/21		
Comparative tracking index		CTI	175			
Rated impulse voltage		V_{IOTM}			10	kV
Maximum working voltage	Recurring peak voltage	V_{IORM}			890	V
Forward current		I_{SI}			275	mA
Power dissipation		P_{SO}			400	mW
Safety temperature		T_{SI}			175	°C
Creepage distance			7.0			mm
Clearance distance			7.0			mm
Insulation distance	per IEC 60950 2.10.5.1		0.4			mm

Note

- According to DIN EN 60747-5-2 (VDE 0884) (see figure 2). These optocouplers are suitable for “safety electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

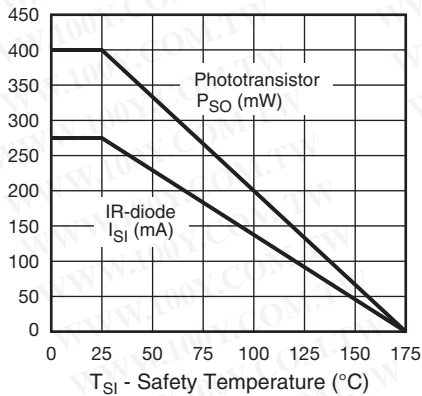


Fig. 1 - Derating Diagram

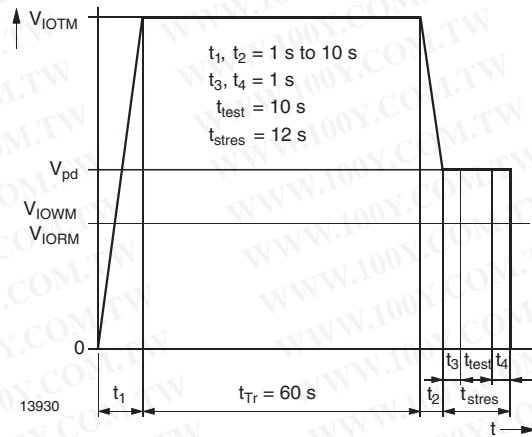


Fig. 2 - Test Pulse Diagram for Sample Test according to DIN EN 60747-5-2 (VDE 0884); IEC 60747-5-5

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SWITCHING CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
NON-SATURATED							
Current	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	I _F		20		mA
		ILQ1	I _F		20		mA
		ILD2	I _F		5		mA
		ILQ2	I _F		5		mA
		ILD5	I _F		10		mA
		ILQ5	I _F		10		mA
Delay	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _D		0.8		μs
		ILQ1	t _D		0.8		μs
		ILD2	t _D		1.7		μs
		ILQ2	t _D		1.7		μs
		ILD5	t _D		1.7		μs
		ILQ5	t _D		1.7		μs
Rise time	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _r		1.9		μs
		ILQ1	t _r		1.9		μs
		ILD2	t _r		2.6		μs
		ILQ2	t _r		2.6		μs
		ILD5	t _r		2.6		μs
		ILQ5	t _r		2.6		μs
Storage	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _s		0.2		μs
		ILQ1	t _s		0.2		μs
		ILD2	t _s		0.4		μs
		ILQ2	t _s		0.4		μs
		ILD5	t _s		0.4		μs
		ILQ5	t _s		0.4		μs
Fall time	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _f		1.4		μs
		ILQ1	t _f		1.4		μs
		ILD2	t _f		2.2		μs
		ILQ2	t _f		2.2		μs
		ILD5	t _f		2.2		μs
		ILQ5	t _f		2.2		μs
Propagation H to L	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _{PHL}		0.7		μs
		ILQ1	t _{PHL}		0.7		μs
		ILD2	t _{PHL}		1.2		μs
		ILQ2	t _{PHL}		1.2		μs
		ILD5	t _{PHL}		1.1		μs
		ILQ5	t _{PHL}		1.1		μs
Propagation L to H	V _{CE} = 5 V, R _L = 75 Ω, 50 % of V _{PP}	ILD1	t _{PLH}		1.4		μs
		ILQ1	t _{PLH}		1.4		μs
		ILD2	t _{PLH}		2.3		μs
		ILQ2	t _{PLH}		2.3		μs
		ILD5	t _{PLH}		2.5		μs
		ILQ5	t _{PLH}		2.5		μs

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SWITCHING CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)							
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT
SATURATED							
Current	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	I_F		20		mA
		ILQ1	I_F		20		mA
		ILD2	I_F		5		mA
		ILQ2	I_F		5		mA
		ILD5	I_F		10		mA
		ILQ5	I_F		10		mA
Delay	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_D		0.8		μs
		ILQ1	t_D		0.8		μs
		ILD2	t_D		1		μs
		ILQ2	t_D		1		μs
		ILD5	t_D		1.7		μs
		ILQ5	t_D		1.7		μs
Rise time	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_r		1.2		μs
		ILQ1	t_r		1.2		μs
		ILD2	t_r		2		μs
		ILQ2	t_r		2		μs
		ILD5	t_r		7		μs
		ILQ5	t_r		7		μs
Storage	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_s		7.4		μs
		ILQ1	t_s		7.4		μs
		ILD2	t_s		5.4		μs
		ILQ2	t_s		5.4		μs
		ILD5	t_s		4.6		μs
		ILQ5	t_s		4.6		μs
Fall time	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_f		7.6		μs
		ILQ1	t_f		7.6		μs
		ILD2	t_f		13.5		μs
		ILQ2	t_f		13.5		μs
		ILD5	t_f		20		μs
		ILQ5	t_f		20		μs
Propagation H to L	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_{PHL}		1.6		μs
		ILQ1	t_{PHL}		1.6		μs
		ILD2	t_{PHL}		5.4		μs
		ILQ2	t_{PHL}		5.4		μs
		ILD5	t_{PHL}		2.6		μs
		ILQ5	t_{PHL}		2.6		μs
Propagation L to H	$V_{CE} = 0.4\text{ V}$, $R_L = 1\text{ k}\Omega$, $V_{CC} = 5\text{ V}$, $V_{TH} = 1.5\text{ V}$	ILD1	t_{PLH}		8.6		μs
		ILQ1	t_{PLH}		8.6		μs
		ILD2	t_{PLH}		7.4		μs
		ILQ2	t_{PLH}		7.4		μs
		ILD5	t_{PLH}		7.2		μs
		ILQ5	t_{PLH}		7.2		μs

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COMMON MODE TRANSIENT IMMUNITY ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Common mode rejection, output high	$V_{CM} = 50\text{ V}_{P-P}$, $R_L = 1\text{ k}\Omega$, $I_F = 0\text{ mA}$	CM_H		5000		$\text{V}/\mu\text{s}$
Common mode rejection, output low	$V_{CM} = 50\text{ V}_{P-P}$, $R_L = 1\text{ k}\Omega$, $I_F = 10\text{ mA}$	CM_L		5000		$\text{V}/\mu\text{s}$
Common mode coupling capacitance		C_{CM}		0.01		pF

TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

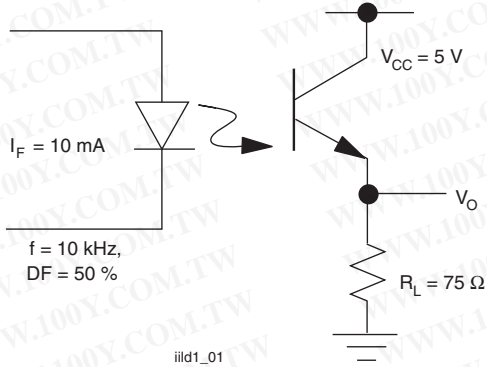


Fig. 3 - Non-Saturated Switching Schematic

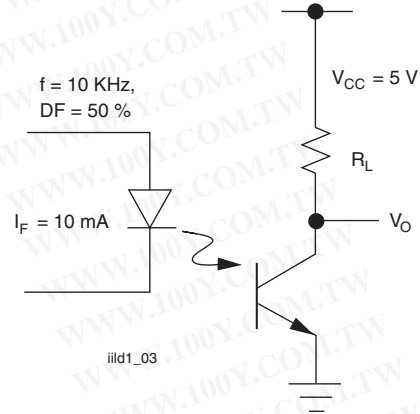


Fig. 5 - Saturated Switching Schematic

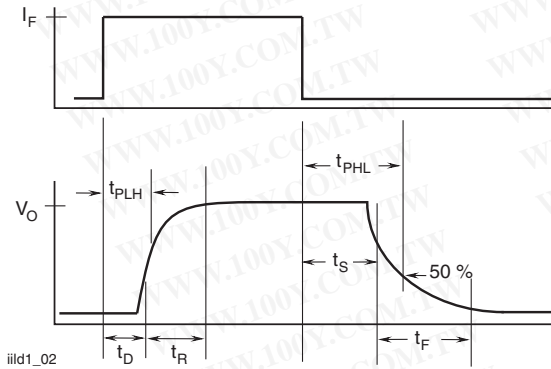


Fig. 4 - Non-Saturated Switching Timing

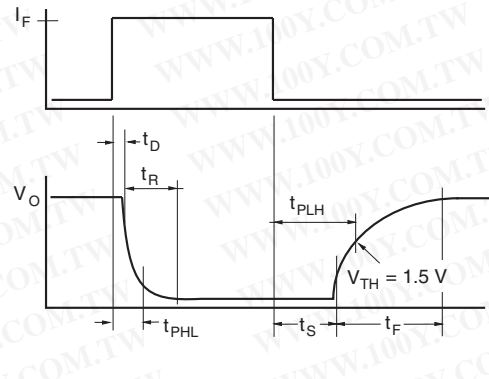


Fig. 6 - Saturated Switching Timing

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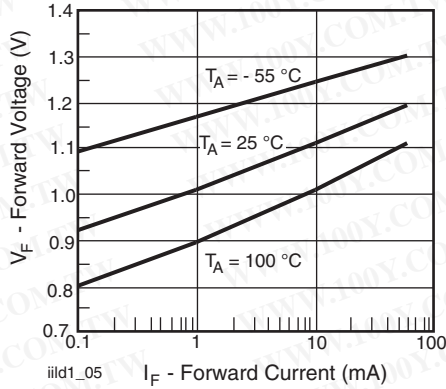


Fig. 7 - Normalized Non-Saturated and Saturated CTR vs. LED Current

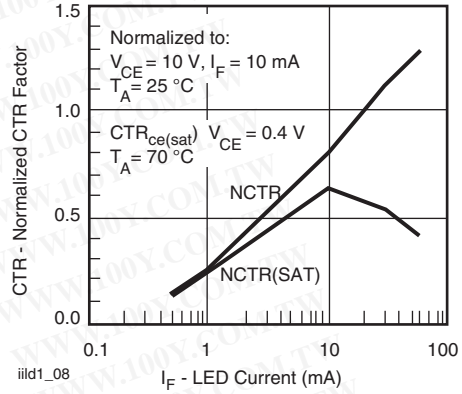


Fig. 10 - Normalized Non-Saturated and Saturated CTR vs. LED Current

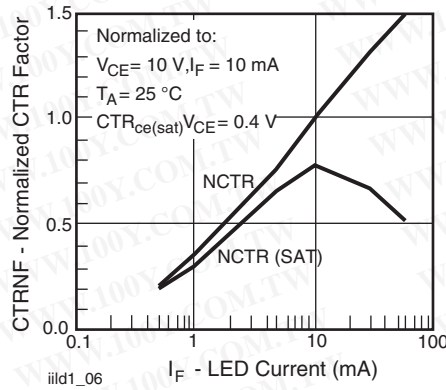


Fig. 8 - Normalized Non-Saturated and Saturated CTR vs. LED Current

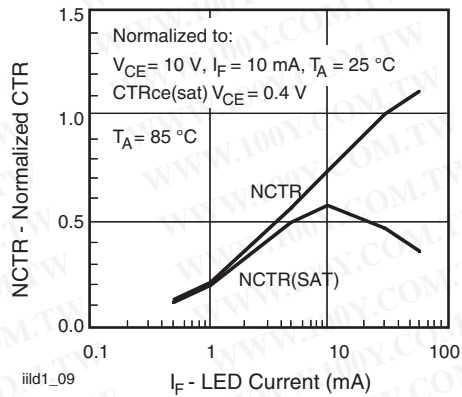


Fig. 11 - Normalized Non-Saturated and Saturated CTR vs. LED Current

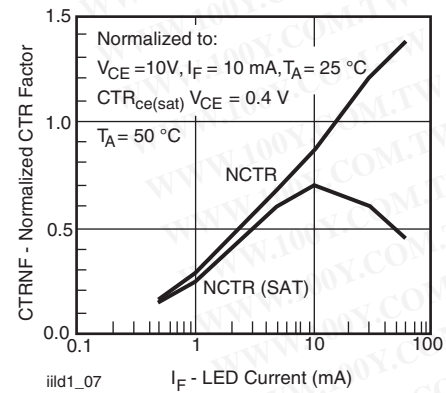


Fig. 9 - Normalized Non-Saturated and Saturated CTR vs. LED Current

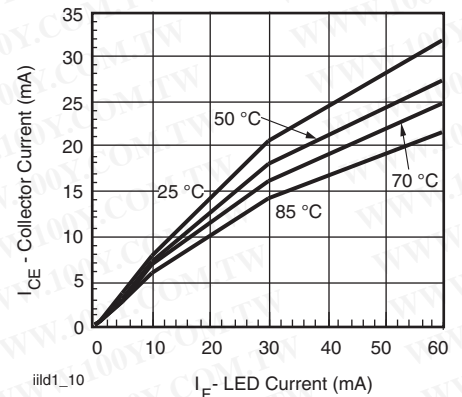


Fig. 12 - Collector Emitter Current vs. Temperature and LED Current

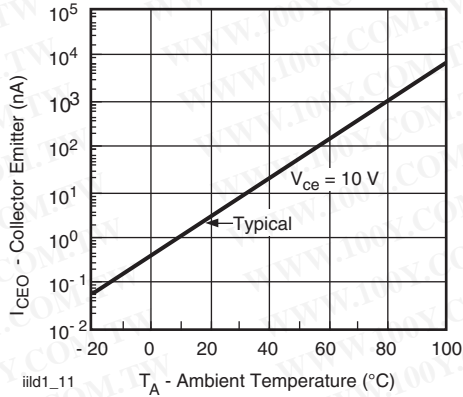


Fig. 13 - Collector Emitter Leakage Current vs. Temperature

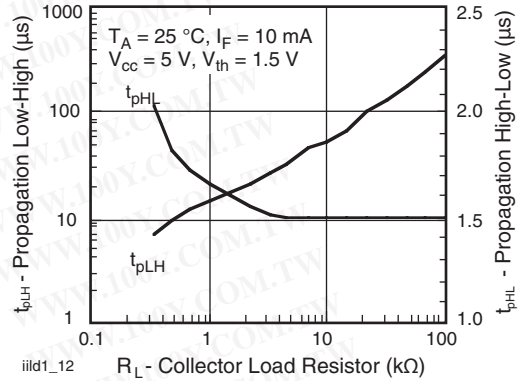
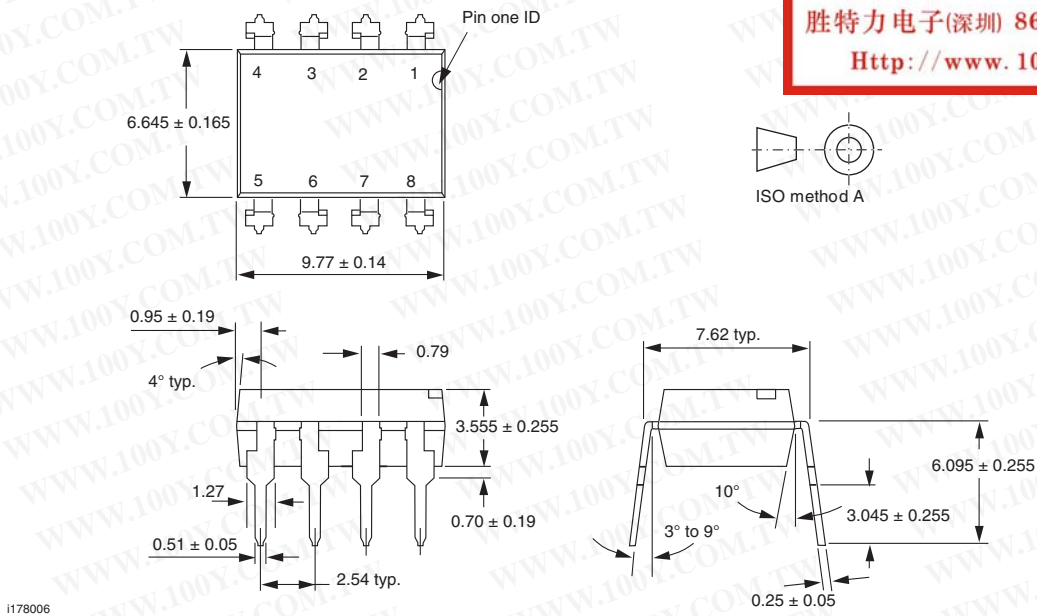


Fig. 14 - Propagation Delay vs. Collector Load Resistor

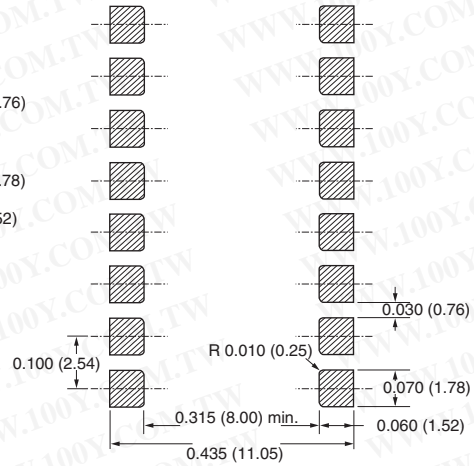
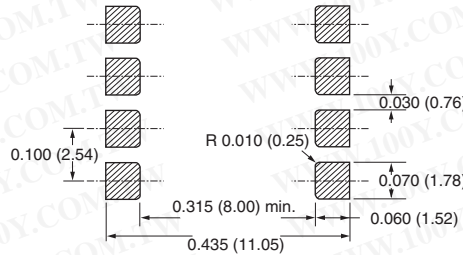
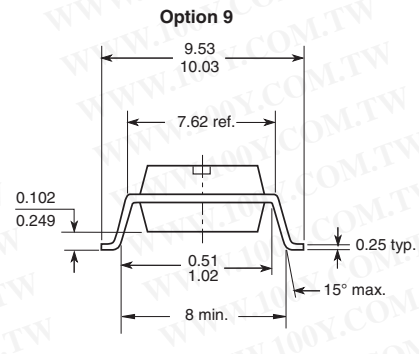
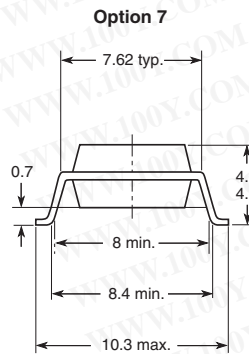
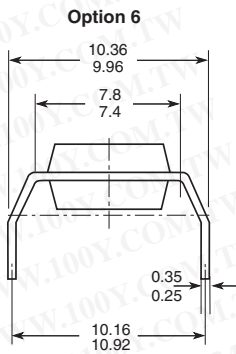
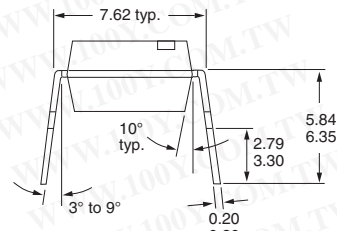
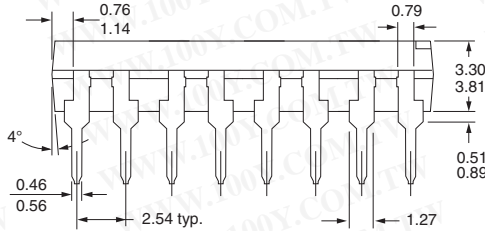
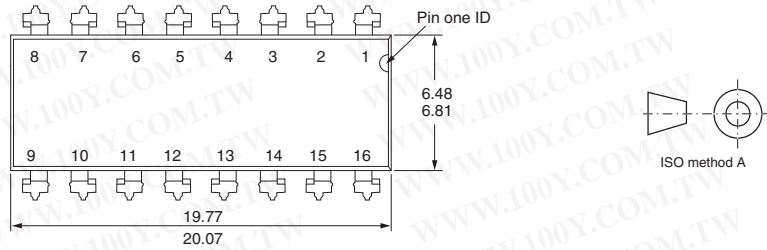
PACKAGE DIMENSIONS in millimeters



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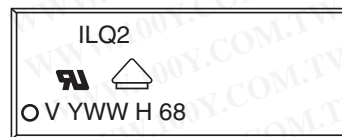
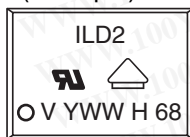


PACKAGE DIMENSIONS in millimeters



18450-9

PACKAGE MARKING (example)



Notes

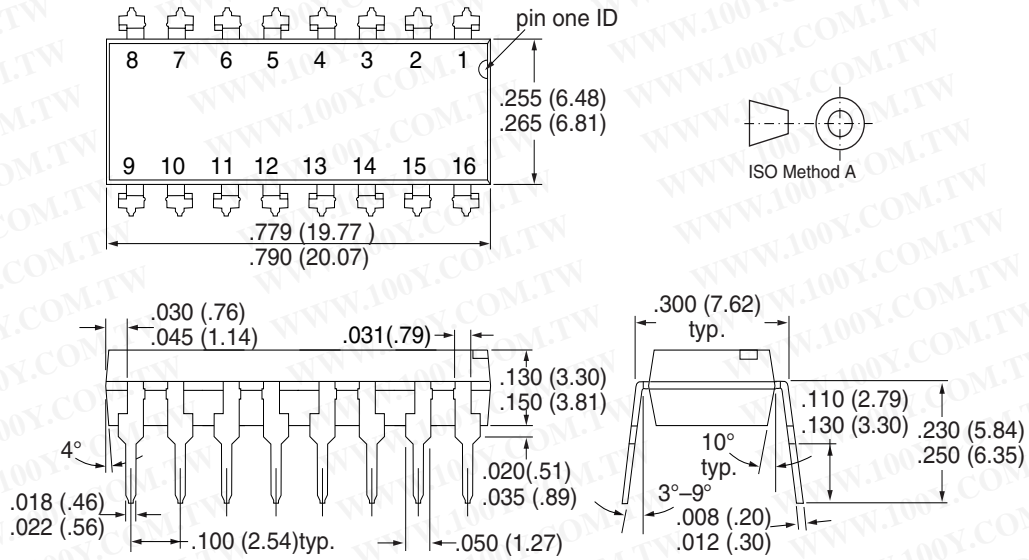
- Only option 1 and 7 reflected in the package marking.
- The VDE logo is only marked on option 1 parts.
- Tape and reel suffix (T) is not part of the package marking.



DIP-16

Package Dimensions in Inches (mm)

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i178007



Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design
and may do so without further notice.**

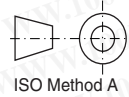
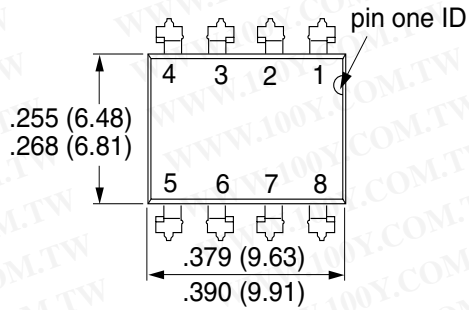
Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Vishay Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify Vishay Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

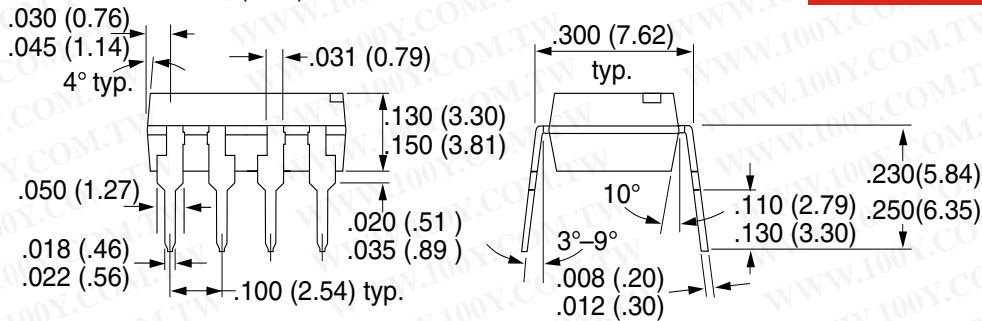


DIP-8

Package Dimensions in Inches (mm)



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i178006



Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

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Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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**We reserve the right to make changes to improve technical design
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Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

Footprints

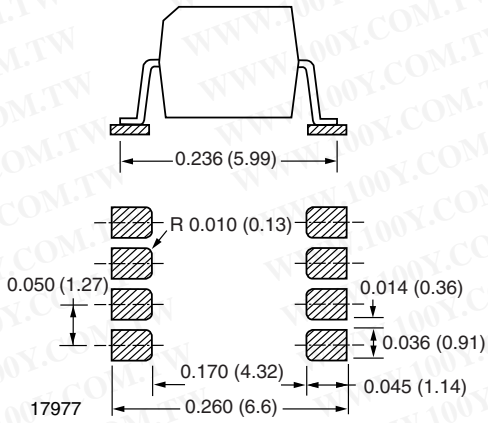


Fig. 1 - SO8A and DSO8A SMD

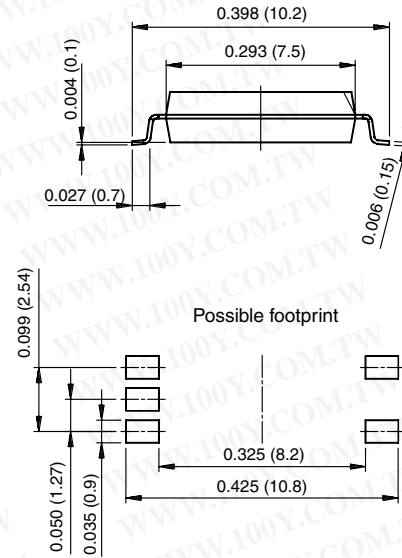


Fig. 3 - SOP-6, 5 Pin Wide Body

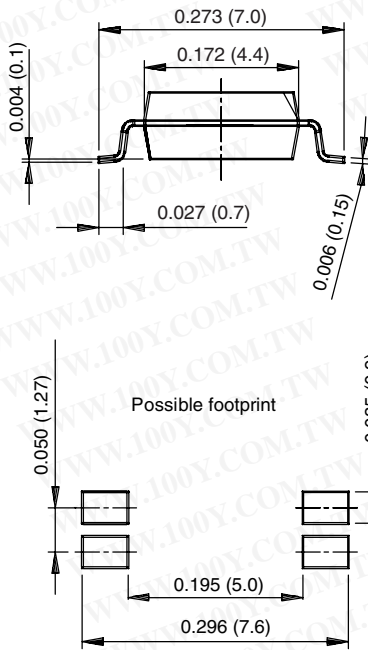


Fig. 2 - SOP-4, Miniflat

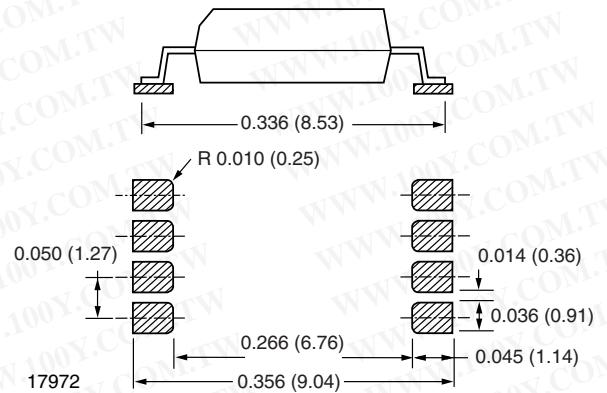


Fig. 4 - 8 Pin PCMCIA

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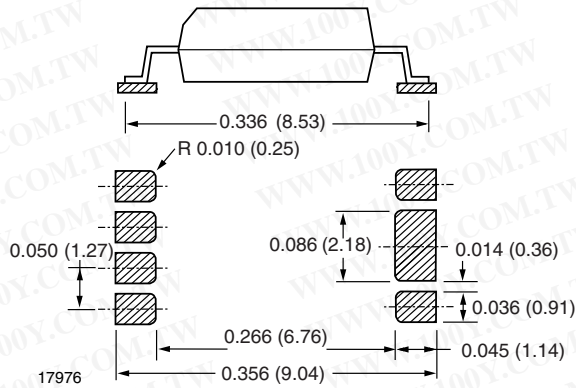


Fig. 5 - 8 Pin PCMCIA, Heat Sink

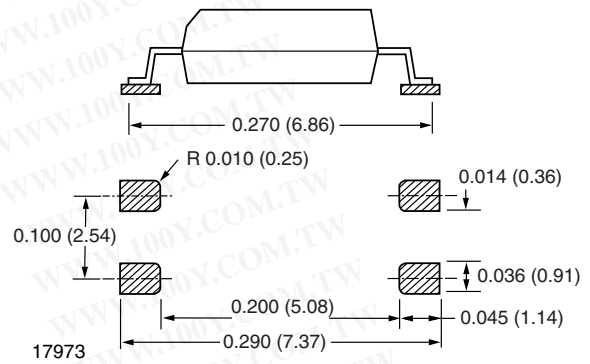


Fig. 8 - 4 Pin Mini-Flat

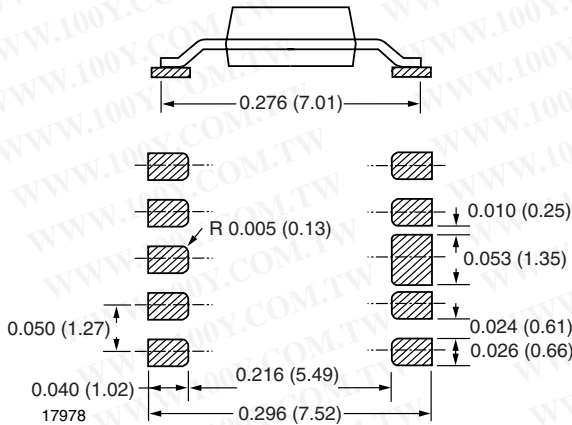


Fig. 6 - Mini Coupler

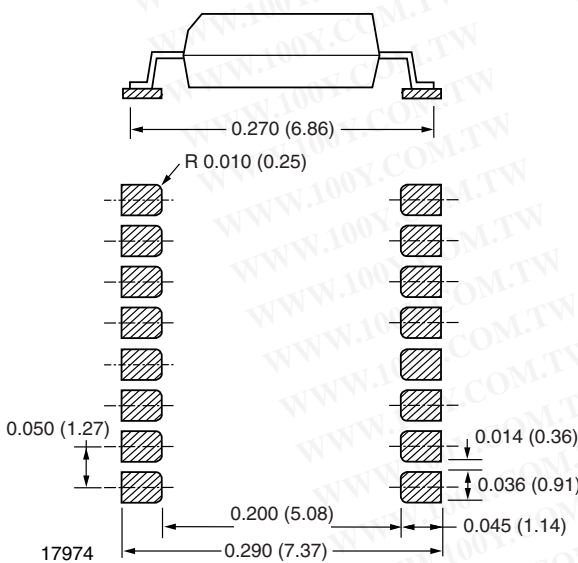


Fig. 7 - SOP-16

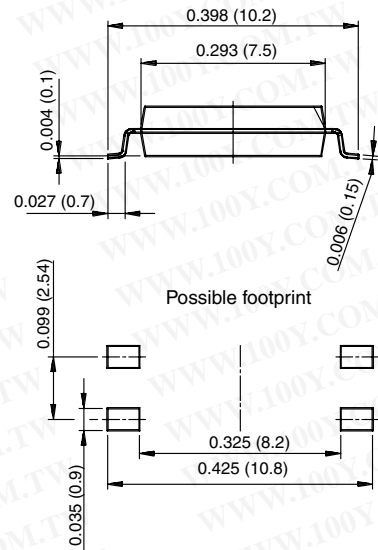


Fig. 9 - SOP-6, 4 Pin Wide Body

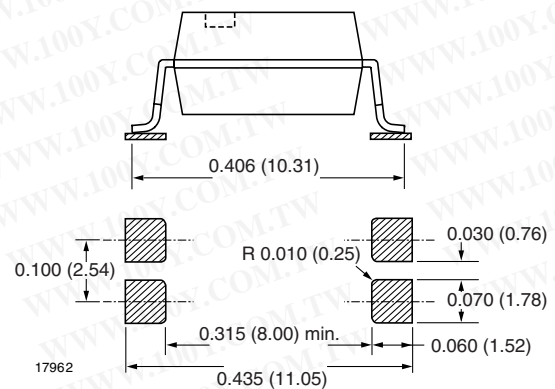


Fig. 10 - 4 Pin SMD Option 7

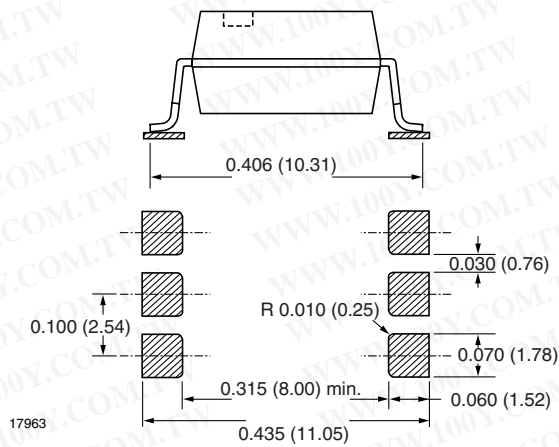


Fig. 11 - 6 Pin SMD Option 7

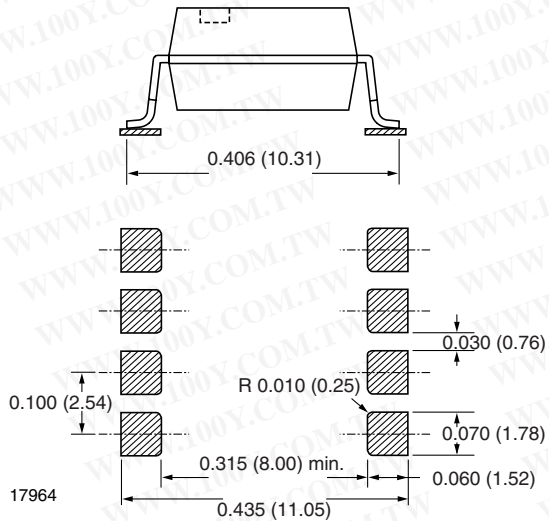


Fig. 12 - 8 Pin SMD Option 7

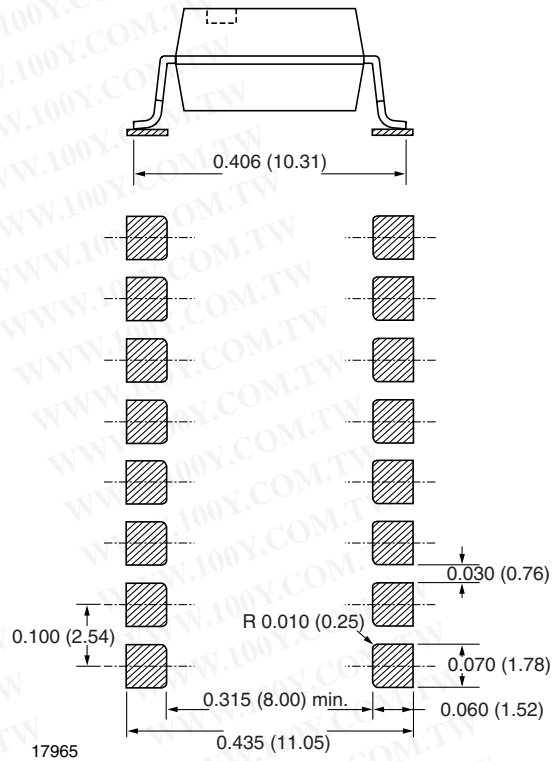


Fig. 13 - 16 Pin SMD Option 7

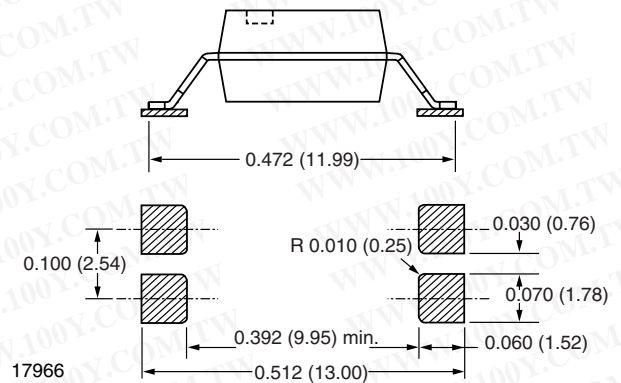


Fig. 14 - 4 Pin SMD Option 8

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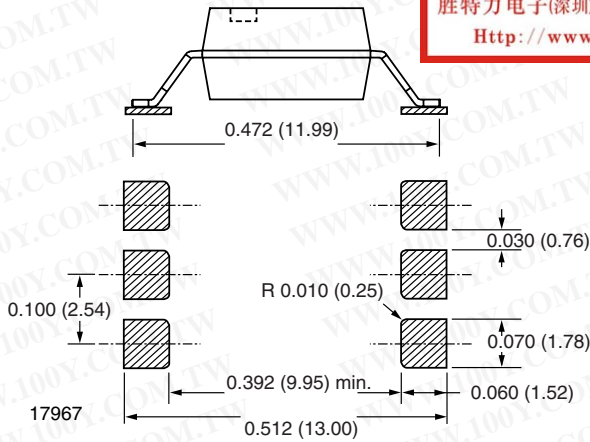


Fig. 15 - 6 Pin SMD Option 8

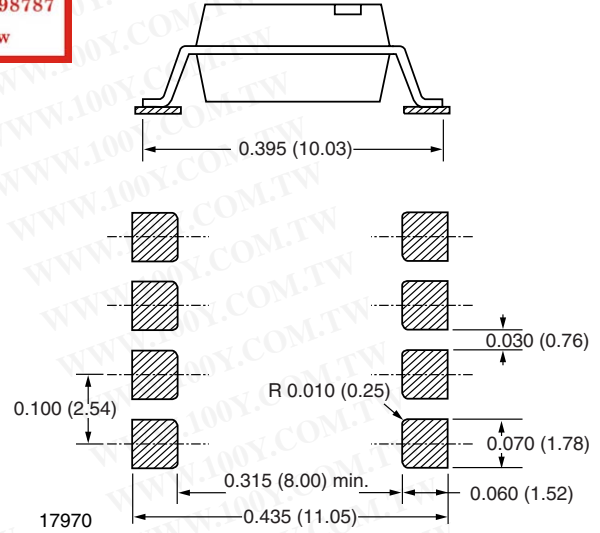


Fig. 18 - 8 Pin SMD Option 9

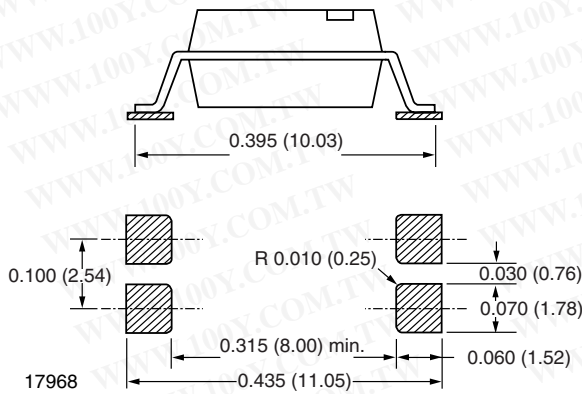


Fig. 16 - 4 Pin SMD Option 9

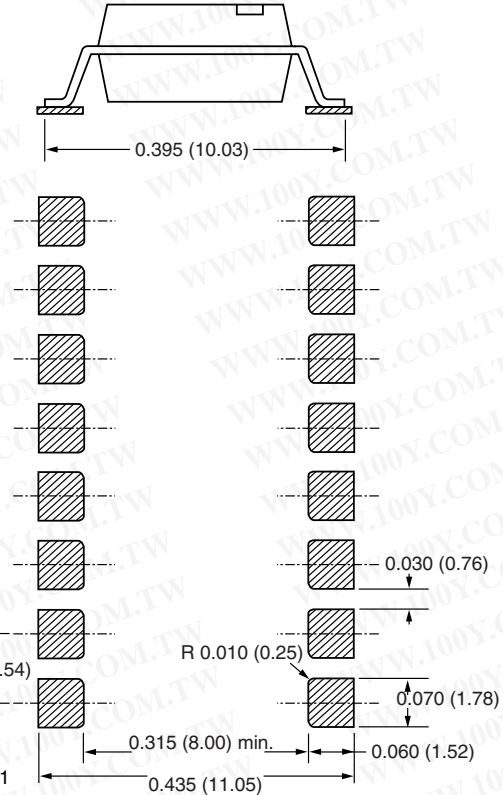


Fig. 19 - 16 Pin SMD Option 9

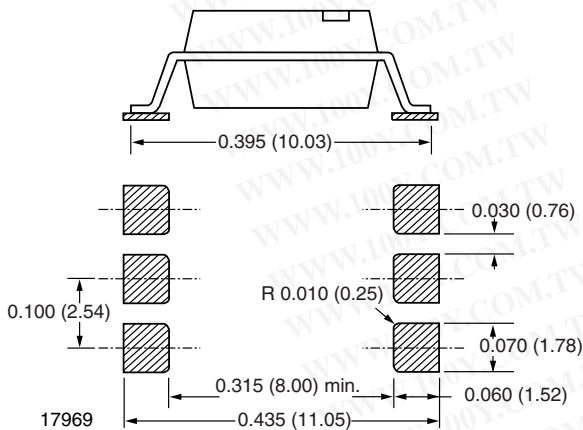


Fig. 17 - 6 Pin SMD Option 9

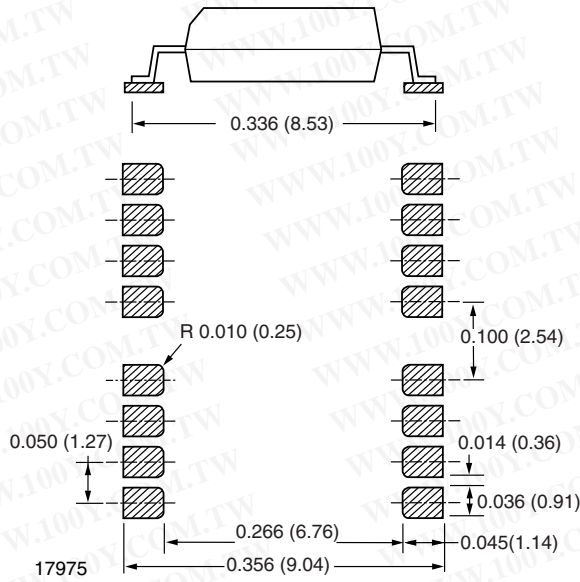


Fig. 20 - 16 Pin PCMCIA

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