28F400BV/CV/CE
28F004BV/BE
SPECIFICATION UPDATE

Release Date: February 1997

Order Number: 297595-013

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
01/16/95	-001	Initial release of this document. Includes the following: Limited V_{CC} Voltage, Reduced V_{LKO} (Commercial/Automotive), 3.3V V_{CC} /12V V_{PP} Programming Erratum, t_{PHWL}/t_{PHEL} Pushout, CE# delay from RP# High, t_{PLPH} Reset Pulse Width, Erroneous Erase Fail Flag Operation.
02/08/95	-002	New erratum: t_{PLQZ} - New Spec, False V_{PP} Flag, Access Time. Additional ID and erratum information for Erroneous Erase Fail Flag erratum.
03/07/95	-003	New erratum: t_{WHEH} - CMOS Control Signals, CE# Timing Erratum/ A_{-1} Timing Erratum. Addition to False V_{PP} Flag Erratum.
03/22/95	-004	Errata summary format changed to include more information. Automotive V_{LKO} erratum: spec changed from 3.5V to 2.0V. Erase Fail Flag: Re-issue erase option added to resolution. Address Timing: Erratum error corrected Affected pin is A_{10} for 28F004, not A_0 as listed in Rev 003. Title also changed to "Address Timing Erratum" from "A_{-1} Timing Erratum."
03/31/95	-005	Access time erratum removed: no material ever affected by this erratum.
04/13/95	-006	CMOS Control Signals erratum title changed to TTL-Level Control Signals erratum. Erratum spec also changed from requiring $V_{CC} \pm 0.2V$ to 4.0V (min), V_{CC} + 0.2V (max) on control pins.
08/09/95	-007	Table format identification criteria added to most items. t_{PHWL}/t_{PHEL} Pushout Erratum: Improved for B-step. CE# Delay from RP# High: Changed to apply to A-step only and not to B-step. t_{PLPH} Reset Pulse Width: Changed to reflect B-step improvements. Erroneous Erase Fail Flag Operation: Command reissue clarified. t_{PLQZ} Specification: Changed to reflect B-step improvements. V_{PP} Low Flag: Title changed from "False V_{PP} Low Flag Operation" to "V_{PP} Low Flag Operation." Separated into 2 parts: False V_{PP} Low Flag Operation and No V_{PP} Flag Operation. TTL-Level Control Signals: Changed to reflect B-step fix. t_{WHEH} /Address Timing: Changed to reflect B-step fix New erratum: t_{WHWL}/ t_{EHEL} for third Write Erratum added. New addenda: Input Slew Rate and Capacitance Specs added. New datasheet clarification: V_{CC} Ramp Time added. New erratum: Extended Temp Cold Program added.

REVISION HISTORY, Continued

Date of Revision	Version	Description
08/22/95	-008	Identification criteria for A-Step sample, A-Step Prod, and B-step changed to use top-side FPO mark for easier access and better accuracy. Max Erase Time Addendum added. Low-Voltage Erase Time Erratum added.
05/01/96	-009	This document has been converted to the new Specification Update format. Errata on extremely early -BR/CR sample material has been removed from this errata listing. This material was never put into production. The two errata removed were: "Limited V_{CC} supply Voltage" and "Reduced V_{LKO} (Commercial Temp)." Access Time Erratum, which was previously removed in revision -005, has dropped from this revision. V_{CC} Ramp Time (Datasheet Clarification) rewritten. Automotive V_{LKO} Spec Change removed, incorporated into datasheet.
06/11/96	-010	New Erratum: BE/CE 5V Extended Temperature Limitation C-step and D-step information added to: t_{PHWL}/t_{PHEL} Pushout (new spec values, status) Third-Write Pulse (affected prod) Ext Temp Programming Limitations (Status, affected products) Low-Voltage Erase Time/Current Erratum (status, affected prod) Spec Changes: I_{OH}/I_{OL} Spec Change in 2.7V and 3.3V Ranges (new) Documentation Changes: Datasheet Erratum - WP# Description (new) Max Byte/Word Program Time Specifications (new)
7/26/96	-011	BE/CE 5V Extended Temperature Limitation erratum modified to include BV/CV products.
12/6/96	-012	E-step information added to: Errata - t_{PHWL}/t_{PHEL} Pushout (new spec values) Errata - Third-Write Pulse (affected prod) Spec Changes - 001 thru 003 Spec Clarifications - 001 New Spec Change: t_{EHQZ} and t_{GHQZ} specs improved.
2/3/97	-013	Errata - t_{PHWL}/t_{PHEL} Pushout (new C & D-step spec values 2 µs to 8 µs) New Spec Change : Removal of Max Byte/Word Write Specification.

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the thirteenth release of the 28F400BV/CV/CE and 28F004BV/BE Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published. Functional descriptions for this product are found in the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet*.

Affected Documents/Related Documents

Title	Order
4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet	290530

Nomenclature

Errata are design defects or errors. These may cause the 28F400BV/CV/CE and 28F004BV/BEs' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet.* Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings					Page	Status	Errata
	A	B	C	D	E			
1	X					9	Fixed	No prog/erase when V_{CC} = 3V, V_{PP} = 12V.
2	X	X	X	X	X	10	NoFix	t_{PHWL}/t_{PHEL} out of spec at 3V. B, C & D-step fixed at 5V. E-Step pushes out to 25 µs and 2.7V added for all steps.
3	X					11	Fixed	Must wait 100 ns after reset before read.
4	X					12	Fixed	Erase status flag may erroneously indicate fail.
5	X					13	Fixed	Erase resume fail may falsely indicate V_{PP}-low.
6	X					14	Fixed	A-step production has V_{PP}-low flag disabled.
7	X					15	Fixed	TTL-levels require V_{IHMIN} = 4.0V on control pins.
8	X					16	Fixed	Write or address timing changes for A-step.
9	X	X	X	X	X	20	NoFix	t_{WHWL}/t_{EHEL} out of spec after 2-write sequence.
10	X	X				22	Fixed	Ext temp, V_{CC} = 3.3V ± 0.3V must program within T = 0°C – +85°C.
11		X				22	Fixed	Erase time and current may increase when V_{CC} = 3.3V ± 0.3V, V_{PP} = 5V ± 10%.
12				X		23	Fixed	Early D-step ext temp BE/CE/BV/CV material limited to 0°C–85°C when using V_{CC} = 5V.

Specification Changes

Number	Steppings					Page	Status	Specification Changes
	A	B	C	D	E			
1	X	X	X	X	X	25	Perm	New t_{PLPH} spec defined with values for A-, B-step.
2	X	X	X	X	X	26	Perm	New t_{PLQZ} spec defined with values for A-, B-step.
3	X	X	X	X	X	27	Perm	I_{OH}/I_{OL} Spec Change in 2.7V and 3.3V Ranges.
4		X	X	X	X	28	Perm	t_{EHQZ} and t_{GHQZ} specs improved.

Specification Clarifications

Number	Steppings					Page	Status	Specification Clarifications
	A	B	C	D	E			
1	X	X	X	X	X	29	Doc	Clarifies V_{CC} ramp rate requirements.

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
1	-001	30	Doc	Input rise/fall times added to datasheet.
2	-001	30	Doc	Input/output capacitance specs added.
3	-001	31	Doc	Max block erase times added to datasheet.
4	-002/-003	31	Doc	Editing mistake in Revisions -002/-003 of datasheet.
5	-003	32	Doc	Removal of Maximum Byte/Word Program time specifications

IDENTIFICATION INFORMATION

Markings

Stepping	Identifier
A-Step Engineering Sample	1. “ES” on topside mark. 2. No ninth digit on topside FPO mark.
A-Step Production	1. Ninth digit of topside FPO mark = “A” or “F” or “C”
B-Step Production	1. Ninth digit of topside FPO mark = “D” or “E”
C-Step Production	1. Ninth digit of topside FPO mark = “G” or “Q”
D-Step Production	1. Ninth digit of topside FPO mark = “J” or “T”
E-Step Production	1. Ninth digit of topside FPO mark = “Y”

NOTE:
C-Step and D-step production material reflect the same schematic revision level

ERRATA

1. 3.3V V_{CC}/12V V_{PP} Program/Erase Limitation

PROBLEM: Affected material will not program and erase consistently using V_{CC} = 3.3 ± 0.3V and V_{PP} = 12V ± 5%. This is limited to a few groups of early A-step material. All other voltage combinations are not affected. The affected modes are summarized in the table below.

V_{CC}	V_{PP}	Read Operation	Program Operation	Erase Operation
3.3 ± 0.3V	5.0V ± 10%	√	√	√
5.0V ± 10%	5.0V ± 10%	√	√	√
3.3 ± 0.3V	12V ± 5%	√	NO	NO
5.0V ± 10%	12V ± 5%	√	√	√

NOTE:
√ = mode functional.

IMPLICATION: Applications using V_{CC} = 3.3 ± 0.3V and V_{PP} = 12V ± 5% will not be able to program or erase using these voltage ranges.

WORKAROUND: For affected material, if using 3.3V V_{CC}, use V_{PP} = 5V instead of V_{PP} = 12V. In a PROM programmer (5V V_{CC}), use 5V or 12V programming.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: Early A-step material using V_{CC} = 3.3 ± 0.3V and V_{PP} = 12V ± 5% is affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
TE28F004BV-T/B, TB28F400BV-T/B, TE28F400CV-T/B, TE28F400BV-T/B,	All	A	Third line of top mark equals T4410002C, T4430001, T4430002, T4430003, T4440003, T4440004, T444005Q, T444020	3.3 ± 0.3V	12V ± 5%	All

2. t_{PHWL}/t_{PHEL} Pushout

PROBLEM: Affected material does not meet its t_{PHWL}/t_{PHEL} specification for write operations in 2.7V, 3.3V and 5V V_{CC} operations. This problem has been improved in the B, C and D-step versions of the product so that it meets specification at 5V, but the parameter does not meet its specification in 2.7V and 3.3V operations. The spec in 2.7V and 3.3V operations has been further pushed-out on the E-stepping. The erratum specifications are below:

Specification	V_{CC} = 3.3 ± 0.3V V_{CC} = 2.7V–3.6V	V_{CC} = 5V ± 10%	Units
t_{PHWL}/t_{PHEL}(Datasheet)	0.8	0.45	µs
t_{PHWL}/t_{PHEL}(A-step Erratum)	8	6	µs
t_{PHWL}/t_{PHEL}(B-step Erratum)	8	meets spec	µs
t_{PHWL}/t_{PHEL}(C-, D-step Erratum)	8	meets spec	µs
t_{PHWL}/t_{PHEL}(E-step Erratum)	25	meets spec	µs

The specification t_{PHWL} (RP# High Recovery to WE# Going Low) is the minimum time between the RP# signal going high to WE# going low. The specification t_{PHEL} (RP# High Recovery to CE# Going Low) is the minimum time between the RP# signal going high to CE# going low.

IMPLICATION: The erratum affects the delay from coming out of a reset until a command write can be executed on the part (affects both WE#-controlled and CE#-controlled command sequences). Although the read specification t_{PHQV} (RP# going high to data valid) Is less than the t_{PHWL}/t_{PHEL} errata, the full time for t_{PHWL}/t_{PHEL} must be completed prior to WE# going low.

WORKAROUND: Verify system timings to ensure this does not impact your design.

STATUS: This erratum has been improved from the A-step to the B-, C- and D-steps. The errata has been pushed-out further on the E-stepping. It now meets specification when operating at 5V, but does not meet specification for 2.7V and 3V operations. No fix or further improvement is planned. Refer to Summary Table of Changes to determine the affected steppings.

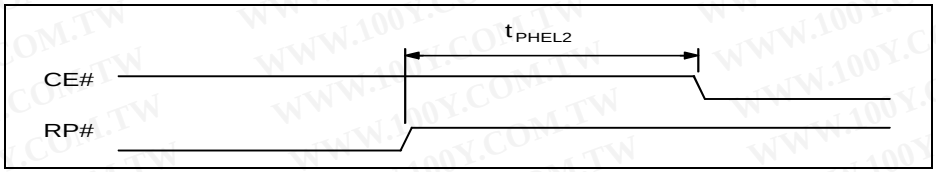
AFFECTED PRODUCTS: This erratum applies to all A-, B-, C-, D- and E-step material with some improvements depending on the stepping.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV/BE, TB28F400BV-T/B, TE28400CV/CE, TE28F400BV-T/B, TE28F400BR-T/B, AB28F400BR-T/B	All	A B C D E	No ninth digit on topside FPO mark or Ninth digit of topside FPO mark = one of: A, F, C, D, E, G, Q, J, T or Y	All	All	All

3. CE# Delay from RP# High

PROBLEM: Affected material requires a delay between coming out of reset (RP# signal going high) and beginning a read operation (CE# going low). This minimum specification must be followed to ensure valid data is read during subsequent read operations.

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PHEL2}	100	100	ns



Timing Diagram for Required Delay

IMPLICATION: Applications that do not meet the required delay may read invalid data from the device.

WORKAROUND: This timing must be followed for A-step material, but not for B-step material. Verify system timings to ensure this does not impact your design.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A-step engineering samples and production materials are affected. B-step has been fixed.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	No ninth digit on topside FPO mark **or** ninth digit of topside FPO mark = "A" or "F" or "C"	All	All	All

4. *Erroneous Erase Fail Flag Operation*

PROBLEM: Due to a logic timing problem, affected units may indicate a block erase error in the Status Register when, in fact, proper block erasure has occurred. The relevant bit of the Status Register is SR.5 (Erase Status), which is shaded on the diagram below. Normally, SR.5 = 1 indicates an error in block erasure, and SR.5 = 0 indicates successful block erase. If SR.5 = 0 following an erase operation, the erase operation was completed successfully. If SR.5 = 1 following an erase operation, the bit was most likely set incorrectly due to the logic timing problem.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTE:
Please see Section 3.3.2 of the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* for more information on Status Register operation.

IMPLICATION: Applications using the Status Register to verify successful erase will have erase failures that will affect operation.

WORKAROUND: The erase status flag (SR.5) should be ignored by masking this bit in your software. To confirm a successful block erase, read back the contents of a block to verify that all bytes contain FFH (all bits in block equal 1). Alternatively, reissue the Block Erase command until a successful erase is reported in the Status Register. Because of these limitations, block cycling for affected material should be limited to 10,000 cycles for both commercial and extended temperature ranges. Reissuing the Erase command upon an error bit counts as another block erase cycle.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A-step engineering samples and production materials are affected. B-step has been fixed.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	No ninth digit on topside FPO mark **or** Ninth digit of topside FPO mark = "A" or "F" or "C"	All	All	All

5. *False V_{PP}-Low Flag Operation When Returning from Erase Suspend*

PROBLEM: Only applications using erase suspend mode are affected. If using erase suspend mode, the following problem may be encountered: When resuming erase from erase suspend mode, the device may abort the erase procedure as a result of a logic timing problem. When this happens, the Status Register will indicate an erase failure (SR.5 = 1) and the V_{PP} status bit will indicate that V_{PP} voltage was not within specification (SR.3 = 1), even if V_{PP} is within tolerances.

The relevant bit of the Status Register is SR.3 (V_{PP} Status), which is shaded on the diagram below. Normally, SR.3 = 1 indicates an aborted operation due to V_{PP} not being switched on.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTE:
Please see Section 3.3.2 of the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* for more information on Status Register operation.

IMPLICATION: Applications using the erase suspend features may intermittently experience failures resuming erase from suspend mode. Data in the block being erased when suspend mode was entered will be corrupted by the partial erasure. Data in other blocks is not affected.

WORKAROUND: If a system design is experiencing program/erase failures under the conditions described above, issue another Erase command to complete a successful block erase.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A-step ES materials using erase suspend mode are affected. B-step has been fixed.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	"ES" on topside mark **and** No ninth digit on topside FPO mark	All	All	All

6. *Disabled V_{PP}-Low Flag*

PROBLEM: The VPPS flag in the Status Register (SR.3) has been disabled in affected products. Normally, when the VPPS flag is operational, a program or erase command initiated with V_{PP} not in range (V_{PPH1} or V_{PPH2}) will result in the erase status bit (ES = SR.5) or program status bit (DWS = SR.4) being set to "1" along with the V_{PP} status bit (VPPS = SR.3) to indicate a failed operation due to low V_{PP}. However, under this erratum, if a program or erase command is initiated with V_{PP} not in range (V_{PPH1} or V_{PPH2}), then the erase status bit (ES = SR.5) or program status bit (DWS = SR.4) will be set to "1" to indicate program or erase failure, but the V_{PP} status bit (VPPS = SR.3) will remain at "0," since the VPPS flag has been disabled.

Basically, the part will operate normally, but will not indicate when low V_{PP} is the cause of a failed program or erase operation.

The relevant bit of the Status Register is SR.3 (V_{PP} Status), which is shaded on the diagram below. Normally, SR.3 = 1 indicates an aborted operation due to V_{PP} not being switched on.

WSMS	ESS	ES	DWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

NOTE:
Please see Section 3.3.2 of the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* for more information on Status Register operation.

IMPLICATION: When an erase or program failure is experienced, the device will not indicate if low V_{PP} was the cause of the failure.

WORKAROUND: If a system design is experiencing program/erase failures under the conditions described above, issue another Erase command to complete a successful block erase. System design using the VPPS flag to detect program or erase errors should use the program and erase status bits instead.

STATUS: This erratum has been fixed in the B-step. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: This erratum applies to all A-step production material. B-step has been fixed.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	Ninth digit of topside FPO mark = “A” or “F” or “C”	All	All	All

7. TTL-Level Control Signals

PROBLEM: This erratum applies only to systems using TTL signal levels and V_{CC} = 5V ± 10%. If you are using CMOS inputs, this erratum does not affect your design. Due to an internal detector problem, TTL logic high level must be minimum 4.0V (instead of 2.4V) on the control pins of the device: CE#, OE#, and WE#. Standard TTL levels can continue to be used on other pins on the device. The required logic-high level is defined in the table below:

Parameter	Min	Max	Units
Input High Voltage (TTL)	4.0	V_{CC} + 0.2V	V

IMPLICATION: Applications using TTL levels will need to modify their designs to meet the higher input voltage requirements on the control signals.

WORKAROUND: This requirement must be met for proper operation of the device.

STATUS: This erratum has been fixed in B-step material. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A-step engineering samples and production material using TTL signal levels and operating at V_{CC} = 5V ± 10% are affected. B-step material has been fixed.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	No ninth digit on topside FPO mark **or** Ninth digit of topside FPO mark = "A" or "F" or "C"	5V ± 10% (TTL Levels)	All	All

8. *Write Timing Erratum/Address Timing Erratum*

PROBLEM: Due to logic timing problems, modifications in write or address timing are required. Two possible workarounds exist: errata A and B. Refer to the following table to determine the operating which applies to your operation conditions. Where the table says, "One of A or B," one of either erratum A **or** B is necessary for proper functionality. Where it says, "A," only erratum A is needed. "Not Affected" means that this erratum does not effect that operation condition.

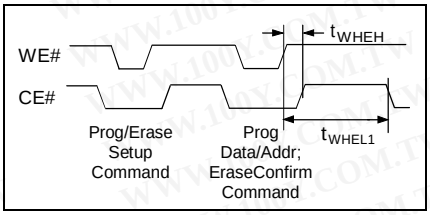
	x8-Mode Operation		x16-Mode Operation	
	V_{PP} = 5V ± 10%	**V_{PP} = 12V ± 5%**	**V_{PP} = 5V ± 10%**	**V_{PP} = 12V ± 5%**
V_{CC} = 3.3 ± 0.3V	One of A or B	A	Not Affected	A
V_{CC} = 5V ± 10%	One of A or B	One of A or B	Not Affected	Not Affected

IMPLICATION: Applications operating in an affected mode must implement the applicable workaround for proper operation.

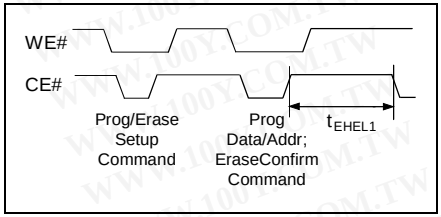
WORKAROUND:

A. t_{WHEH}- CE# Timing Erratum

Due to a logic timing problem, new timing restrictions may be necessary between the WE# and CE# signals during write operations. The timing waveforms and specifications are shown below:



Timing Waveform for WE#-Controlled Writes



Timing Waveform for CE#-Controlled Writes

Affected Parameters for WE#-Controlled Writes

Symbol	Parameter	Datasheet		Errata		Units
		Min	Max	Min	Max	
t_{WHEH}	CE# Hold Time from WE# High	0	no spec	0	5	ns
t_{WHEL1}	CE# Pulse Width High from WE# High	no spec	no spec	110		ns

NOTE:
Erratum timing for t_{WHEL1}, given above, is required only after the second WE# pulse in a WE# controlled write sequence.

Basically, these new errata specifications for WE#-controlled writes require the system timing to:

1. Take CE# to logic high no earlier than WE# goes high and no later than 5 ns after WE# goes high.
2. Hold CE# high for at least 110 ns, starting from the time WE# goes high.

Affected Parameters for CE#-Controlled Writes

Symbol	Parameter	Datasheet		Errata		Units
		Min	Max	Min	Max	
t_{EHEL1}	CE# Pulse Width High from WE# or CE# High, whichever occurs last	20	no spec	110		ns

NOTE:
The erratum timing for t_{EHEL1}, given above, is required only after the second CE# pulse in a CE# controlled write sequence.

A system can also use the alternative CE#-controlled writes with the specifications given in the datasheet with the addition of t_{EHEL1}, which must have a pulse width of 110 ns, as shown above.

These timing specifications must be met for proper operation of the device. The flash memory chip select must go inactive within 5 ns of a program/erase operation and remain inactive for a period of 110 ns before going active again. Consider the following options for meeting the t_{WHEL1} or t_{EHEL1} requirement:

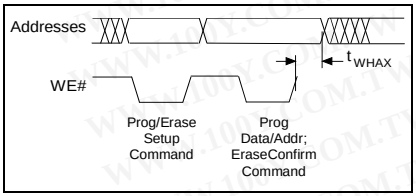
1. Follow a program/erase two-write sequence with an access to another memory so as not to decode the flash memory chip select for the required period of time.
2. Insert one or more no-op commands following a program/erase two-write sequence, again to ensure the flash memory chip select is disabled for the required period of time.

Depending on your system implementation, the t_{WHEH} requirement may require additional logic to ensure the required t_{WHEH} timing. Evaluate your system timing to ensure the new write requirements can be met. This erratum has been fixed in B-step material.

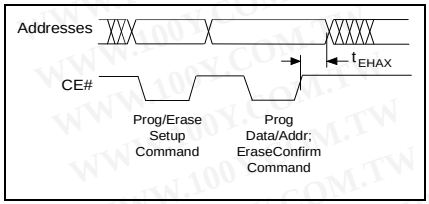
B. Address Timing Erratum

Due to a logic timing problem, new timing restrictions may be necessary on the lowest order address pin. This pin is the A_{-1} address pin for 28F400 products in x8-mode and the A_{10} address pin for 28F004 x8-only products. The timing waveforms and specifications follow:

Product	Affected Pin
28F400	A_{-1} (in x8 mode)
28F004	A_{10}



Timing Waveform for WE#-Controlled Writes



Timing Waveform for CE#-Controlled Writes

Affected Parameters for WE#-Controlled Writes

Symbol	Parameter	Datasheet		Erratum		Unit
		Min	Max	Min	Max	
t_{WHAX}	Address Hold Time from WE# High (unaffected pins)	10				ns
	Address Hold Time from WE# High (affected pin: A_{-1} for 28F400 in x8, A_{10} for 28F004)	10		40		ns

Affected Parameters for CE#-Controlled Writes

Symbol	Parameter	Datasheet		Erratum		Unit
		Min	Max	Min	Max	
t_{EHAX}	Address Hold Time from CE# High (unaffected pins)	10				ns
	Address Hold Time from CE# High (affected pin: A_{-1} for 28F400 in x8, A_{10} for 28F004)	10		40		ns

This new erratum specification requires the system timing in x8-mode to hold the affected address pin valid for 40 ns from the time WE# goes high (for WE#-controlled writes) or from the time CE# goes high (for CE#-controlled writes).

These timing specifications must be met for proper operation of the device. Additional logic may be needed to meet these requirements.

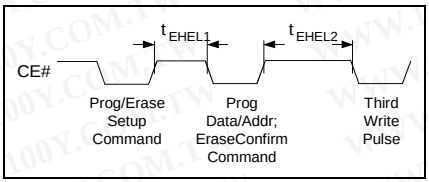
STATUS: This erratum has been fixed in B-step material. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A-step material is affected depending on operating mode (see table below). B-step material has been fixed.

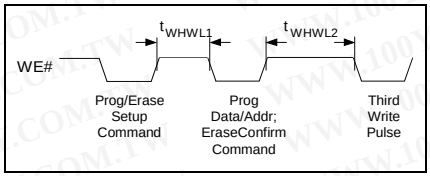
These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	All	A	No ninth digit on topside FPO mark **or** Ninth digit of topside FPO mark = "A" or "F" or "C"	All	All	All

9. Third Write-Pulse t_{WHWL}/t_{EHEL} Specification Erratum

PROBLEM: This erratum affects designs issuing program or erase commands to the flash device with V_{CC} = 2.7V–3.6V or 3.3 ± 0.3V. Operation with V_{CC} = 5V ± 10% is not affected. Program and erase functions are initiated using a two-write sequence, with the Program or Erase Setup command being written to the part, then the data program or erase confirm being written on the next cycle after a time t_{WHWL1} (t_{EHEL1} for CE#-controlled writes) between the write low pulses. Following the second write in a two-write sequence; the WE# (CE#) signal must stay high for 35 ns before going low again for a third write pulse, shown as the t_{WHWL2} (t_{EHEL2}) on the right in the below. The value of t_{WHWL1} (t_{EHEL1}) between the first and second write in the sequence remains at its datasheet specification. The specified and erratum values are shown in the table which follows.



Timing Waveform Showing Two t_{WHWL} Specifications



Timing Waveform Showing Two t_{EHEL} Specifications

Parameter	Product	BV–60		BV–80/BV–120		Units
	V_{CC}	2.7V–3.6V or 3.3 ± 0.3V				
	Load	50 pF				
		Spec	Errata	Spec	Errata	
t_{WHWL2} (min, third write only)		20	40	30	40	ns
t_{EHEL2} (min, third write only)		20	40	30	40	ns

IMPLICATION: Violating the errata conditions described in this erratum can cause the Write State Machine to abort the program or erase operation in progress and report a successfully completed operation in the Status Register, although in reality, the operation has not completed successfully.

WORKAROUND: Note, however, that even without this erratum, it is not useful for the system to write to the flash device after a program sequence until the Status Register reports that the program operation has completed, since the State Machine is designed to ignore all instructions while a program operation is in progress. Writing the Status Register Read command to the device is not necessary since the device defaults to outputting Status Register data while the program operation is in progress. In the case of an erase operation, the only valid command that should be written to the device while an erase operation is in progress is the Erase Suspend command. In this situation, the system must wait for the erratum value of t_{WHWL2} (t_{EHEL2}) before requesting an Erase Suspend.

STATUS: This is a permanent change. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All A-, B-, C- and D-step materials are affected when using V_{CC} = 3.3 ± 0.3V or 2.7V–3.6V.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV/BE, TB28F400BV-T/B, TE28400CV/CE, TE28F400BV-T/B	All	A B C D E	No ninth digit on topside FPO mark **or** ninth digit of topside FPO mark = one of: A, F, C, D, E, G, Q, J, T or Y	2.7V–3.6V **or** 3.3 ± 0.3V	All	All

10. Extended Temperature Programming Limitations

PROBLEM: Affected material has the following limitations on operating parameters:

Parameter	Min	Max	Unit
Extended Temperature Range (Program only)	0	+85	°C

Because on-chip program circuitry is sensitive to very low temp operation, this material must be programmed within the temperature range of 0°C to +85°C. Read and erase operation is unaffected over the full extended temperature operating range (–40°C to +85°C).

IMPLICATION: This erratum limits the temperature range over which affected material can be programmed.

WORKAROUND: Contact your Intel representative for workaround information.

STATUS: This errata has been fixed on the C- and D-steppings. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: All A- and B-step materials are affected when using V_{CC} = 3.3 ± 0.3V and programming over T = –40°C to 0°C. Products using commercial temperature, or not programming over this temperature range are not affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B	All	A B	No ninth digit on topside FPO mark **or** Ninth digit of topside FPO mark = one of: A, F, C, D, or E	3.3 ± 0.3V	All	-40°C to 0°C

11. Low-Voltage Erase Time/Current Erratum

PROBLEM: Block erase times for affected material may intermittently exceed erase time and I_{PPE} current specifications when operating with V_{CC} = 3.3 ± 0.3V and V_{PP} = 5V ± 10% over specified cycling limits. Typical erase times are not affected. The increased erase time and I_{PPE} erase current only occur together and do not occur independently of each other. The errata erase times and currents are indicated between the thickened lines, in the tables which follow.

Errata Erase Times (V_{CC} = 3.3 ± 0.3V, V_{PP} = 5V ± 10%

Parameter	DS Spec	Errata	Unit
Maximum Block Erase Time (Boot/Parameter)	7	20	s
Maximum Block Erase Time (Main)	14	20	s

Errata I_{PPE} Specification (V_{CC} = 3.3 ± 0.3V, V_{PP} = 5V ± 10%

Parameter	DS Spec	Errata	Unit
I_{PPE} (max, during errata occurrence only)	30	40	mA

IMPLICATION: Applications operating under the affected conditions may intermittently see longer than normal erase times, accompanied by increased erase current.

WORKAROUND: Ensure that system operation is not affected by errata parameters.

STATUS: This errata has been fixed on later B-step (ninth digit = "E") and C-/D-step parts. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS: Early B-, C-, and D-step material is affected when erasing at V_{CC} = 3.3 ± 0.3V and V_{PP} = 5V ± 10%.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
E28F004BV-T/B, PA28F400BV-T/B, E28F400CV-T/B, E28F400BV-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B	All	Early B or C or D	Ninth digit of topside FPO mark = "D" or "G" or "J" is affected. "E," "Q," and "T" materials are fixed.	3.3 ± 0.3V	5V ± 10%	All

NOTE:
Designs not using B-step material or the 3V V_{CC} / 5V V_{PP} voltage combination are not affected. All B-step units of the listed products that meet the application and marking criteria are affected. A-step is not affected.

12. BE/CE/BV/CV 5V V_{cc} Extended Temperature Limitation

PROBLEM

The operating temperature for affected material is limited to 0°C - +85°C when using V_{CC} = 5V ± 10%. This is detailed in the table below.

Parameter	Min	Max	Unit
Extended Temperature Range (V_{CC} = 5V ± 10% or 5V ± 5%)	0	+85	°C

When using 5V V_{CC}, the chip must be operated within the temperature range of 0°C to +85°C. Low voltage operation (3.3±0.3V or 2.7-3.6V) is unaffected and can be used over the full extended temperature operating range (–40°C to +85°C). Note that if the flash pin CE# is permanently tied low (enabled), then this erratum does not apply.

IMPLICATION

This erratum limits the temperature range over which affected material can be used at 5V V_{CC}.

WORKAROUND

Ensure the erratum temperature requirements are not violated when using 5V V_{CC}. Contact your Intel representative for additional workaround options.

STATUS

This erratum has been modified to include -BV/CV suffix products as well as the -BE/CE products originally covered. This erratum has been fixed in new production material. However, shipments of affected products may contain fixed and unfixed material through October 1996. Fixed material can be identified a “T” in the ninth digit of the topside FPO mark. Refer to Summary Table of Changes to determine the affected stepping.

AFFECTED PRODUCTS

Only initial limited production D-Step -BE/CE/BV/CV material (identified by a “J” in the ninth digit of the topside FPO mark) is affected by this erratum when operating at 5V V_{CC}. All A-, B-, C-, and later D-step materials (ninth digit = “T”) are **unaffected**. Applications not using 5V V_{CC} or sub –0°C temperatures are not affected.

These products are affected. . .				. . .under these operating conditions		
Name	**Package**	**Step**	**Marking**	**V_{CC}**	**V_{PP}**	**Temp**
TE28F004BE-T/B, TB28F400CE-T/B, TE28F004BV-T/B, TB28F400BV-T/B, TE28400CV-T/B, TE28F400BV-T/B, AB28F400BR-T/B	40-TSOP 44-PSOP 48-TSOP 56-TSOP	D	Ninth digit of topside FPO mark = “J“	5V ± 5% 5V ± 10%	All	-40°C to 0°C

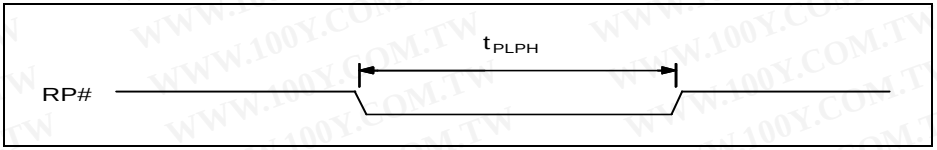
SPECIFICATION CHANGES

1. New t_{PLPH} Specification Definition and Values

PROBLEM: This item defines a new specification that will be added to the datasheet. This specification is t_{PLPH} and is defined as the minimum time that RP# must be held low in order to produce a valid reset of the device.

The first data row of the table below lists t_{PLPH} values for A-step material and the second data row lists t_{PLPH} values for B-step material.

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PLPH} (Reset Pulse Width) **A-Step**	250	250	ns
t_{PLPH} (Reset Pulse Width) **B-, C-, D-, E-Step**	150	60	ns



Timing Diagram for t_{PLPH} Specification

IMPLICATION: Systems that are not asserting the reset signal low longer than t_{PLPH} may not be properly resetting the flash component.

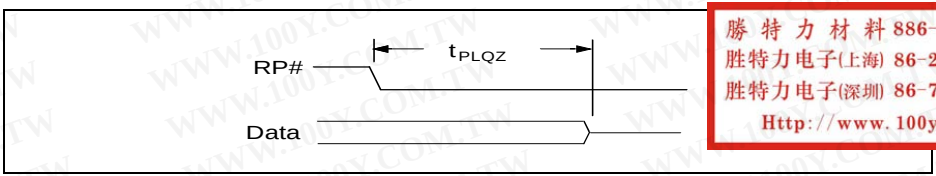
AFFECTED PRODUCTS: While both A-step and B-step materials are affected, note that the parameter values for t_{PLPH} are different between A-step and B-step. Reference the identification information for clarification on distinguishing between steppings.

2. *New t_{PLQZ} Specification Definition and Values*

PROBLEM: This item defines a new specification that will be added to the datasheet. This specification is t_{PLQZ} and is defined as the maximum time after RP# goes to logic low until the flash data pins go to high-impedance state. The first data row of the table below lists t_{PLQZ} values for A-step material and the second data row lists t_{PLQZ} values for B-step material. (typical output loads)

AC Characteristics: Read Only Operations

Specification	V_{CC} = 3.3 ± 0.3V	V_{CC} = 5V ± 10%	Units
t_{PLQZ} (RP# Low to Output High Z) **A-Step**	250	250	ns
t_{PLQZ} (RP# Low to Output High Z) **B-, C-, D-, E-Step**	150	60	ns



Timing Diagram for t_{PLQZ} Specification

IMPLICATION: Because the flash requires a time t_{PLQZ} after reset goes low until the data pins go to high-impedance, systems that do not meet this specification may have problems with bus contention.

AFFECTED PRODUCTS: While both A-step and B-step material are affected, note that the parameter values for t_{PLQZ} are different between A-step and B-step. Reference the identification information for clarification on distinguishing between steppings.

3. I_{OH}/I_{OL} Spec Change in 2.7V and 3.3V Ranges

PROBLEM: The output current specs I_{OH}/I_{OL} are being changed from their datasheet specifications. I_{OH}/I_{OL} are specified in the test conditions column of the V_{OL}, V_{OH1}, and V_{OH2} rows of the DC Characteristics table. The table below details the changes made to the DC Characteristics table of the datasheet.

	Sym	Parameter	V_{CC} 3.3 ± 0.3V 2.7V–3.6V		Unit	Test Conditions
			Min	Max		
Before	V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = V_{CC}Min$, I_{OL} = 5.8 mA
After	V_{OL}	Output Low Voltage		0.45	V	$V_{CC} = V_{CC}Min$, **I_{OL} = 2.0 mA**
Before	V_{OH1}	Output High Voltage (TTL)	2.4		V	$V_{CC} = V_{CC}Min$, I_{OH} = –2.5 mA
After	V_{OH1}	Output High Voltage (TTL)	2.4		V	$V_{CC} = V_{CC}Min$, **I_{OH} = –2.0 mA**
Before	V_{OH2}	Output High Voltage (CMOS)	0.85 × V_{CC}		V	$V_{CC} = V_{CC}Min$, I_{OH} = –2.5 mA
After	V_{OH2}	Output High Voltage (CMOS)	0.85 × V_{CC}		V	$V_{CC} = V_{CC}Min$, **I_{OH} = –2.0 mA**

IMPLICATION: This change can impact the number of devices that can be driven from the outputs of the flash memory (reduced fan out) due the reduced output current specs.

AFFECTED PRODUCTS: This specification is applicable to all products covered by this document.

4. t_{EHQZ} and t_{GHQZ} Specification Improvement

PROBLEM: This item improves the specifications t_{EHQZ} and t_{GHQZ}, which define how long the flash takes to get off the bus after the outputs are disabled. t_{EHQZ} specifies the latency between when CE# goes high to when the flash output drivers go to high-impedance. t_{GHQZ} specifies the latency between when OE# goes high to when the flash output drivers go to High-Z. The following table defines the new spec values, which will be included in the *1997 Flash Memory Databook*.

Read Specification Improvement: Commercial and Extended Temperature

Parameter	V_{CC}	2.7V-3.6V or 3.3 ± 0.3V	5V ± 5% or 5V ± 10%	Unit
		New Spec	New Spec	
t_{EHQZ} (CE# High to Output High-Z)		25	20	ns
t_{GHQZ} (OE# High to Output High-Z)		25	20	ns

IMPLICATION: This spec improvement can eliminate the need for a bus transceiver in higher frequency designs, depending on the specific processor-memory interface.

AFFECTED PRODUCTS: This improvement applies to all speeds of the 28F004/400BV/CV/BE/CE products at both commercial and extended temperature.

SPECIFICATION CLARIFICATIONS

1. V_{CC} Ramp Time Clarification

PROBLEM: The *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* (Order 290530-001 and 290530-002, Sections 5.1 and 6.1) specifies timings for V_{CC} voltage switching. As defined in these datasheet revisions, these timing specs, t_{5VPH} and t_{3VPH}, require RP# to be held low during a V_{CC} ramp until 2 µs after V_{CC} has stabilized above its minimum voltage specification. Because this requirement may be difficult to meet in a system design, this datasheet clarification defines new guidelines for V_{CC} ramp-up and changes. Basically, the specs require a delay of 2 µs only when the V_{CC} ramps at a rate faster than 1V/100 µs, and define the delay as the time between V_{CC} reaching V_{CCMIN} and the first device operation. These specs are no longer tied to the operation of the RP# pin. However, RP# = GND during power-up is still recommended to protect against spurious write signals between V_{LKO} and V_{CCMIN}. The new requirement is summarized in the table below:

V_{CC} Ramp Rate	Required Timing
≤ 1V/100 µs	No delay required.
> 1V/100 µs	A delay time of 2 µs is required before any device operation is initiated, including read operations, command writes, program operations, and erase operations. The delayis measured beginning from the time V_{CC} reaches V_{CCMIN} (3.0V for 3.3V operation and 4.5V for 5V operation).

NOTE:

1. These requirements must be strictly followed to guarantee all other read and write specifications.
2. To switch between 3.3V and 5.0V operation, the system should first transition V_{CC} from the existing voltage range to GND, and then to the new voltage. Any time the V_{CC} supply drops below V_{LKO}, the chip will be reset, aborting any operations pending or in progress.
3. These guidelines must be followed for any V_{CC} transition from GND.

DOCUMENTATION CHANGES

1. Input Slew Rate

ITEM: Two figure notes were inadvertently left out of the initial release of the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* (order 290530-001) for the affected products. The notes describe test conditions and specify that input signal rise and fall times (from 10% to 90%) must be less than 10 ns. The table below contains the missing notes and to which figure numbers they apply. Please evaluate possible impact on system designs. These notes have been added to the next revision of the datasheet.

Figure Number	Text of Missing Note
13, 23	AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic 1 and V_{OL} (0.45 V_{TTL}) for a logic 0. Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10 ns.
15, 25	AC test inputs are driven at 3.0V for a logic 1 and 0.0V for a logic 0. Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) <10 ns.

2. Capacitance Specifications

ITEM: This addendum adds the capacitance values in the table below to the datasheets for the affected material. Please evaluate possible impact on system designs. These notes will be added to the next revision of the datasheet.

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	10	12	pF	V_{OUT} = 0V

NOTE:
Sampled, not 100% tested.

3. Maximum Erase Time Specifications

ITEM: This addendum adds the maximum erase time values in the table below to the datasheets for the affected material. Previously, only typical numbers were given in the datasheet. This information will be added to the next revision of the datasheet.

Block Erase Timings (Commercial and Extended Temperature)

	V_{PP}	5V ± 10%				12V ± 5%				
	V_{CC}	3.3 ± 0.3V		5V ± 10%		3.3 ± 0.3V		5V ± 10%		
Parameter		**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Boot/Parameter Block Erase Time		0.84	7	0.8	7	0.44	7	0.34	7	s
Main Block Erase Time		2.4	14	1.9	14	1.3	14	1.1	14	s

NOTES:

1. Max erase times are specified under worst case conditions. The max erase times are tested at the same value independent of V_{CC} and V_{PP}. See Note 2 for typical conditions.
2. Typical conditions are +25°C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0V, V_{PP} = 12.0V typically results in a 60% reduction in programming time.

4. Datasheet Erratum (WP# Description)

ITEM: Revisions -002 and -003 of the *4-Mbit (256K x 16, 512K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet* contain an editing error in the pin description for the WP# pin (Section 1.5, Table 2). The error is in the last "NOTE" paragraph of that description. The sentence, "This pin is not available on the 44-lead PSOP package," is not applicable to the 4-Meg product and should not be there. (This was an accidental carry-over from the *8-Mbit (512K x 16,1024K x 8) SmartVoltage Boot Block Flash Memory Family Datasheet.*) The corrected paragraph will read: "**NOTE:** This feature is overridden and the boot block unlocked when RP# is at V_{HH}. See Section 3.4 for details on write protection."

This erratum will be corrected in the next revision of the datasheet.

5. *Removal of Maximum Byte/Word Program Time Specifications*

ITEM: In the previous revision of this Specification Update (297595-012), this addendum was included to add the maximum programming times for byte/word writes. It was stated that this addendum would be added to the datasheets for the affected product. Since that publication, it has been determined that further testing is required before this parameter can be guaranteed. It is recommended that this specification not be used when designing your application. When more information becomes available, it will be published in future Specification Updates and datasheets.

Program Timings (Commercial and Extended Temperature)

Parameter	5V ± 10%						12V ± 5%						Unit
	2.7V–3.6V		3.3 ± 0.3V		5V ± 10%		2.7V–3.6V		3.3 ± 0.3V		5V ± 10%		
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Byte Program Time	11	note 3	10	note 3	10	note 3	8.8	note 3	8	note 3	8	note 3	µs
Word Program Time	14.3	note 3	13	note 3	13	note 3	8.8	note 3	8	note 3	8	note 3	µs

NOTES:

1. Typical conditions are +25°C with V_{CC} and V_{PP} at the center of the specified voltage range. Production programming using V_{CC} = 5.0V, V_{PP} = 12.0V typically results in a 60% reduction in programming time.
2. Maximum program timings apply only to the two parameter blocks and the 96-KB main block.
3. This value was previously 100 µs, but will now remain unspecified until further notice