Audio Dual Matched PNP Transistor

SSM2220

FEATURES

- Very Low Voltage Noise ..... @ 100Hz, 1nV/$\sqrt{Hz}$ Max
- High Gain Bandwidth ..... 190MHz Typ
- Excellent Gain ..... @ I_C = 1mA, 165 Typ
- Tight Gain Matching ..... 3% Max
- Outstanding Logarithmic Conformance .. r_{BE} = 0.3Ω Typ
- Low Offset Voltage ..... 200µV Max
- Low Cost

APPLICATIONS

- Microphone Preamplifiers
- Tape-Head Preamplifiers
- Current Sources and Mirrors
- Low Noise Precision Instrumentation
- Voltage Controlled Amplifiers/Multipliers

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2220P	–40°C to +85°C	PDIP	P-8
SSM2220S	–40°C to +85°C	SOIC	S-8
SSM2220S-REEL	–40°C to +85°C	SOIC	S-8

GENERAL DESCRIPTION

The SSM2220 is a dual low noise matched PNP transistor which has been optimized for use in audio applications.

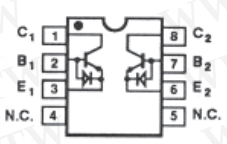
The ultra-low input voltage noise of the SSM2220 is typically only 0.7nV/$\sqrt{Hz}$ over the entire audio bandwidth of 20Hz to 20kHz. The low noise, high bandwidth (190MHz), and Offset Voltage of (200µV Max) make the SSM2220 an ideal choice for demanding low noise preamplifier applications.

The SSM2220 also offers excellent matching of the current gain (Δh_{FE}) to about 0.5% which will help to reduce the high order amplifier harmonic distortion. In addition, to insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction were used to clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

Another feature of the SSM2220 is its very low bulk resistance of 0.3Ω typically which assures accurate logarithmic conformance.

The SSM2220 is offered in 8-pin plastic, dual-in-line, and SO and its performance and characteristics are guaranteed over the extended industrial temperature range of –40°C to +85°C.

PIN CONNECTIONS



8-PIN
PLASTIC DIP
(P-Suffix)

8-PIN
SO
(S-Suffix)

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

ABSOLUTE MAXIMUM RATINGS

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Operating Temperature Range
SSM2220P ..... –40°C to +85°C
SSM2220S ..... –40°C to +85°C
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SO packages.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM2220 MIN	TYP	MAX	UNITS
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA I_C = 100µA I_C = 10µA	80 70 60	165 150 120	– – –	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	–	0.5	6	%
Noise Voltage Density (Note 3)	e_N	I_C = 1mA, V_{CB} = 0V f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz	– – – –	0.8 0.7 0.7 0.7	2 1 1 1	nV/√Hz
Offset Voltage (Note 4)	V_{OS}	V_{CB} = 0V, I_C = 100µA	–	40	200	µV
Offset Voltage Change vs. Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100µA V_{CB1} = 0V V_{CB2} = –36V	–	11	200	µV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C1} = 10µA, I_{C2} = 1mA	–	12	75	µV
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	–	6	45	nA
Collector-Base Leakage Current	I_{CBO}	V_{CB} = –36V = V_{MAX}	–	50	400	pA
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10µA ≤ I_C ≤ 1mA	–	0.3	0.75	Ω
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100µA	–	0.026	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100(\Delta I_B)\, h_{FE}(MIN)}{I_C}.$$

3. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.
4. Offset voltage is defined as:
$V_{OS} = V_{BE1} - V_{BE2}$,
where V_{OS} is the differential voltage for

$$I_{C2} = I_{C2} : V_{OS} = V_{BE1} - V_{BE2} = \frac{KT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

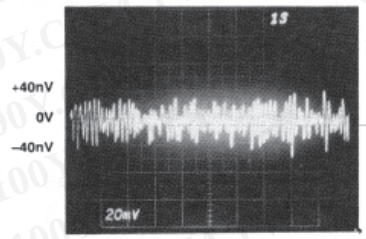
ELECTRICAL CHARACTERISTICS at –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM2220 MIN	SSM2220 TYP	SSM2220 MAX	UNITS
Current Gain	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA I_C = 100µA I_C = 10µA	 60 50 40	 120 105 90	 – – –	
Offset Voltage	V_{OS}	I_C = 100µA, V_{CB} = 0V	–	30	265	µV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100µA, V_{CB} = 0V	–	0.3	1.0	µV/°C
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	–	10	200	nA
Breakdown Voltage	BV_{CEO}		36	–	–	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} << V_{BE}$) where T = 298°K for T_A = 25°C.

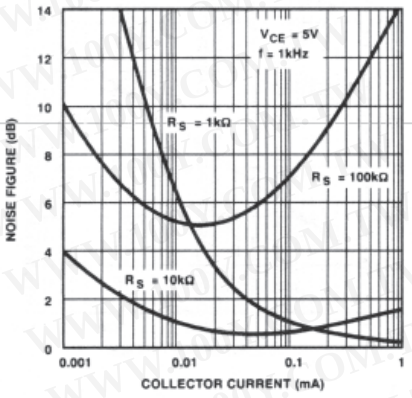
TYPICAL PERFORMANCE CHARACTERISTICS

LOW FREQUENCY NOISE

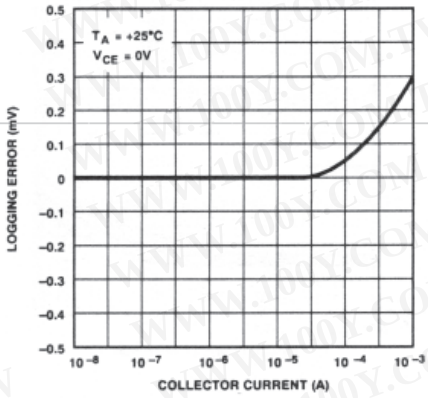


VERTICAL = 40nV/DIV
HORIZONTAL = 1s/DIV
V_{CE} = 5V
I_C = 1mA
T_A = +25°C

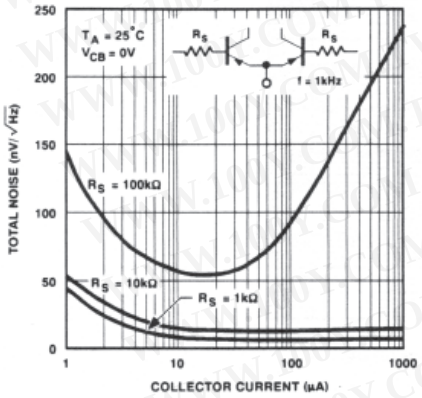
NOISE FIGURE vs COLLECTOR CURRENT



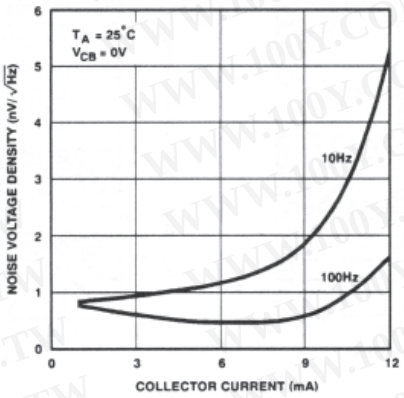
EMITTER-BASE LOG CONFORMITY



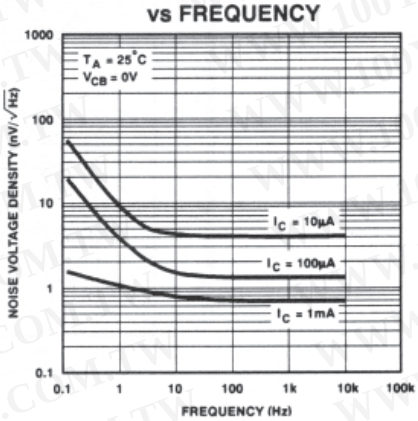
TOTAL NOISE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



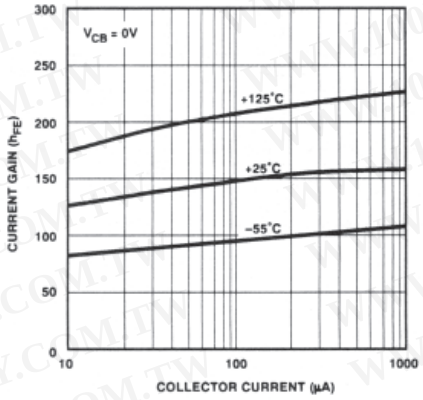
NOISE VOLTAGE DENSITY vs FREQUENCY



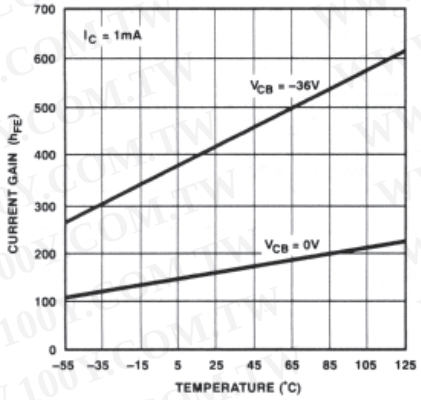
SSM2220–Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

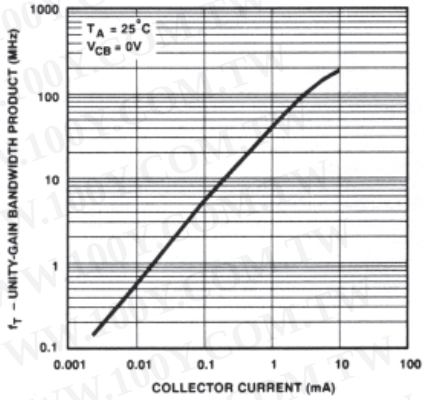
CURRENT GAIN vs COLLECTOR CURRENT



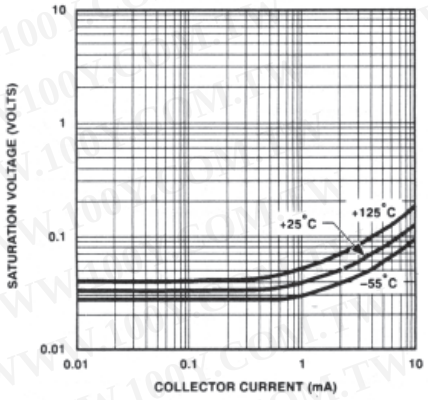
CURRENT GAIN vs TEMPERATURE



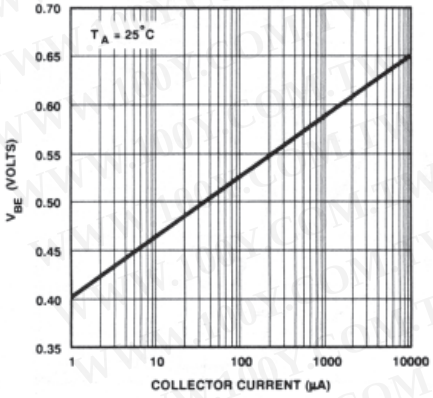
GAIN BANDWIDTH vs COLLECTOR CURRENT



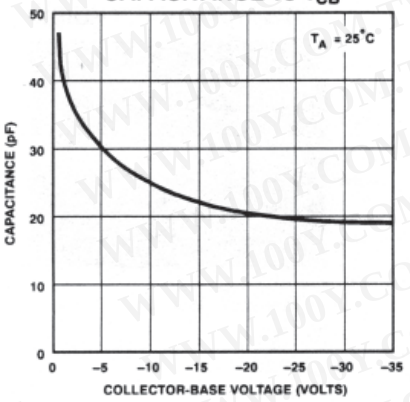
SATURATION VOLTAGE vs COLLECTOR CURRENT



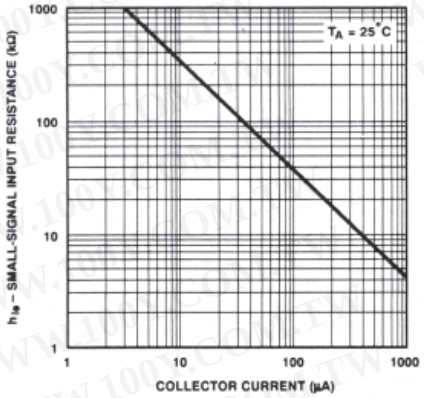
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



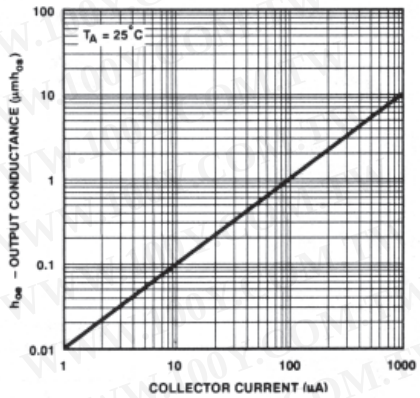
COLLECTOR-BASE CAPACITANCE vs V_{CB}



SMALL-SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



SMALL-SIGNAL OUTPUT CONDUCTANCE (h_{oe}) vs COLLECTOR CURRENT



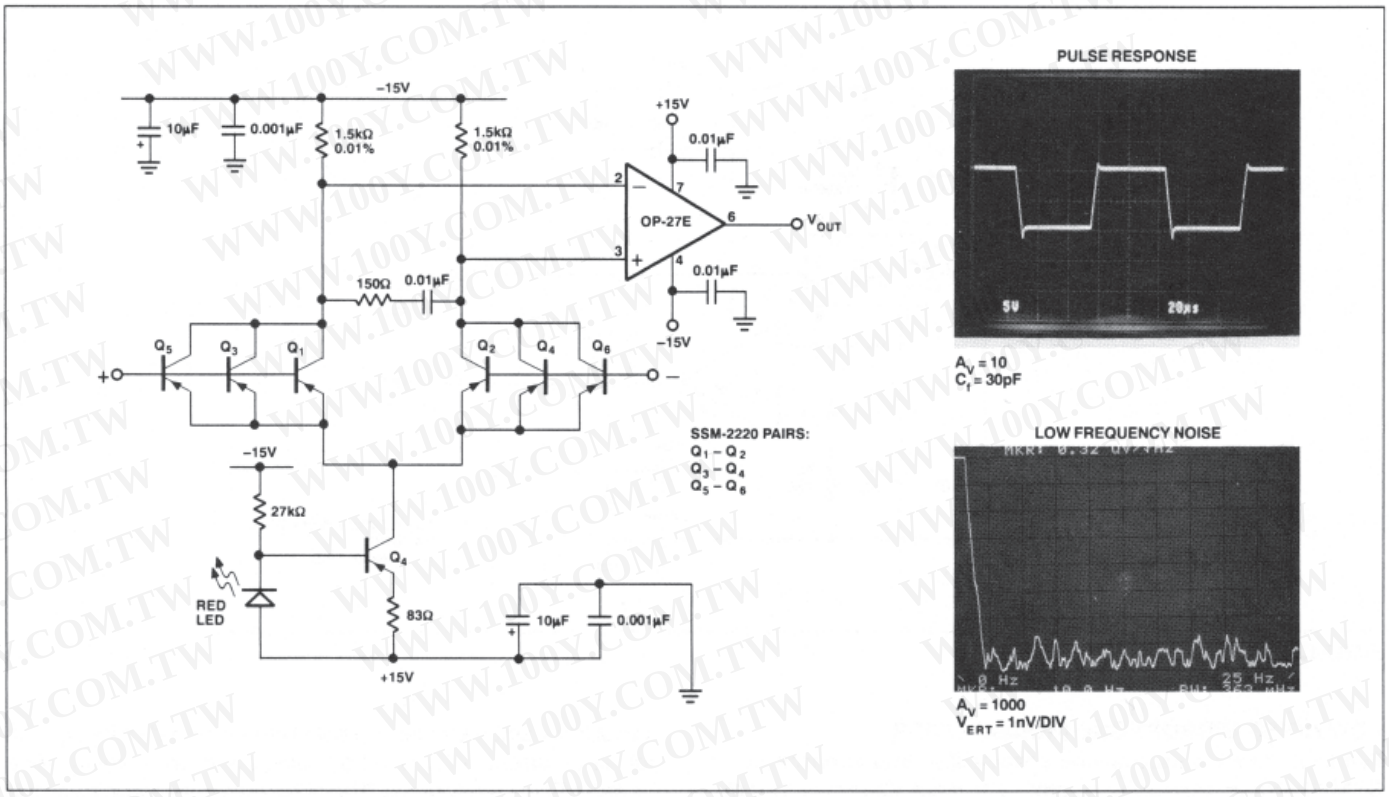


FIGURE 1a: *Super Low Noise Amplifier*

APPLICATIONS INFORMATION

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 1a is a super low noise amplifier with equivalent input voltage noise of 0.32nV/$\sqrt{Hz}$. By paralleling SSM-2220 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by $\sqrt{3}$. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

This amplifier exhibits excellent full power AC performance, 0.08% THD into a 600Ω load, making it suitable for exacting audio applications (see Figure 1b).

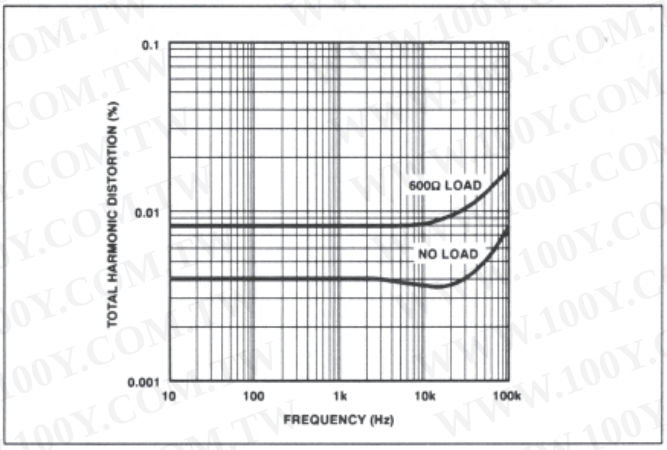


FIGURE 1b: *Super Low Noise Amplifier – Total Harmonic Distortion*

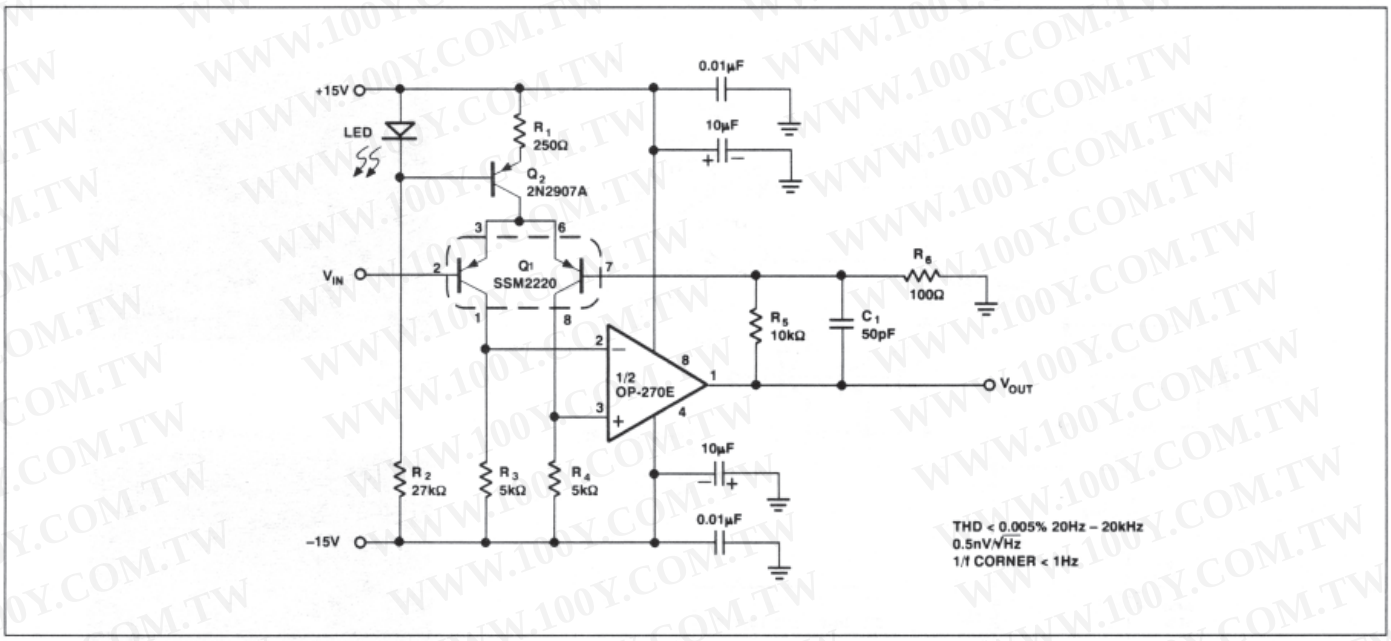


FIGURE 2: *Super Low Noise Amplifier*

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 2 shows a microphone preamplifier that consists of a SSM2220 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2mA per side, which reduces the SSM2220 transistor's voltage noise. The $1/f$ corner is less than 1Hz. Total harmonic distortion is under 0.005% for a $10V_{p-p}$ signal from 20Hz to 20kHz. The preamp gain is 100, but can be modified by varying R_5 or R_6 ($V_{OUT}/V_{IN} = R_5/R_6 + 1$).

A total input stage emitter current of 4mA is provided by Q_2. The constant current in Q_2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1V, is dropped across the 250Ω resistor which produces a temperature stabilized emitter current.

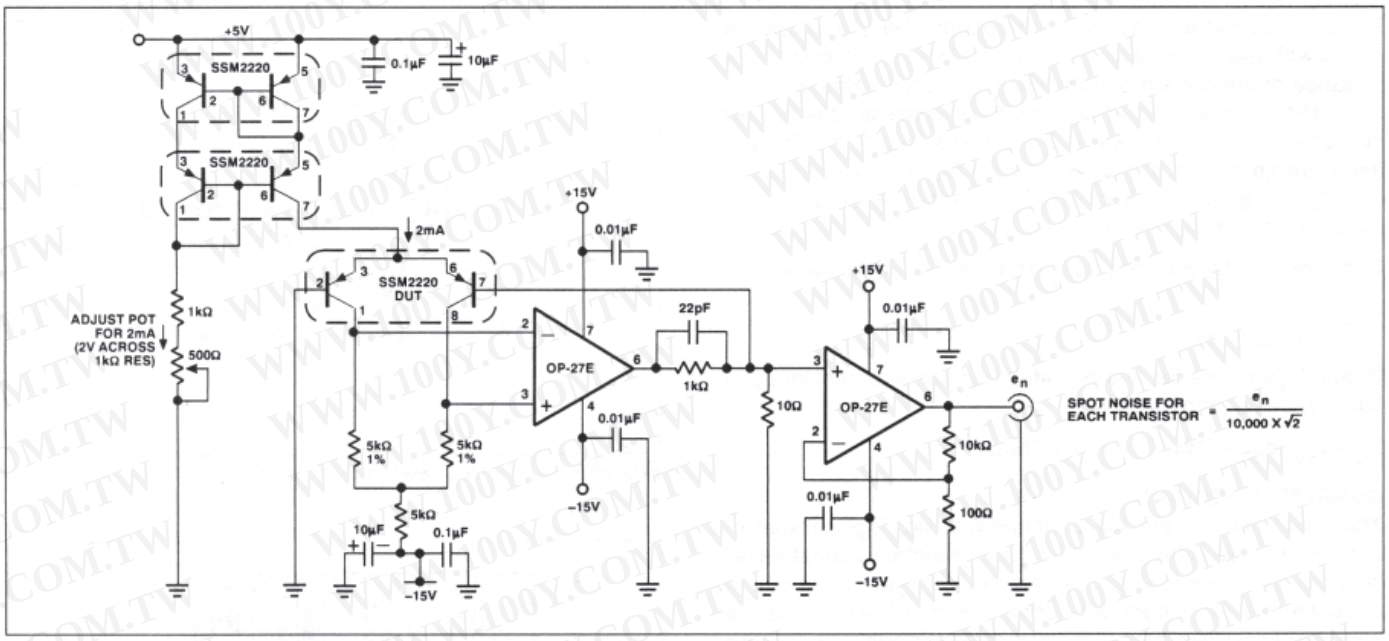


FIGURE 3: *SSM2220 Voltage Noise Measurement Circuit*

SSM2220 NOISE MEASUREMENT

All resistive components (Johnson noise, $e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/$\sqrt{\text{Hz}}$, where R is in kΩ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors, $I_n = 0.556\sqrt{I}$ pA/$\sqrt{\text{Hz}}$ where I is in µA) contribute to the system input noise.

Figure 3 illustrates a technique for measuring the equivalent input noise voltage of the SSM2220. 1mA of stage current is used to bias each side of the differential pair. The 5kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the SSM2220. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048nV/$\sqrt{\text{Hz}}$. This is considerably less than the typical 0.8nV/$\sqrt{\text{Hz}}$ input noise voltage of the SSM2220 transistor.

The noise contribution of the OP-27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density (e_{in} x 10000) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the SSM-2220, the output is divided by $\sqrt{2}$ to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

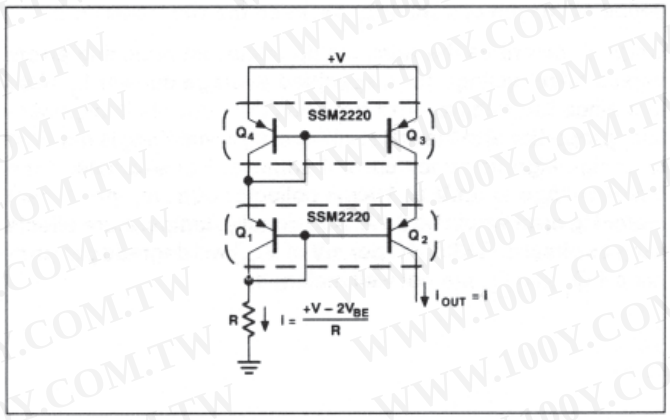


FIGURE 4: *Cascode Current Source*

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between V_{BE}'s required to equalize collector current) and gain matching, the SSM2220 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications, a wider signal bandwidth.

Figure 4 illustrates a cascode current mirror consisting of two SSM2220 transistor pairs.

The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h_{oe} vs. Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100µA, we have:

$$ro_{Q3} = \frac{1}{1.0\mu MHOS} = 1M\Omega.$$

Q_2 and Q_3 are in series and operate at the same current level, so the total output impedance is:

$$R_O = h_{FE}\, ro_{Q3} \approx (160)(1M\Omega) = 160M\Omega.$$

CURRENT MATCHING

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 5. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a non-zero V_{OS}, we define ΔI_C as the current error between the two transistors.

Graph 5 describes the relationship of current matching errors versus offset voltage for a specified average current I_C. Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5mV at 100µA collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3µV/°C per mV of V_{OS}) will degrade performance if Q_1 and Q_2 are not well matched.

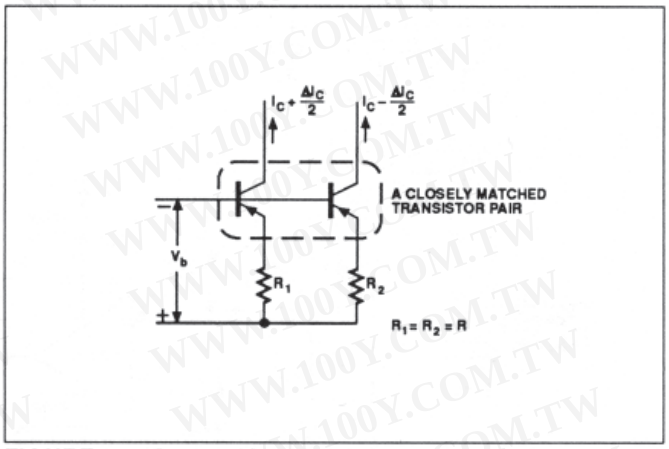


FIGURE 5a: *Current Matching Circuit*

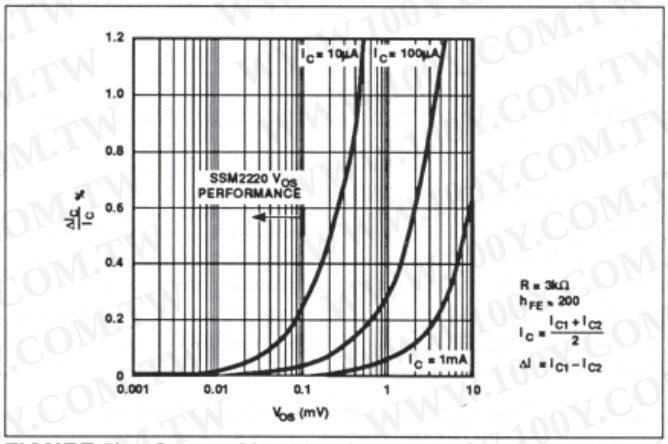
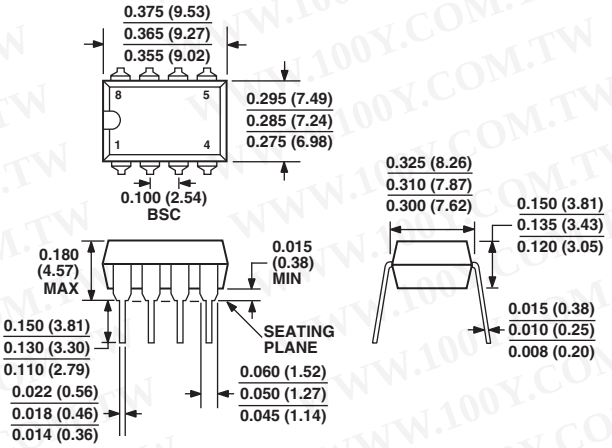


FIGURE 5b: *Current Matching Accuracy % vs. Offset Voltage*

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
[P-Suffix]
(N-8)

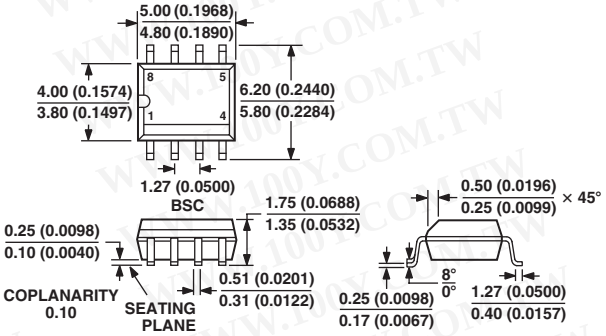
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
[S-Suffix]
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
11/03—Data Sheet changed from REV. A to REV. B.	
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Updated OUTLINE DIMENSIONS	9