



# CEPF640/CEBF640 CEFF640

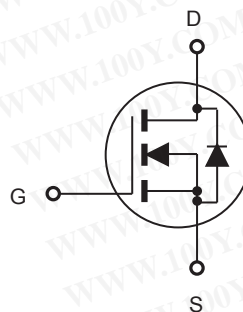
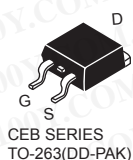
## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEPF640	200V	0.15Ω	19A	10V
CEBF640	200V	0.15Ω	19A	10V
CEFF640	200V	0.15Ω	19A <sup>d</sup>	10V

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
 Http://www.100y.com.tw

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-220F full-pak for through hole.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	200		V
Gate-Source Voltage	V <sub>GS</sub>	±20		V
Drain Current-Continuous	I <sub>D</sub>	19	19 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	76	76 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	125	40	W
		1.0	0.32	W/°C
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.0	3.1	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



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### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	200			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 160V, V_{GS} = 0V$			25	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 10A$		0.125	0.150	$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Forward Transconductance	$g_{FS}$	$V_{DS} = 10V, I_D = 9A$		9		S
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1955		pF
Output Capacitance	$C_{oss}$			355		pF
Reverse Transfer Capacitance	$C_{rss}$			55		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100V, I_D = 11A, V_{GS} = 10V, R_{GEN} = 9.1\Omega$		21	42	ns
Turn-On Rise Time	$t_r$			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			66	132	ns
Turn-Off Fall Time	$t_f$			11	22	ns
Total Gate Charge	$Q_g$	$V_{DS} = 160V, I_D = 19A, V_{GS} = 10V$		44	57	nC
Gate-Source Charge	$Q_{gs}$			8		nC
Gate-Drain Charge	$Q_{gd}$			14		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				19	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 19A^g$			1.5	V
<b>Notes :</b> <ul style="list-style-type: none"> <li>a. Repetitive Rating : Pulse width limited by maximum junction temperature .</li> <li>b. Pulse Test : Pulse Width <math>\leq 300\mu s</math>, Duty Cycle <math>\leq 2\%</math> .</li> <li>c. Guaranteed by design, not subject to production testing.</li> <li>d. Limited only by maximum temperature allowed .</li> <li>e. Pulse width limited by safe operating area .</li> <li>f. Full package <math>I_{S(max)} = 10.5A</math> .</li> <li>g. Full package <math>V_{SD}</math> test condition <math>I_S = 10.5A</math> .</li> <li>i. <math>L = 1mH, I_{AS} = 25A, V_{DD} = 25V, R_G = 25\Omega, \text{Starting } T_J = 25\text{ C}</math></li> </ul>						



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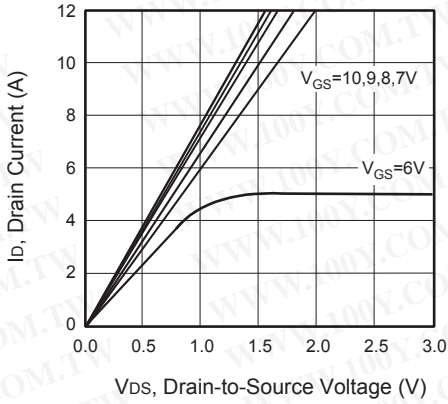


Figure 1. Output Characteristics

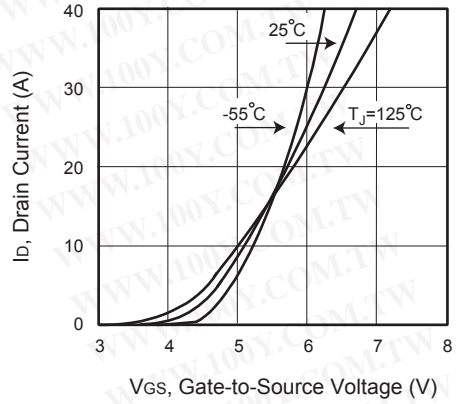


Figure 2. Transfer Characteristics

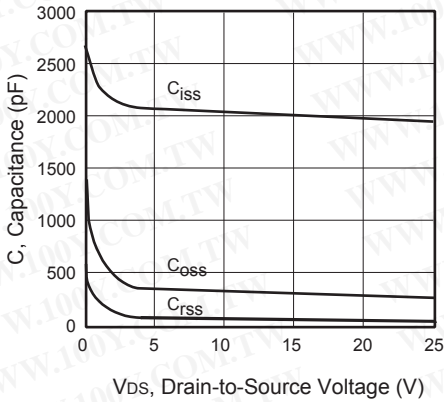


Figure 3. Capacitance

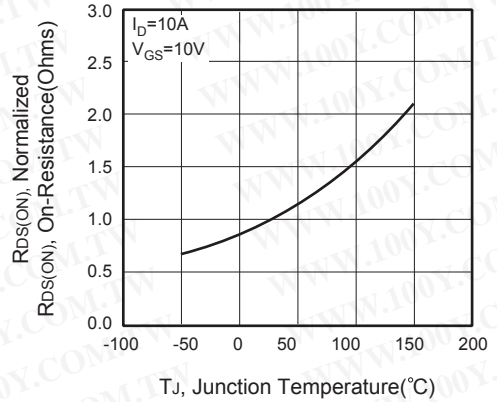


Figure 4. On-Resistance Variation with Temperature

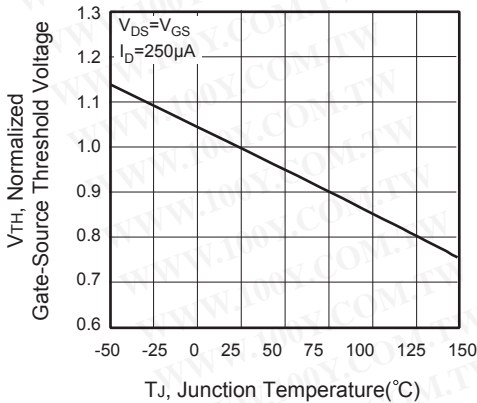


Figure 5. Gate Threshold Variation with Temperature

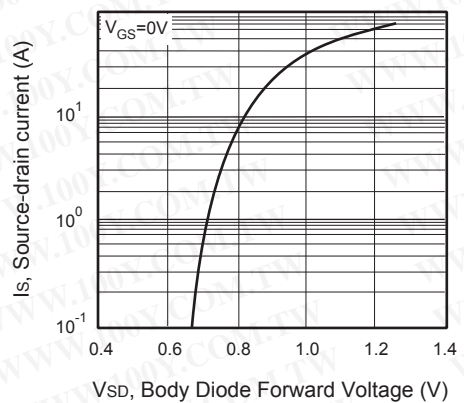


Figure 6. Body Diode Forward Voltage Variation with Source Current

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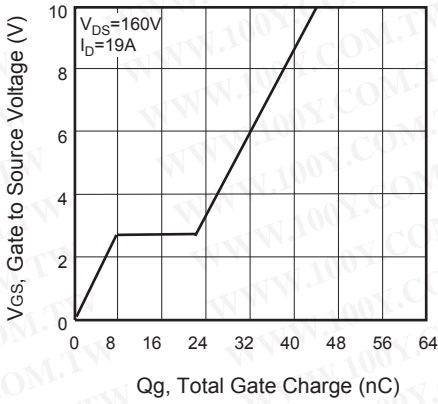


Figure 7. Gate Charge

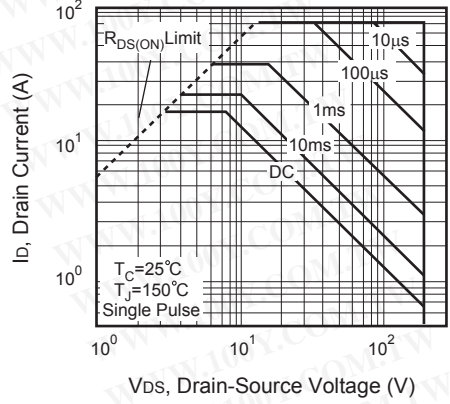


Figure 8. Maximum Safe Operating Area

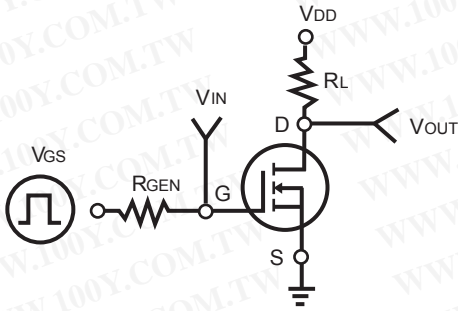


Figure 9. Switching Test Circuit

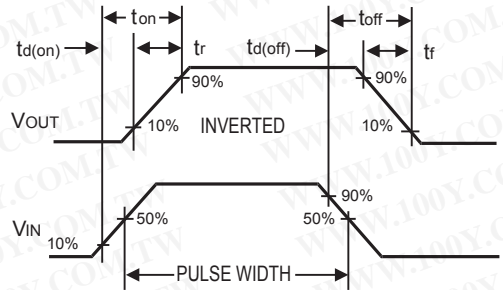


Figure 10. Switching Waveforms

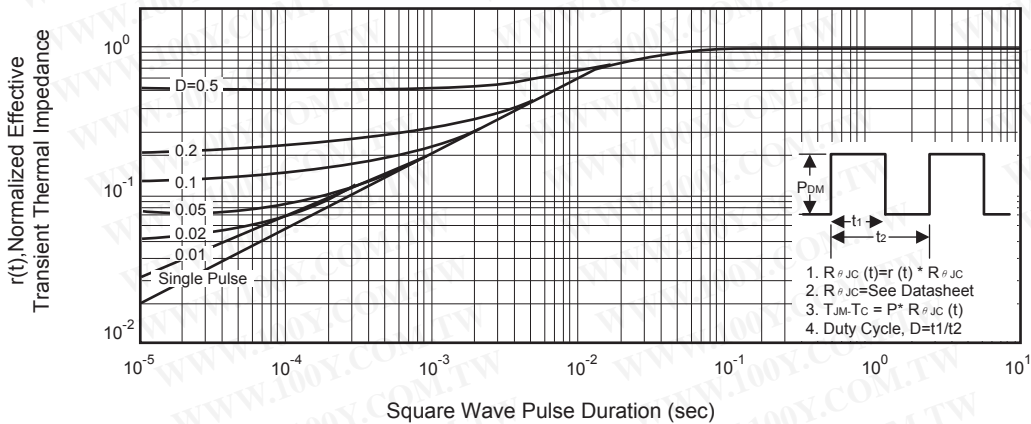


Figure 11. Normalized Thermal Transient Impedance Curve