FAIRCHILD SEMICONDUCTOR®

July 2007

FDMS9620S

Dual N-Channel PowerTrench® MOSFET

Q1: 30V, 16A, 21.5mΩ Q2: 30V, 18A, 13mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 21.5mΩ at V_{GS} = 10V, I_D = 7.5A
- Max $r_{DS(on)}$ = 29.5mΩ at V_{GS} = 4.5V, I_D = 6.5A

Q2: N-Channel

- Max $r_{DS(on)}$ = 13mΩ at V_{GS} = 10V, I_D = 10A
- Max $r_{DS(on)}$ = 17mΩ at V_{GS} = 4.5V, I_D = 8.5A
- Low Qg high side MOSFET
- Low $r_{DS(on)}$ low side MOSFET
- Thermally efficient dual Power 56 package
- Pinout optimized for simple PCB design
- RoHS Compliant

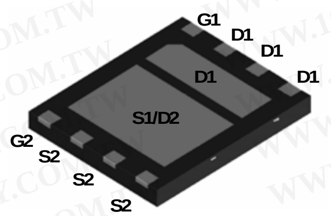
General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal Synchronous Buck power stage in terms of efficiency and PCB utilization. The low switching loss "High Side" MOSFET is complemented by a Low Conduction Loss "Low Side" SyncFET.

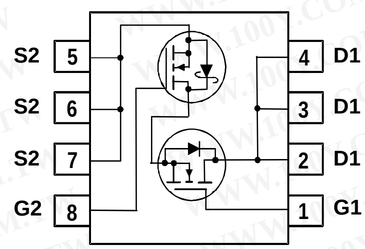
Applications

Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load



Power 56



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter				Q1	Q2	Units
V_{DS}	Drain to Source Voltage				30	30	V
V_{GS}	Gate to Source Voltage				±20	±20	V
I_D	Drain Current	-Continuous (Package limited)	T_C = 25°C		16	18	A
		-Continuous (Silicon limited)	T_C = 25°C		21	44	
		-Continuous	T_A = 25°C	(Note 1a)	7.5	10	
		-Pulsed			60	60	
P_D	Power Dissipation for Single Operation		T_A = 25°C	(Note 1a)	2.5		W
			T_A = 25°C	(Note 1b)	1		
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +150		°C

Thermal Characteristics

Symbol	Parameter		Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case		8.2	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	120		

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS9620S	FDMS9620S	Power 56	13"	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

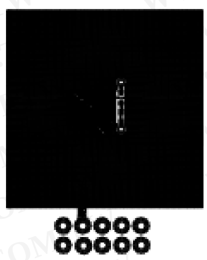
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V I_D = 1mA, V_{GS} = 0V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = 1mA, referenced to 25°C	Q1 Q2		23 23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	Q1 Q2			1 500	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS}= 0V	Q1 Q2			±100 ±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250µA V_{GS} = V_{DS}, I_D = 1mA	Q1 Q2	1 1	1.6 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250µA, referenced to 25°C I_D = 1mA, referenced to 25°C	Q1 Q2		-4 -4		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 7.5A V_{GS} = 4.5V, I_D = 6.5A V_{GS} = 10V, I_D = 7.5A , T_J = 125°C	Q1		18 23 25	21.5 29.5 32	mΩ
		V_{GS} = 10V, I_D = 10A V_{GS} = 4.5V, I_D = 8.5A V_{GS} = 10V, I_D = 10A , T_J = 125°C	Q2		9 13 14	13 17 22	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 7.5A V_{DD} = 10V, I_D = 10A	Q1 Q2		25 27		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHZ	Q1 Q2		500 700	665 935	pF
C_{oss}	Output Capacitance		Q1 Q2		100 500	135 665	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		65 100	100 150	pF
R_g	Gate Resistance	f = 1MHz	Q1 Q2		0.9 1.8		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω	Q1 Q2		11 15	20 27	ns
t_r	Rise Time		Q1 Q2		7 13	14 24	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		23 27	37 44	ns
t_f	Fall Time		Q1 Q2		2.3 7	10 14	ns
Q_g	Total Gate Charge	Q1 V_{DD} = 15V, V_{GS} = 10V ,I_D = 7.5A Q2 V_{DD} = 15V, V_{GS} = 10V ,I_D = 10A	Q1 Q2		10 18	14 25	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		1.7 2.8		nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		2.0 3.6		nC

Electrical Characteristics T_J = 25°C unless otherwise noted

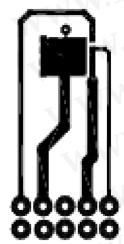
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			2.1 3.5	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.1A (Note 2) V_{GS} = 0V, I_S = 3.5A (Note 2)	Q1 Q2		0.7 0.5	1.2 1.0	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 7.5A, di/dt = 100A/µs	Q1 Q2		13 14		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 10A, di/dt = 300A/µs	Q1 Q2		4 9		nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a.50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 120°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

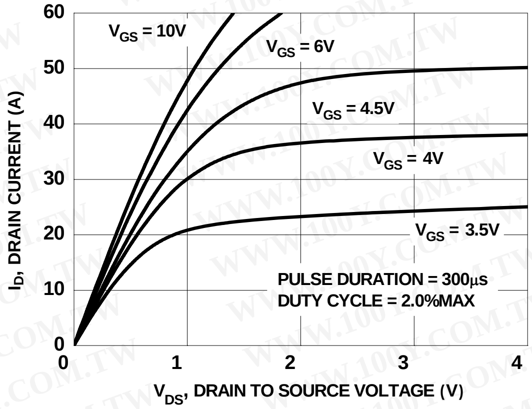


Figure 1. On Region Characteristics

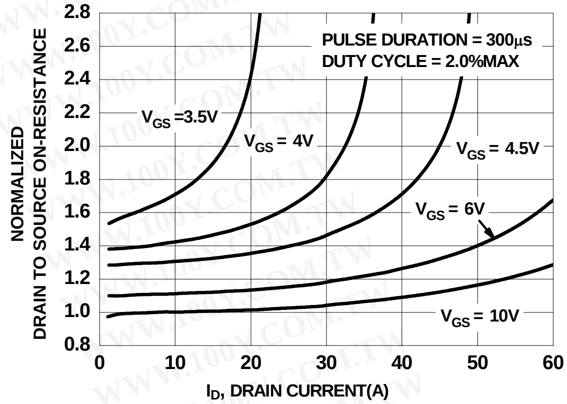


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

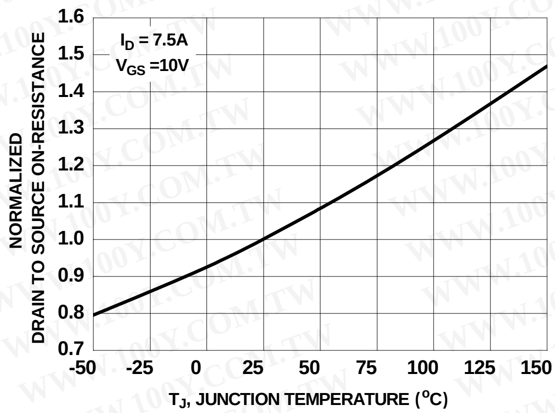


Figure 3. Normalized On Resistance vs Junction Temperature

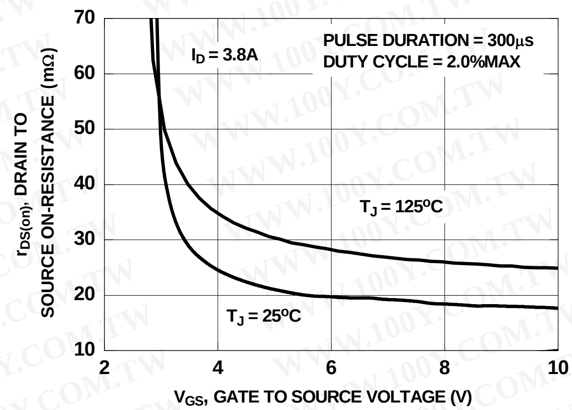


Figure 4. On-Resistance vs Gate to Source Voltage

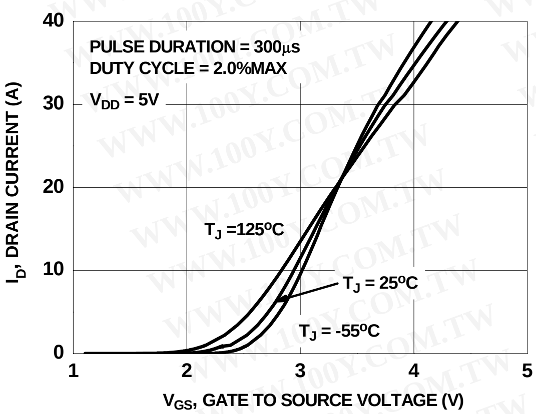


Figure 5. Transfer Characteristics

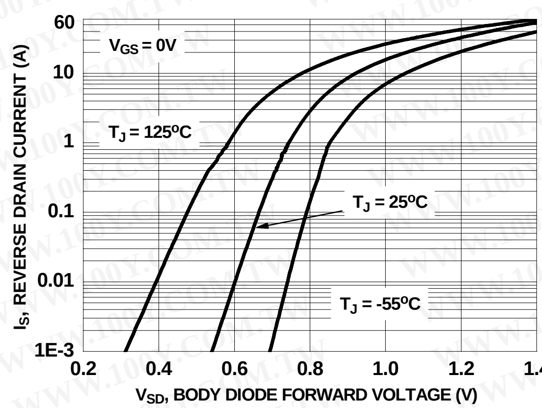


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

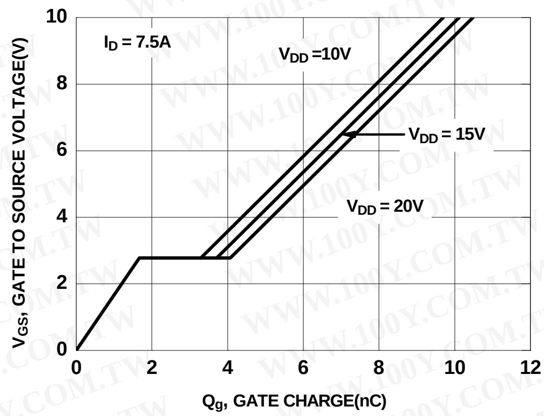


Figure 7. Gate Charge Characteristics

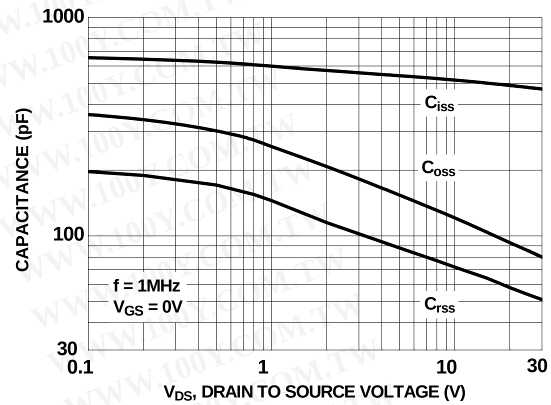


Figure 8. Capacitance vs Drain to Source Voltage

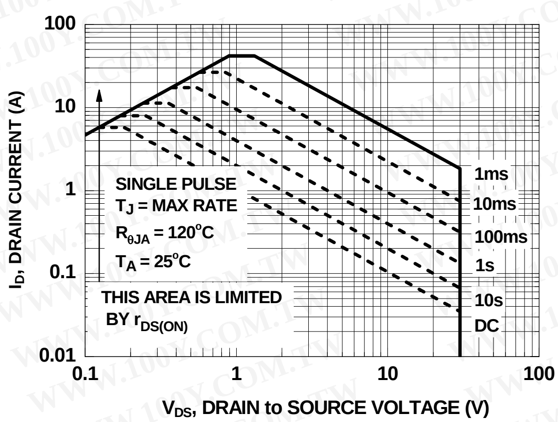


Figure 9. Forward Bias Safe Operating Area

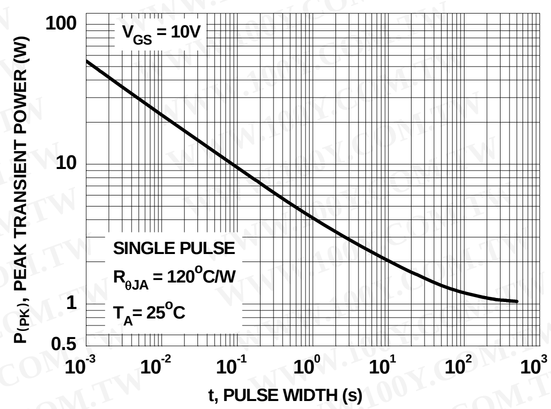


Figure 10. Single Pulse Maximum Power Dissipation

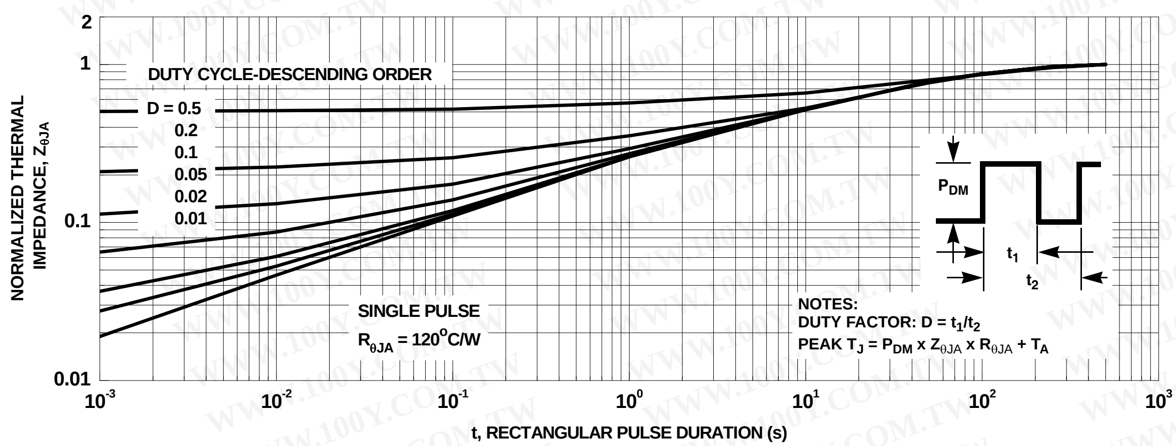


Figure 11. Transient Thermal Response Curve

Typical Characteristics (Q2 SyncFET)

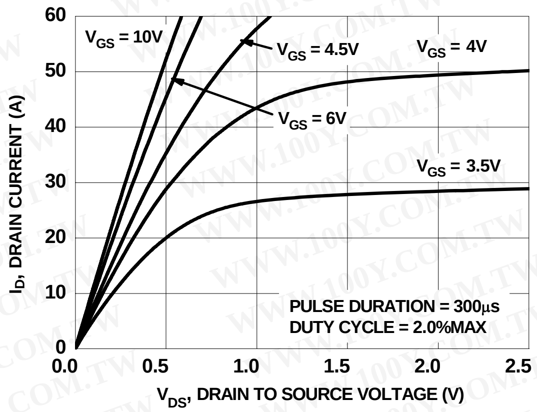


Figure 12. On-Region Characteristics

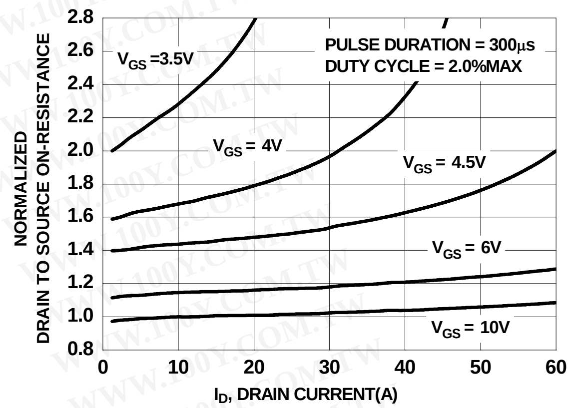


Figure 13. Normalized on-Resistance vs Drain Current and Gate Voltage

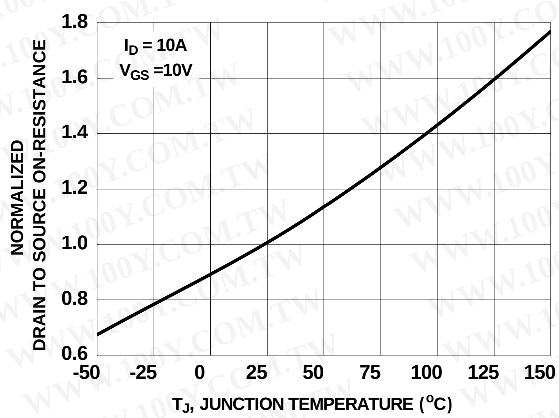


Figure 14. Normalized On-Resistance vs Junction Temperature

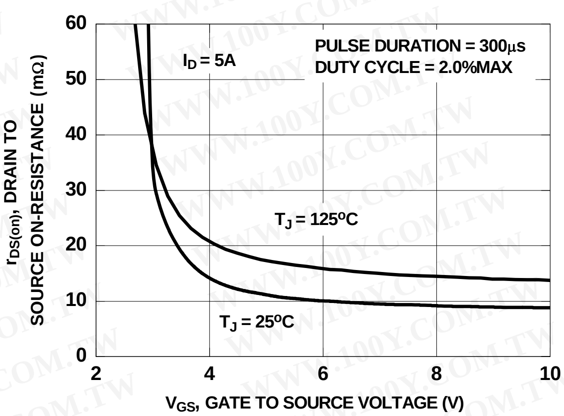


Figure 15. On-Resistance vs Gate to Source Voltage

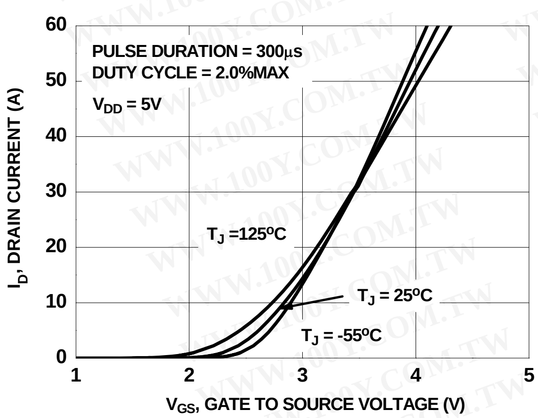


Figure 16. Transfer Characteristics

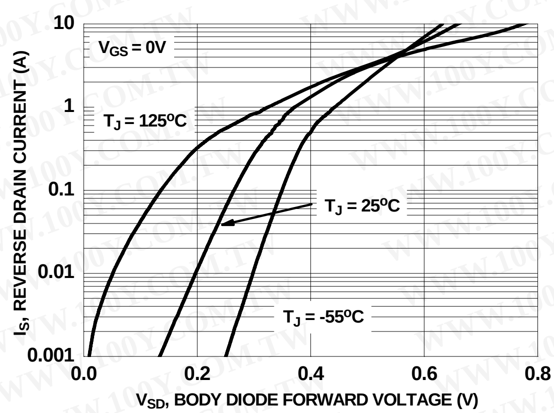


Figure 17. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

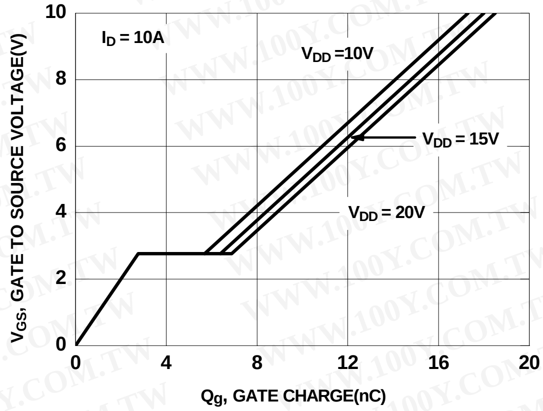


Figure 18. Gate Charge Characteristics

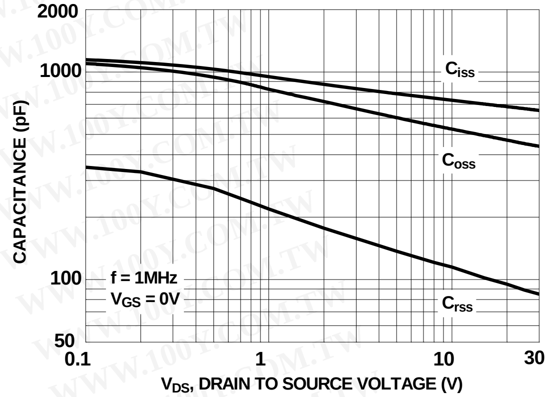
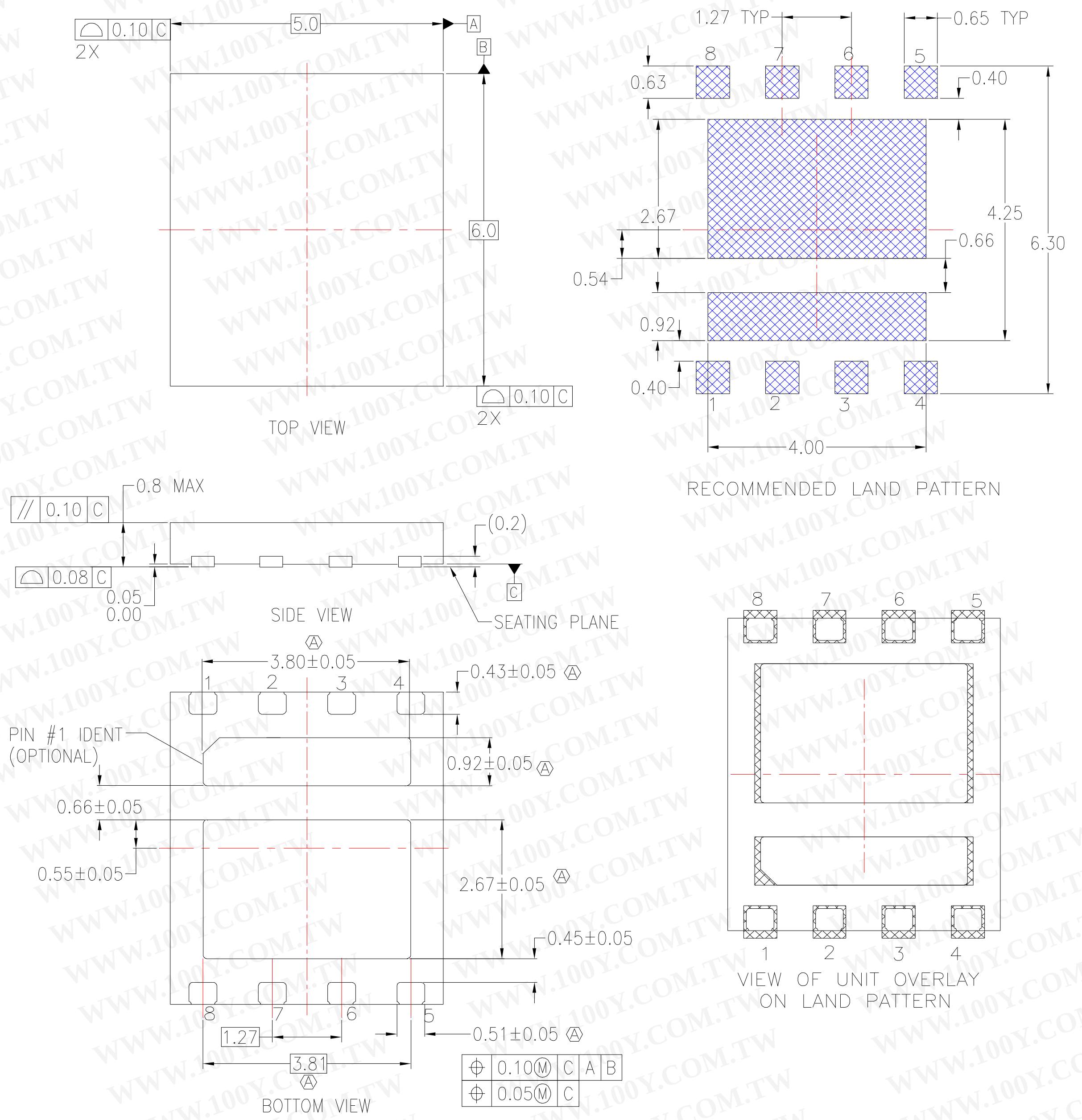


Figure 19. Capacitance vs Drain to Source Voltage

Dimensional Outline and Pad Layout



NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO−229. DATED 11/2001.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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