



# FDZ7296

## 30V N-Channel PowerTrench® BGA MOSFET

### General Description

Combining Fairchild's advanced PowerTrench process with state-of-the-art BGA packaging, the FDZ7296 minimizes both PCB space and  $R_{DS(ON)}$ . This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $R_{DS(ON)}$ .

### Applications

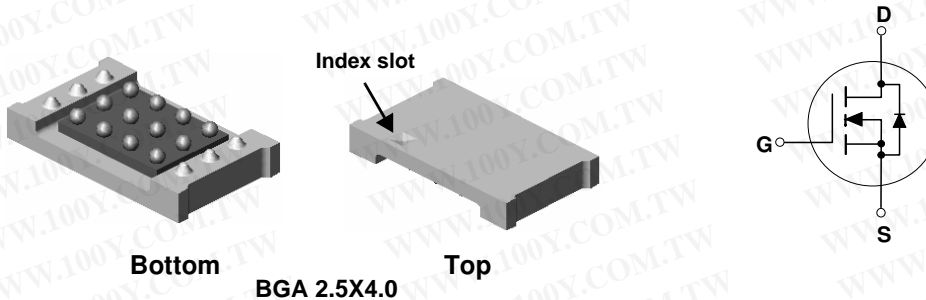
- High-side Mosfet in DC-DC converters for Server and Notebook applications
- RoHS Compliant



### Features

11 A, 30 V.  $R_{DS(ON)} = 8.5 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 12 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$

- Occupies only  $0.10 \text{ cm}^2$  of PCB area: 1/3 the area of SO-8.
- Ultra-thin package: less than 0.80 mm height when mounted to PCB.
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Optimized for low  $Q_g$  and  $Q_{gd}$  to enable fast switching and reduce  $CdV/dt$  gate coupling



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	11	A
		20	
$P_D$	Power Dissipation (Steady State) (Note 1a)	2.1	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Ball (Note 1)	6.3	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.6	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
7296	FDZ7296	7"	8mm	3000 units

## Electrical Characteristics

T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		27		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

### On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.8	3	V
ΔV <sub>GS(th)</sub> ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		-4.9		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11 A V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 11 A, T <sub>J</sub> = 125°C		7 9 9.1	8.5 12 13	mΩ

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		1520		pF
C <sub>oss</sub>	Output Capacitance			420		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			130		pF
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 11 A		46		S
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15 mV, f = 1.0 MHz		1.1		Ω

### Switching Characteristics (Note 2)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		10	20	ns
t <sub>r</sub>	Turn-On Rise Time			4	8	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			27	43	ns
t <sub>f</sub>	Turn-Off Fall Time			13	23	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at V <sub>gs</sub> =10V	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 11 A,		22	31	nC
Q <sub>g</sub>	Total Gate Charge at V <sub>gs</sub> =5V			12	17	nC
Q <sub>gs</sub>	Gate-Source Charge			4.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			3.1		nC

### Drain-Source Diode Characteristics and Maximum Ratings

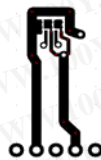
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current			1.7		A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.7 A (Note 2)		0.7	1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = 11 A		28		nS
Q <sub>rr</sub>	Diode Reverse Recovery Charge	d <sub>I</sub> /d <sub>t</sub> = 100 A/μs (Note 2)		18		nC

#### Notes:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, R<sub>θJB</sub>, is defined for reference. For R<sub>θJC</sub>, the thermal reference point for the case is defined as the top surface of the copper chip carrier. R<sub>θJC</sub> and R<sub>θJB</sub> are guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.



- a) 60 °C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB

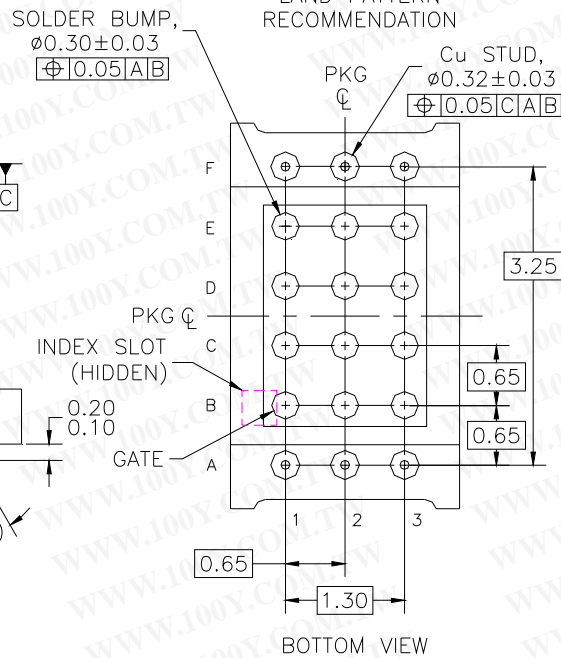
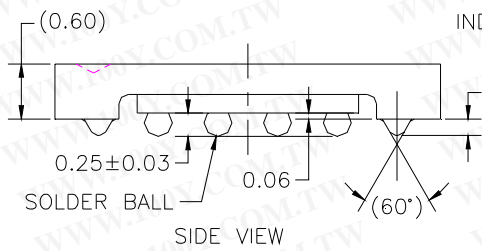
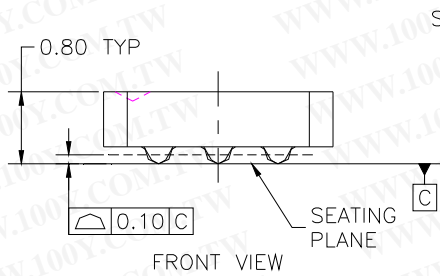
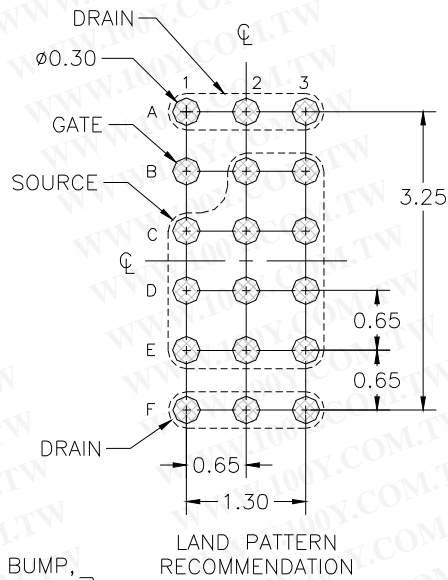
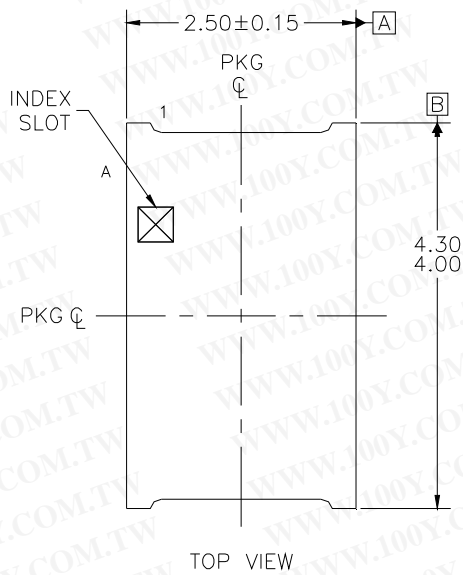


- b) 108 °C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

# Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
- C) BALL CONFIGURATION TABLE

TERMINAL	DESIGNATION
A1,A2,A3,F1,F2,F3	DRAIN
B1	GATE
B2,B3,C1,C2,C3, D1,D2,D3,E1,E2,E3	SOURCE

FDZ7296 30V N-Channel PowerTrench® BGA MOSFET

## Typical Characteristics

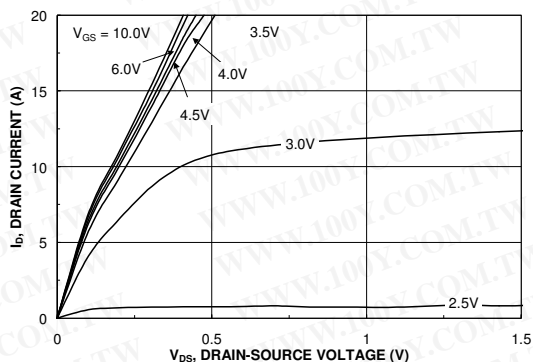


Figure 1. On-Region Characteristics.

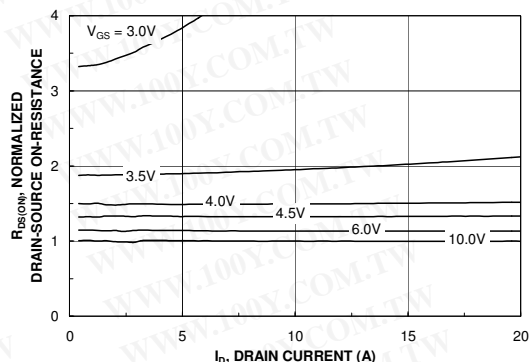


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

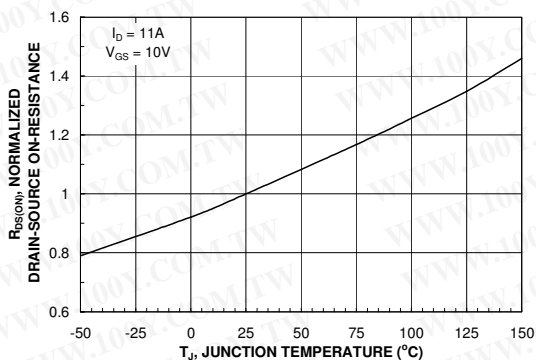


Figure 3. On-Resistance Variation with Temperature.

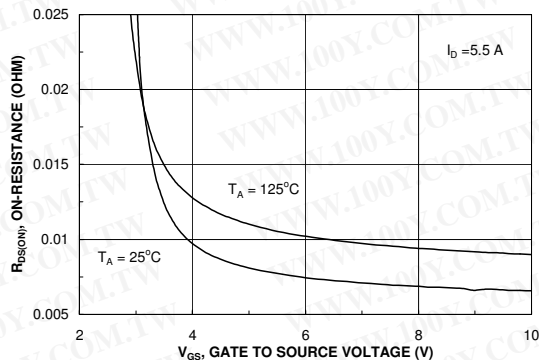


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

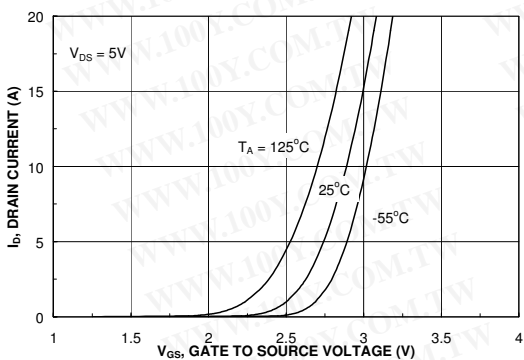


Figure 5. Transfer Characteristics.

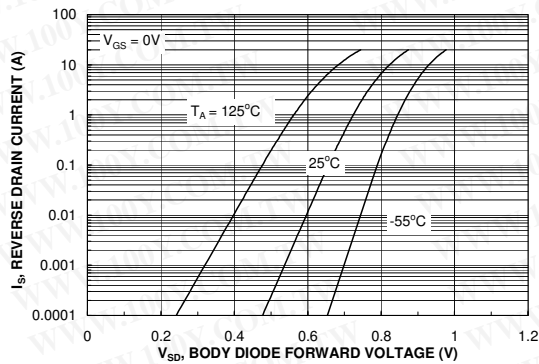


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

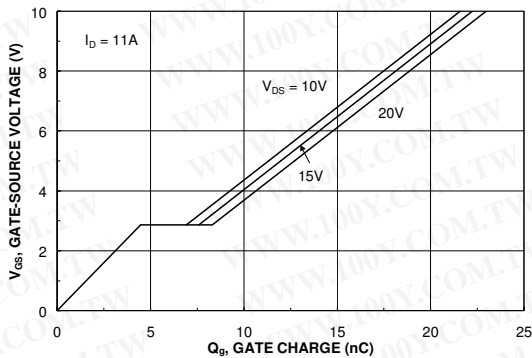


Figure 7. Gate Charge Characteristics.

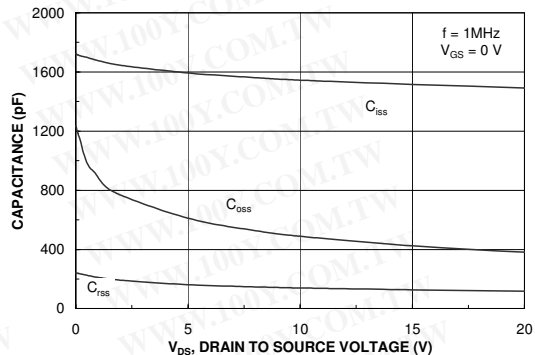


Figure 8. Capacitance Characteristics.

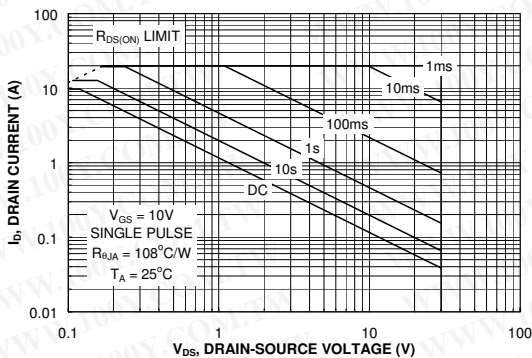


Figure 9. Maximum Safe Operating Area.

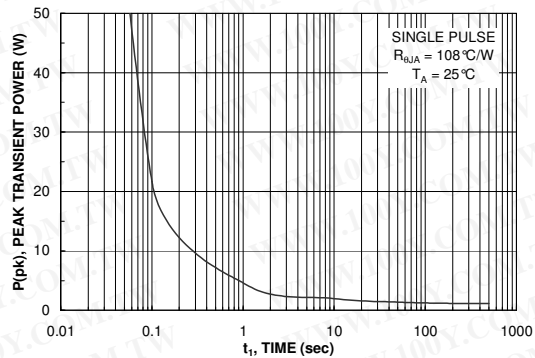


Figure 10. Single Pulse Maximum Power Dissipation.

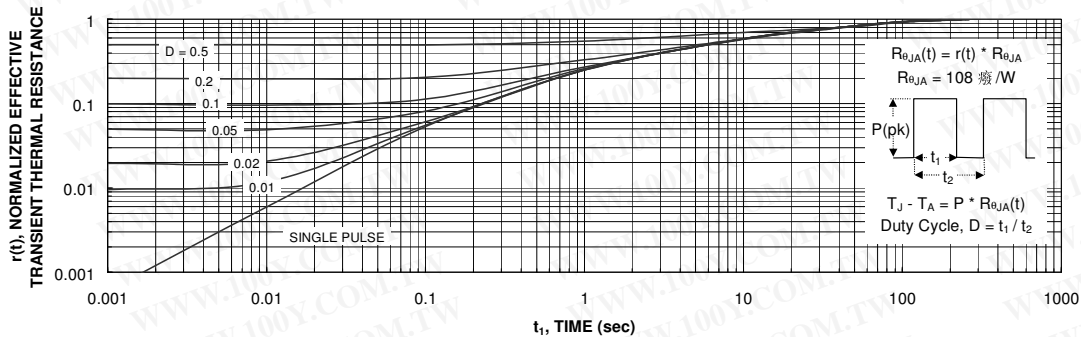


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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