

# FQD12N20L / FQU12N20L

## 200V LOGIC N-Channel MOSFET

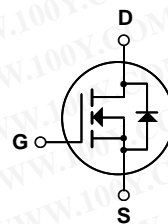
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, motor control.

### Features

- 9.0A, 200V,  $R_{DS(on)} = 0.28\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 16 nC)
- Low Crss ( typical 17 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Low level gate drive requirement allowing direct operation from logic drivers
- RoHS Compliant



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

| Symbol                            | Parameter   | FQD12N20L / FQU12N20L | Units |
|-----------------------------------|---|-----------------------|-------|
| V <sub>DSS</sub>                  | Drain-Source Voltage  | 200                   | V     |
| I <sub>D</sub>                    | Drain Current - Continuous (T <sub>C</sub> = 25°C)<br>- Continuous (T <sub>C</sub> = 100°C) | 9.0                   | A     |
|                                   |   | 5.7                   | A     |
| I <sub>DM</sub>                   | Drain Current - Pulsed (Note 1)   | 36                    | A     |
| V <sub>GSS</sub>                  | Gate-Source Voltage   | ± 20                  | V     |
| E <sub>AS</sub>                   | Single Pulsed Avalanche Energy (Note 2)   | 210                   | mJ    |
| I <sub>AR</sub>                   | Avalanche Current (Note 1)  | 9.0                   | A     |
| E <sub>AR</sub>                   | Repetitive Avalanche Energy (Note 1)  | 5.5                   | mJ    |
| dv/dt                             | Peak Diode Recovery dv/dt (Note 3)  | 5.5                   | V/ns  |
| P <sub>D</sub>                    | Power Dissipation (T <sub>A</sub> = 25°C) *   | 2.5                   | W     |
|                                   | Power Dissipation (T <sub>C</sub> = 25°C)<br>- Derate above 25°C                            | 55                    | W     |
|                                   |   | 0.44                  | W/°C  |
| T <sub>J</sub> , T <sub>STG</sub> | Operating and Storage Temperature Range   | -55 to +150           | °C    |
| T <sub>L</sub>                    | Maximum lead temperature for soldering purposes,<br>1/8" from case for 5 seconds            | 300                   | °C    |

### Thermal Characteristics

| Symbol           | Parameter                                 | Typ | Max  | Units |
|------------------|---|-----|------|-------|
| R <sub>θJC</sub> | Thermal Resistance, Junction-to-Case      | --  | 2.27 | °C/W  |
| R <sub>θJA</sub> | Thermal Resistance, Junction-to-Ambient * | --  | 50   | °C/W  |
| R <sub>θJA</sub> | Thermal Resistance, Junction-to-Ambient   | --  | 110  | °C/W  |

\* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

| Symbol                         | Parameter                                 | Test Conditions   | Min | Typ  | Max  | Units               |
|--------------------------------|---|---|-----|------|------|---------------------|
| <b>Off Characteristics</b>     |   |   |     |      |      |                     |
| $BV_{DSS}$                     | Drain-Source Breakdown Voltage            | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$               | 200 | --   | --   | V                   |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ | --  | 0.14 | --   | V/ $^\circ\text{C}$ |
| $I_{DSS}$                      | Zero Gate Voltage Drain Current           | $V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$                | --  | --   | 1    | $\mu\text{A}$       |
|                                |   | $V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$            | --  | --   | 10   | $\mu\text{A}$       |
| $I_{GSSF}$                     | Gate-Body Leakage Current, Forward        | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$                 | --  | --   | 100  | nA                  |
| $I_{GSSR}$                     | Gate-Body Leakage Current, Reverse        | $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$                | --  | --   | -100 | nA                  |

### On Characteristics

|              |                                   |   |     |      |      |          |
|--------------|-----------------------------------|---|-----|------|------|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage            | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$           | 1.0 | --   | 2.0  | V        |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$          | --  | 0.22 | 0.28 | $\Omega$ |
|              |                                   | $V_{GS} = 5\text{ V}, I_D = 4.5\text{ A}$           | --  | 0.25 | 0.32 | $\Omega$ |
| $g_{FS}$     | Forward Transconductance          | $V_{DS} = 30\text{ V}, I_D = 4.5\text{ A}$ (Note 4) | --  | 11.6 | --   | S        |

### Dynamic Characteristics

|           |                              |  |    |     |      |    |
|-----------|------------------------------|--|----|-----|------|----|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1.0\text{ MHz}$ | -- | 830 | 1080 | pF |
| $C_{oss}$ | Output Capacitance           |  | -- | 120 | 155  | pF |
| $C_{rss}$ | Reverse Transfer Capacitance |  | -- | 17  | 22   | pF |

### Switching Characteristics

|              |                     |   |    |     |     |    |
|--------------|---------------------|---|----|-----|-----|----|
| $t_{d(on)}$  | Turn-On Delay Time  | $V_{DD} = 100\text{ V}, I_D = 11.6\text{ A},$<br>$R_G = 25\ \Omega$<br><br>(Note 4, 5)    | -- | 15  | 40  | ns |
| $t_r$        | Turn-On Rise Time   |   | -- | 190 | 390 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time |   | -- | 60  | 130 | ns |
| $t_f$        | Turn-Off Fall Time  |   | -- | 120 | 250 | ns |
| $Q_g$        | Total Gate Charge   | $V_{DS} = 160\text{ V}, I_D = 11.6\text{ A},$<br>$V_{GS} = 5\text{ V}$<br><br>(Note 4, 5) | -- | 16  | 21  | nC |
| $Q_{gs}$     | Gate-Source Charge  |   | -- | 2.8 | --  | nC |
| $Q_{gd}$     | Gate-Drain Charge   |   | -- | 7.6 | --  | nC |

### Drain-Source Diode Characteristics and Maximum Ratings

|          |   |   |    |      |     |               |
|----------|---|---|----|------|-----|---------------|
| $I_S$    | Maximum Continuous Drain-Source Diode Forward Current | --  | -- | 9.0  | A   |               |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current     | --  | -- | 36   | A   |               |
| $V_{SD}$ | Drain-Source Diode Forward Voltage                    | $V_{GS} = 0\text{ V}, I_S = 9.0\text{ A}$       | -- | --   | 1.5 | V             |
| $t_{rr}$ | Reverse Recovery Time                                 | $V_{GS} = 0\text{ V}, I_S = 11.6\text{ A},$     | -- | 128  | --  | ns            |
| $Q_{rr}$ | Reverse Recovery Charge                               | $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4) | -- | 0.56 | --  | $\mu\text{C}$ |

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 3.9\text{ mH}, I_{AS} = 9.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 11.6\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

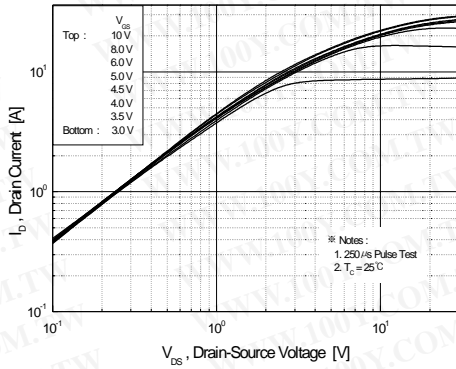


Figure 1. On-Region Characteristics

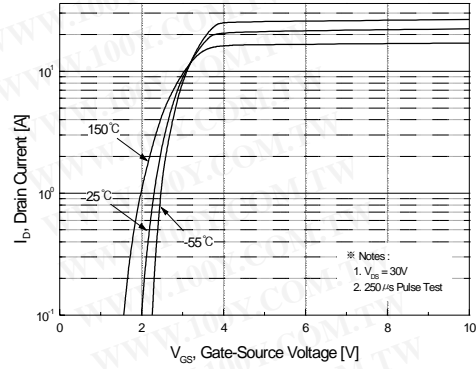


Figure 2. Transfer Characteristics

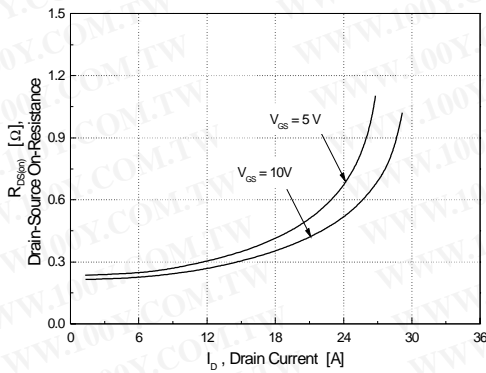


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

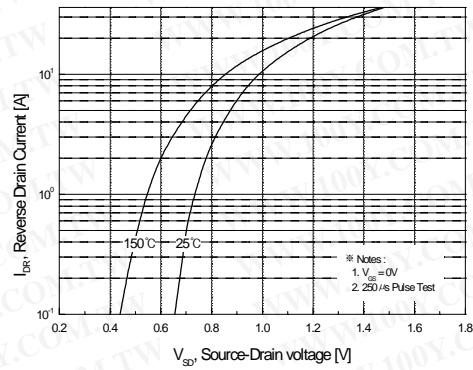


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

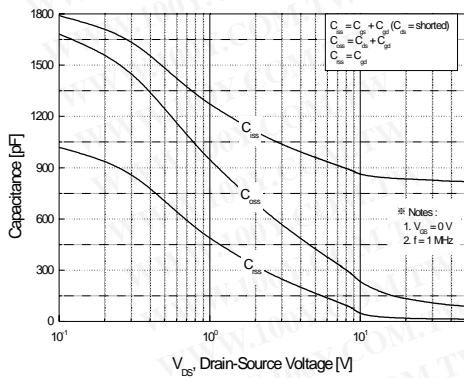


Figure 5. Capacitance Characteristics

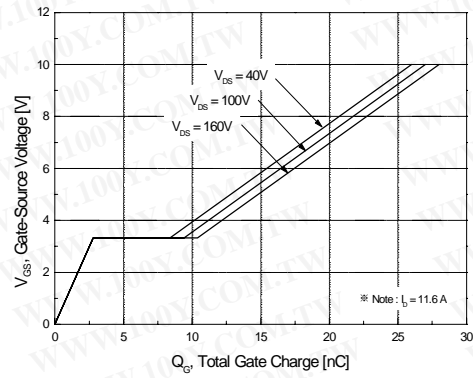
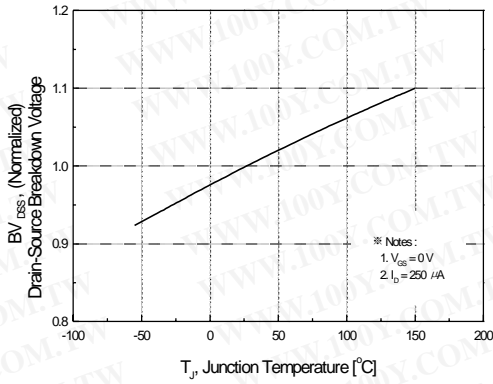
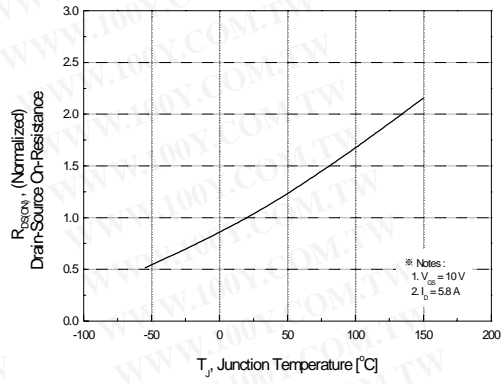


Figure 6. Gate Charge Characteristics

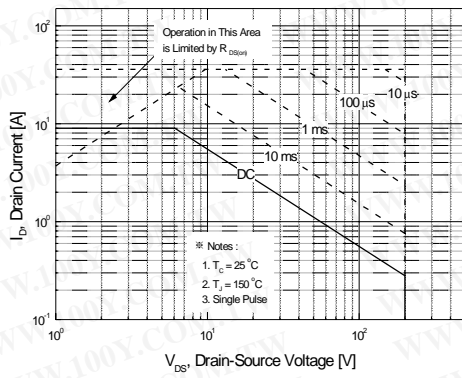
**Typical Characteristics** (Continued)



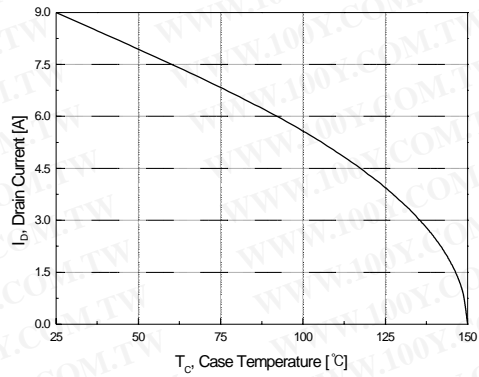
**Figure 7. Breakdown Voltage Variation vs. Temperature**



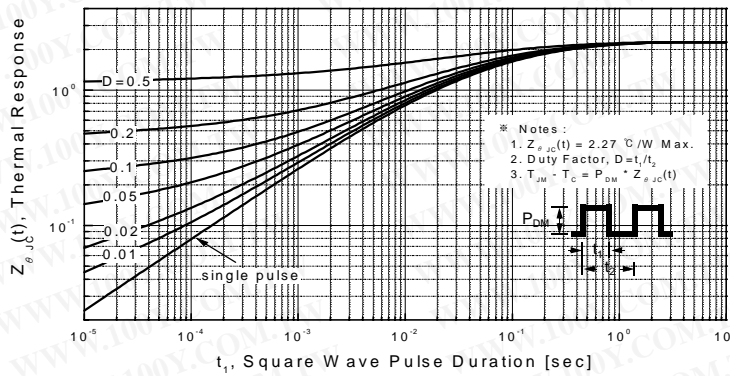
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

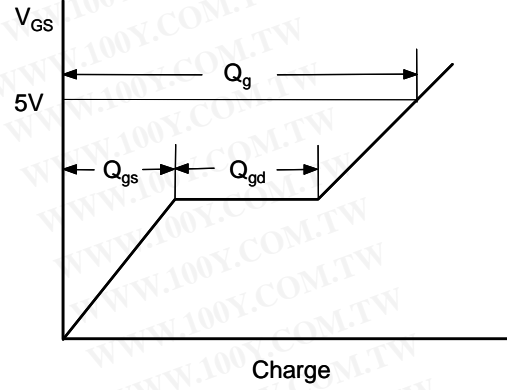
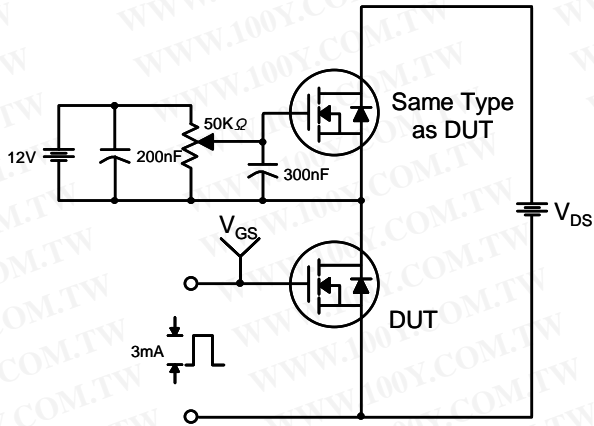


**Figure 10. Maximum Drain Current vs. Case Temperature**

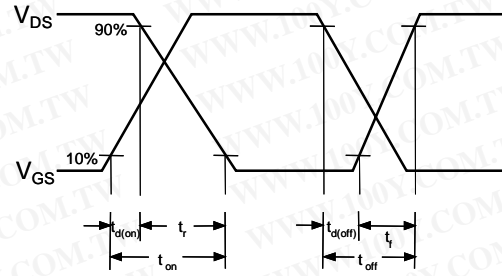
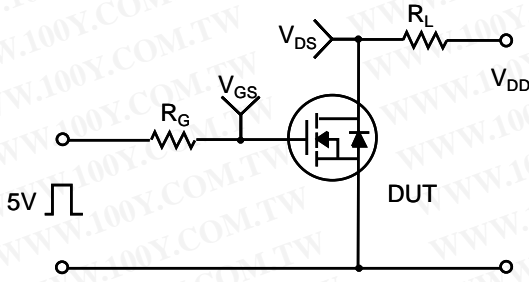


**Figure 11. Transient Thermal Response Curve**

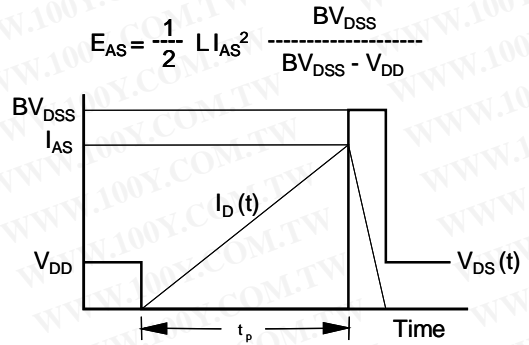
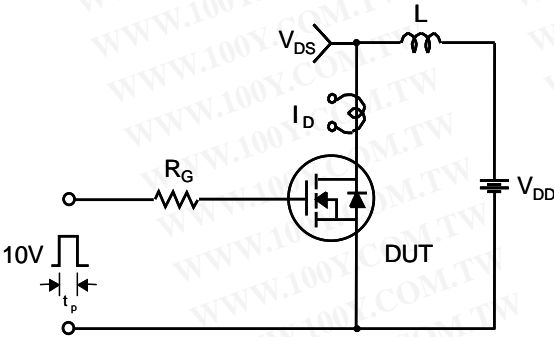
**Gate Charge Test Circuit & Waveform**



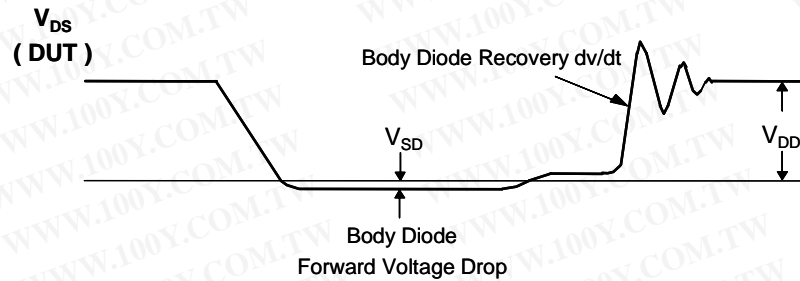
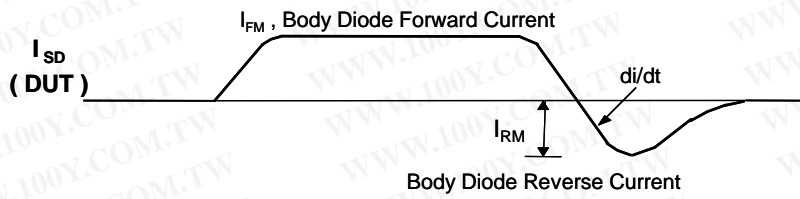
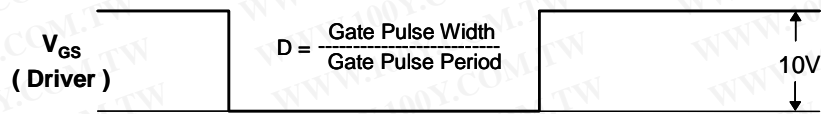
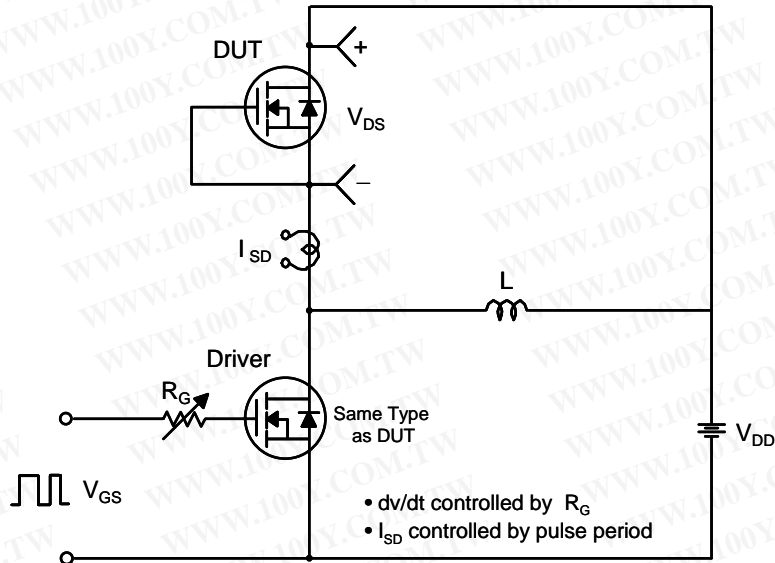
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

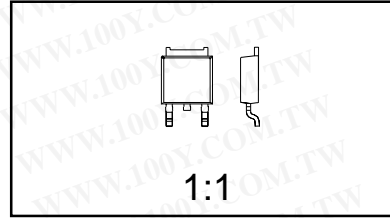
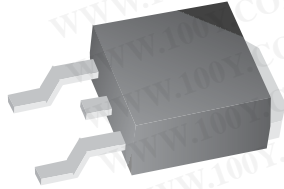


Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Mechanical Dimensions**

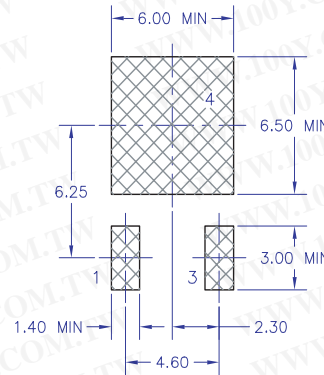
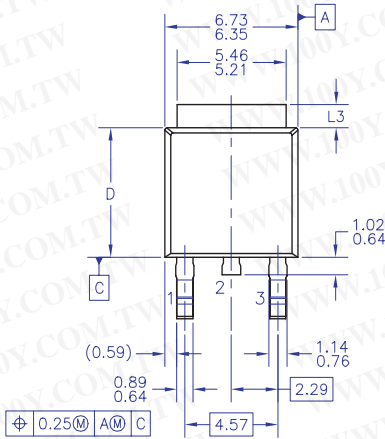
**TO-252 (DPAK) (FS PKG Code 36)**



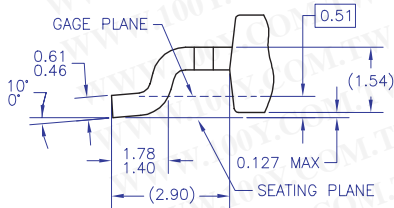
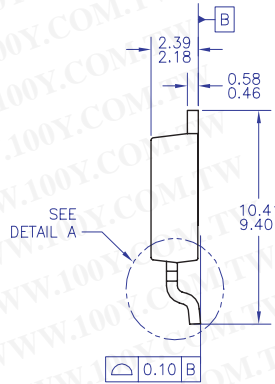
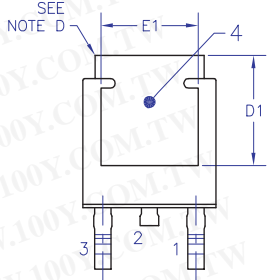
Scale 1:1 on letter size paper

Dimensions shown below are in millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



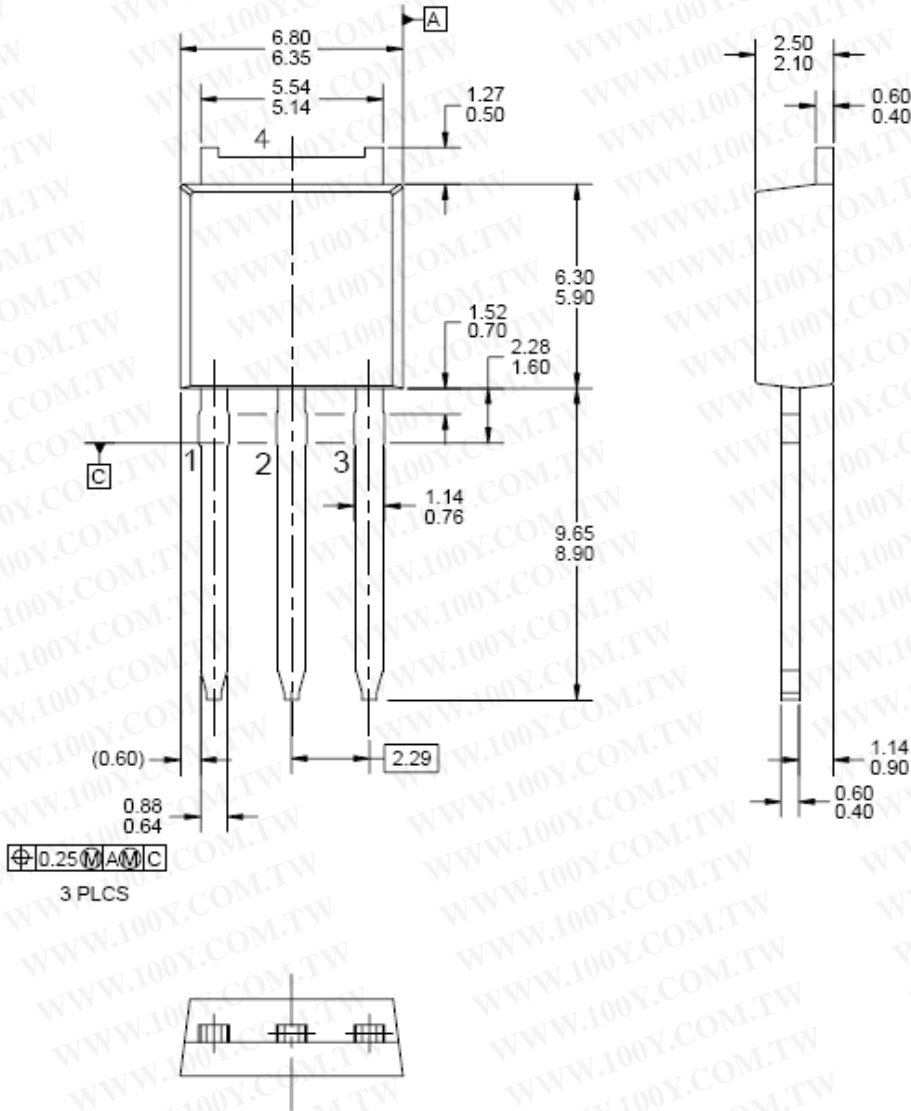
DETAIL A  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:

|    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |

Mechanical Dimensions

I - PAK






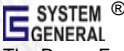


Dimensions in Millimeters



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| Datasheet Identification | Product Status        | Definition  |
|--------------------------|-----------------------|---|
| Advance Information      | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.   |
| Preliminary              | First Production      | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production       | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.   |
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