TVS Diode

Transient Voltage Suppressor Diodes

ESD200-B1-CSP0201

Low Clamping Voltage TVS Diode in a Thin 0201 Chip Scale Package

ESD200-B1-CSP0201

Data Sheet

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Revision 1.0, 2013-05-21	
All	Status change to final

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Last Trademarks Update 2010-10-26

1 Low Clamping Voltage TVS Diode in a Thin 0201 Chip Scale Package

1.1 Features

- ESD / Transient protection of susceptible I/O lines to:
  - **IEC61000-4-2 (ESD): ±16 kV (air/contact discharge)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs))**
- Low clamping voltage
- Low dynamic resistance: R_{DYN} **≤ 0.2 Ω typ**.
- Supports applications with signal voltage between -5.5 V and 5.5 V max.
- Line capacitance: C_L **= 6.5 pF**
- Minimized overshoot due to extremely low parasitic inductance of chip scale package
- Miniature form factor (XY) = 0201 (0.58 mm x 0.28 mm)
- Thin 0.15 mm package thickness to allow direct integration into modules
- Optimized assembly: its bidirectional and symmetric I/V characteristics allow placement on the PCB with no danger of polarity orientation issues

RoHS

1.2 Application Examples

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

1.3 Product Description

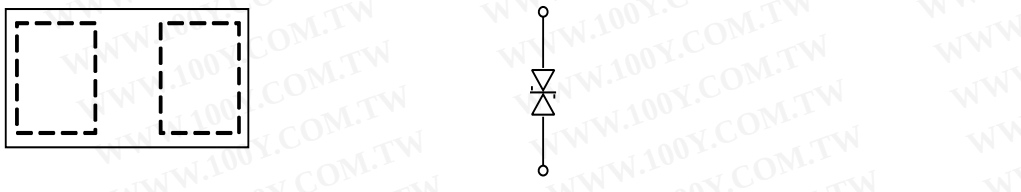

Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD200-B1-CSP0201	WLL-2-1	1 line, bi-directional	A[1)]

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Characteristics

2.1 Maximum Ratings

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD[1)] Contact discharge Air discharge	V_{ESD}	 -16 -16	 - -	 16 16	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	-	3	A
Operating temperature range	T_{OP}	-40	-	125	°C
Storage temperature	T_{stg}	-65	-	150	°C

1) V_{ESD} according to IEC61000-4-2 (R = 330, C = 150 pF discharge network)

2) I_{PP} according to IEC61000-4-5 (t_p = 8/20 µs)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

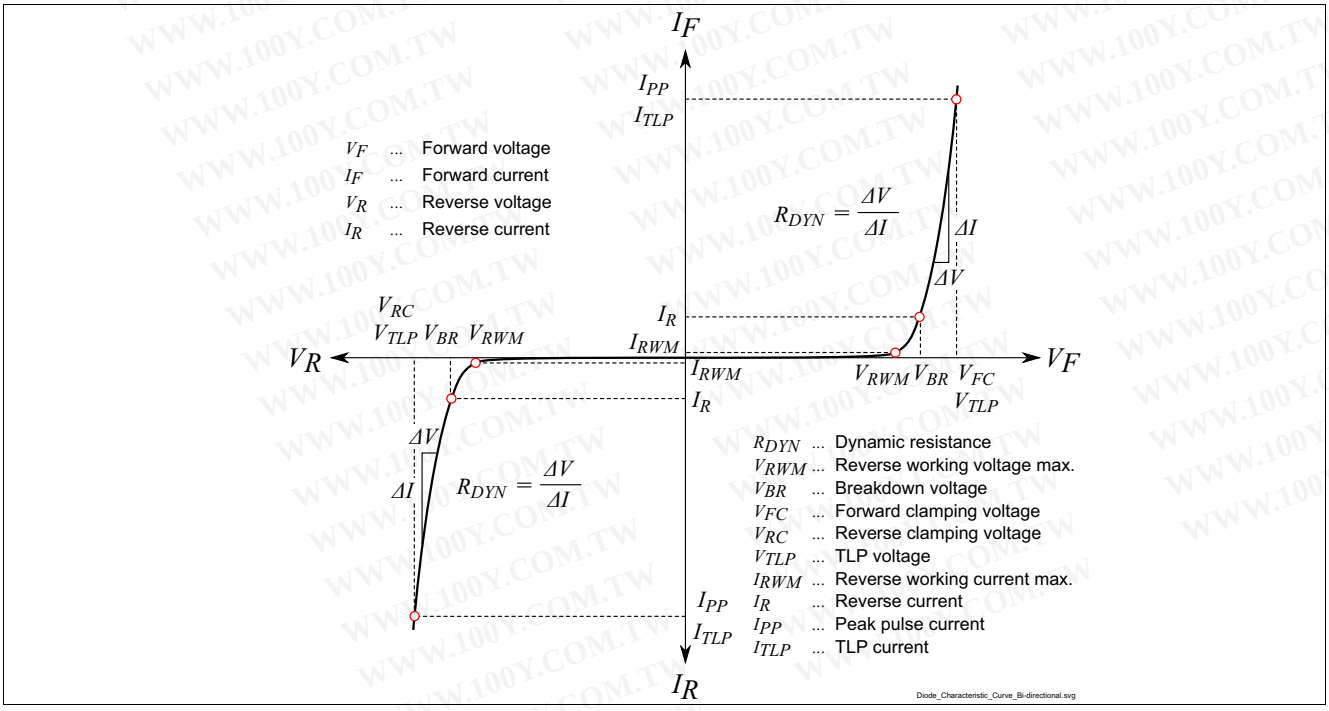

Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	-	5.5	V	
Breakdown voltage	V_{BR}	6	-	10	V	I_{BR} = 1 mA
Reverse current	I_R	-	0.1	100	nA	V_R = 5.5 V

Table 2-3 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L		6.5		pF	V_R = 0 V, f = 1 MHz

Table 2-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	-	12	-	V	V_{ESD} = 8 kV contact discharge
Clamping voltage[2)]		- -	10 13	- -		I_{TLP} = 1 A I_{TLP} = 16 A
Clamping voltage[3)]		- -	10 12.5	- -		I_{PP} = 1 A I_{PP} = 3 A
Dynamic resistance[2)]	R_{DYN}	-	0.2	-	Ω	

1) V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)

2) ANSI/ESDSTM5.5.1-Electrostatistic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} average window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 2.5 A and I_{TLP2} = 17 A. Please refer to Application Note AN210[1]

3) I_{PP} according to IEC61000-4-5 (t_p = 8/20 µs)

3 Typical Characteristics

Curves specified at T_A = 25 °C, unless otherwise specified

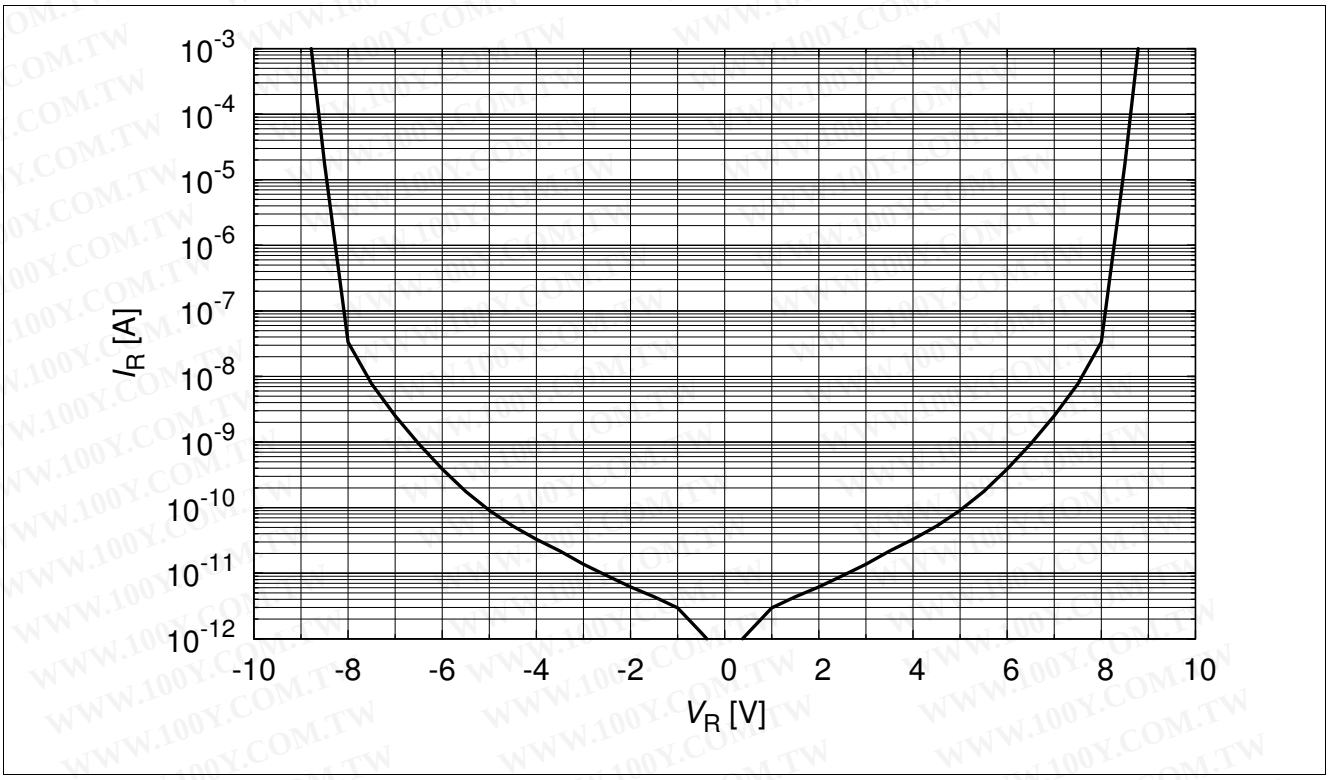

Figure 3-1 Reverse current: $I_R = f(V_R)$

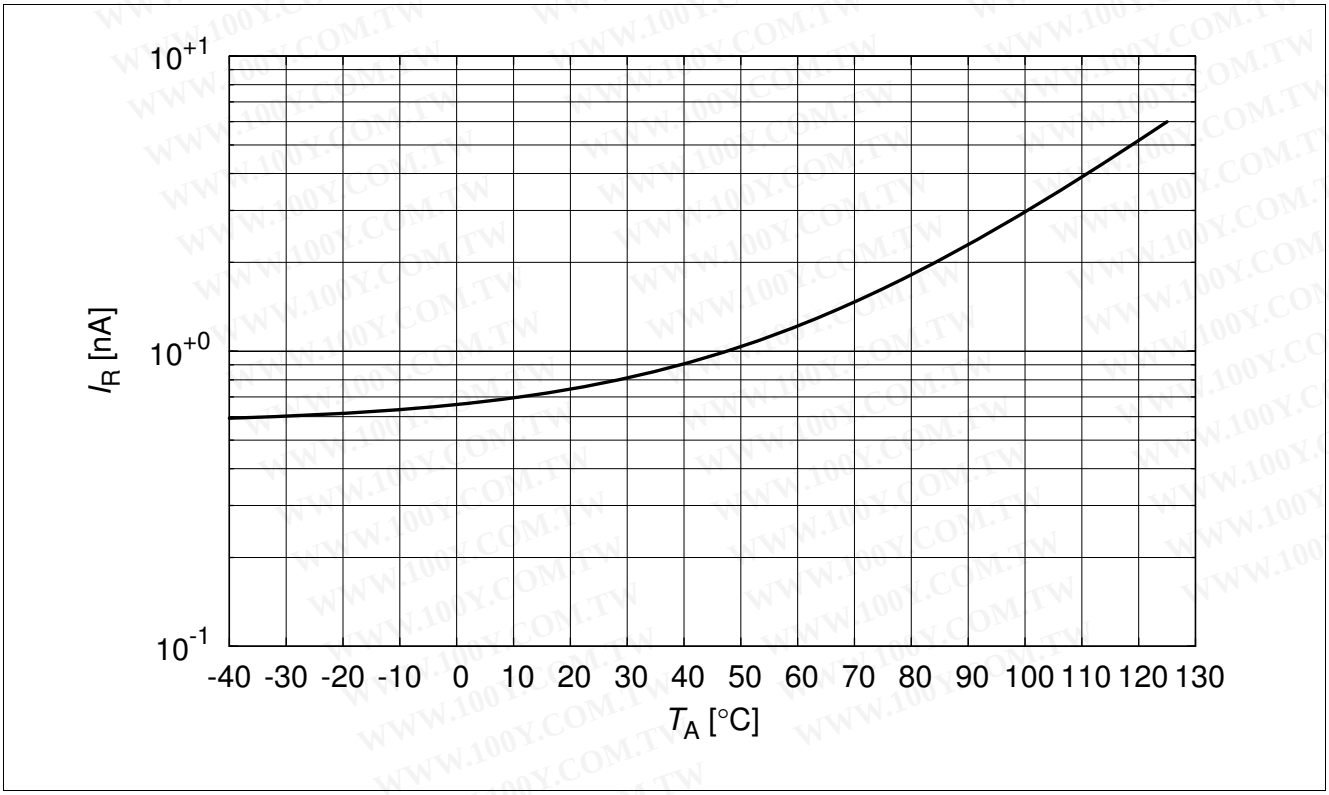

Figure 3-2 Reverse current: $I_R = f(T_A)$, V_R = 5.5 V

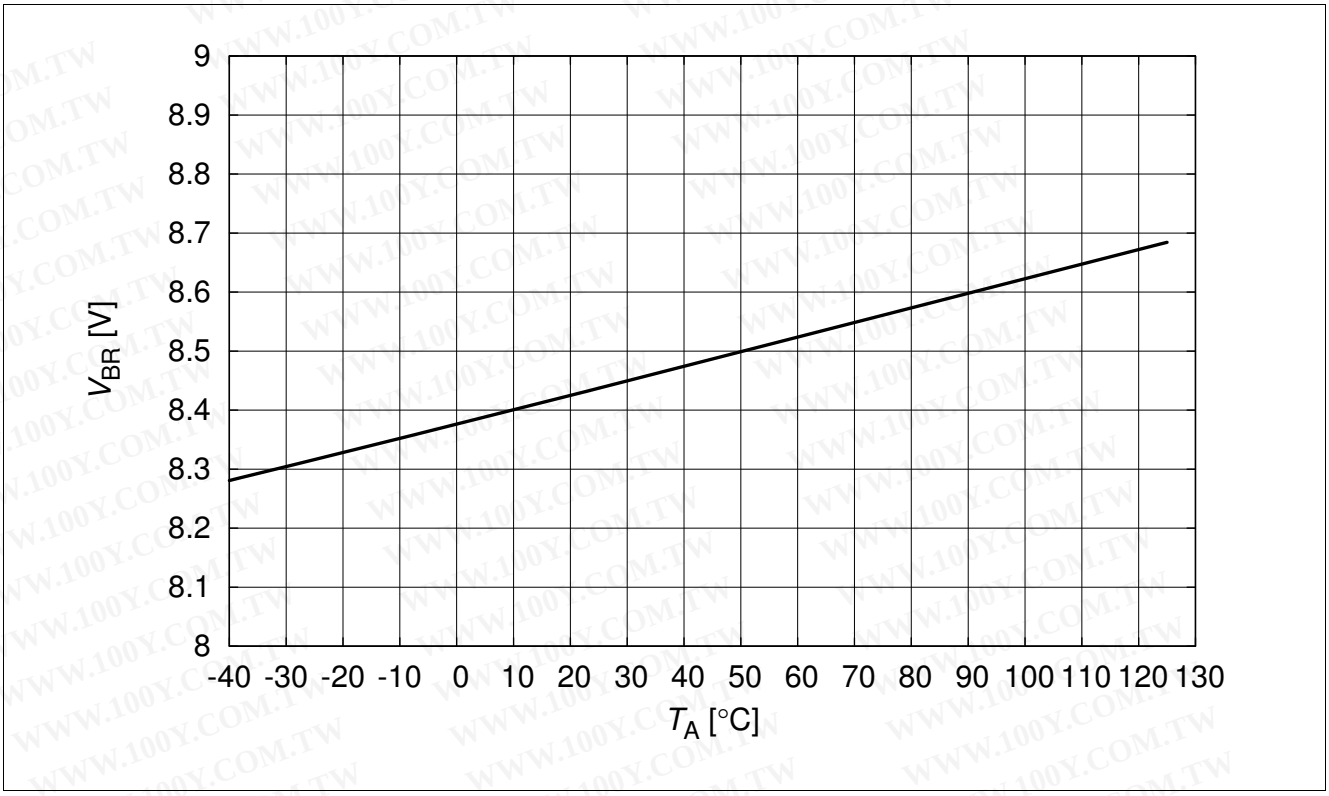

Figure 3-3 Reverse voltage: $V_{BR} = f(T_A)$, I_R = 1 mA

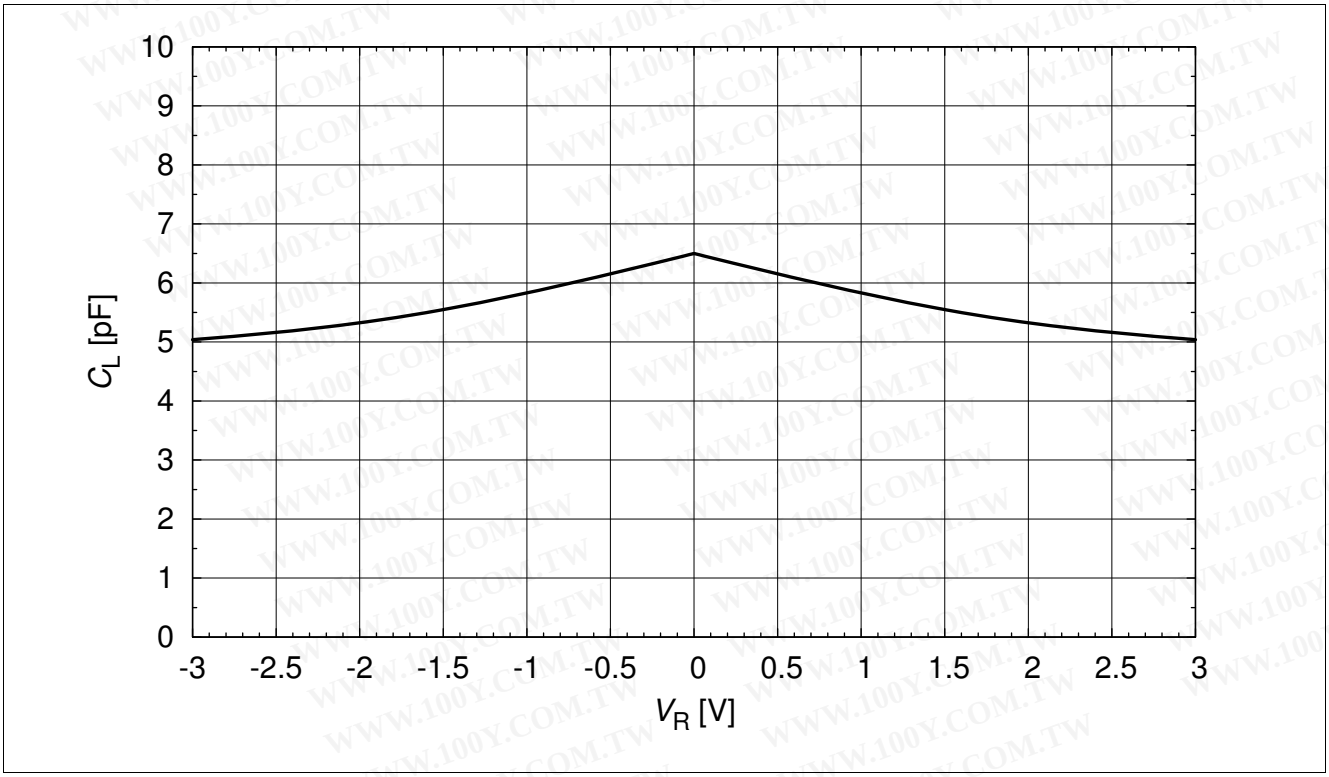

Figure 3-4 Line capacitance: $C_L = f(V_R)$, f = 1 MHz

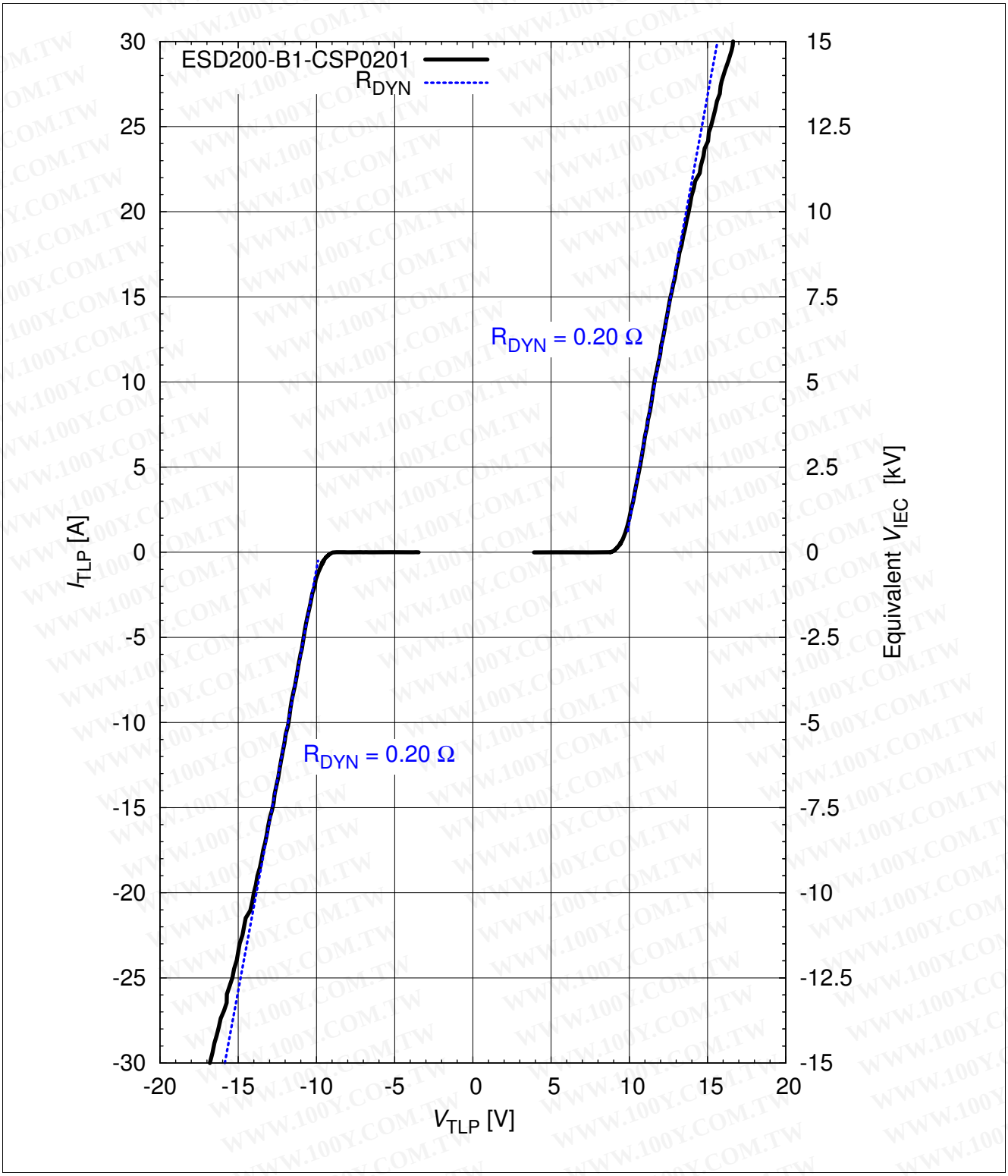

Figure 3-5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESDSTM5.5.1-Electrostatistic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} average window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 2.5 A and I_{TLP2} = 17 A. Please refer to Application Note AN210[1]

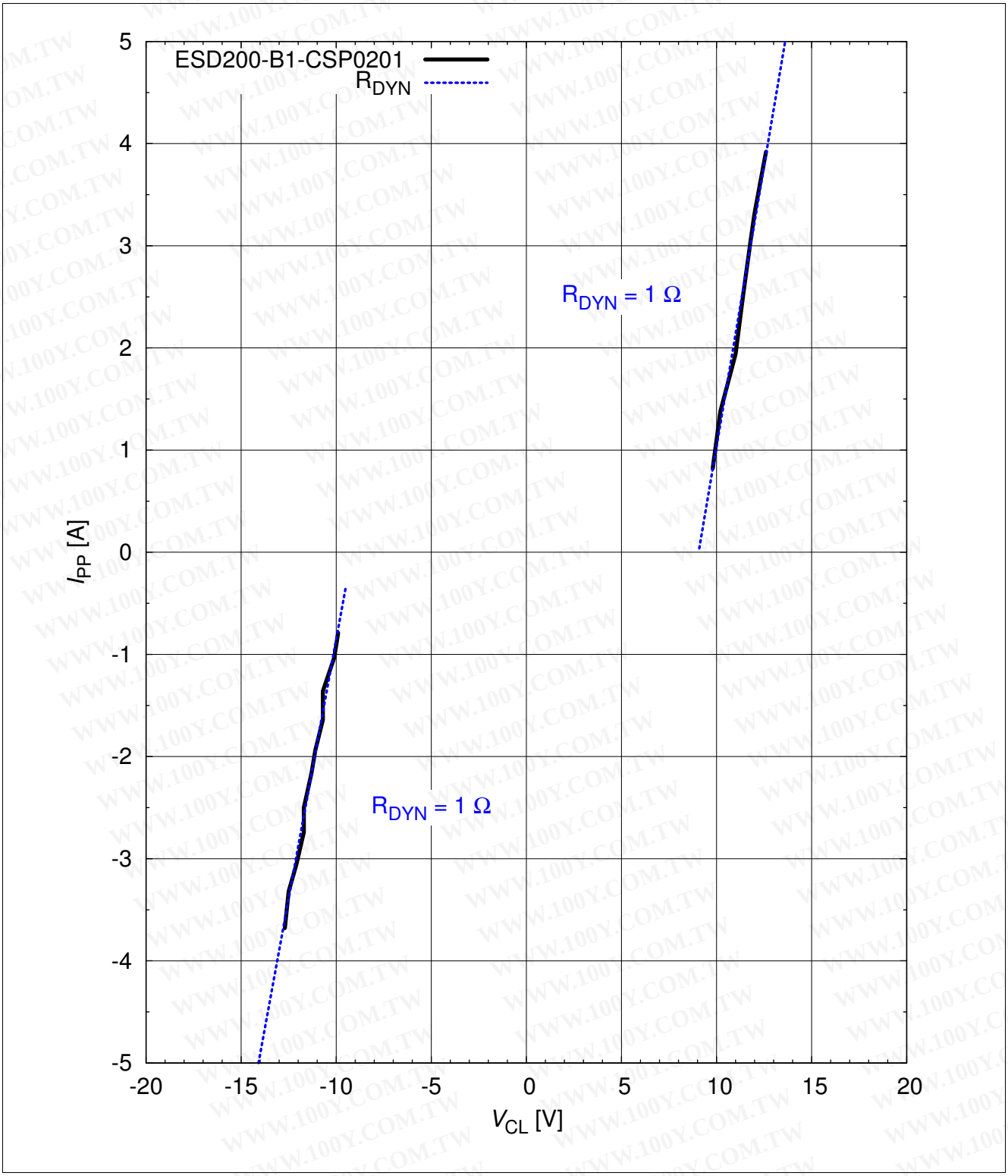

Figure 3-6 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

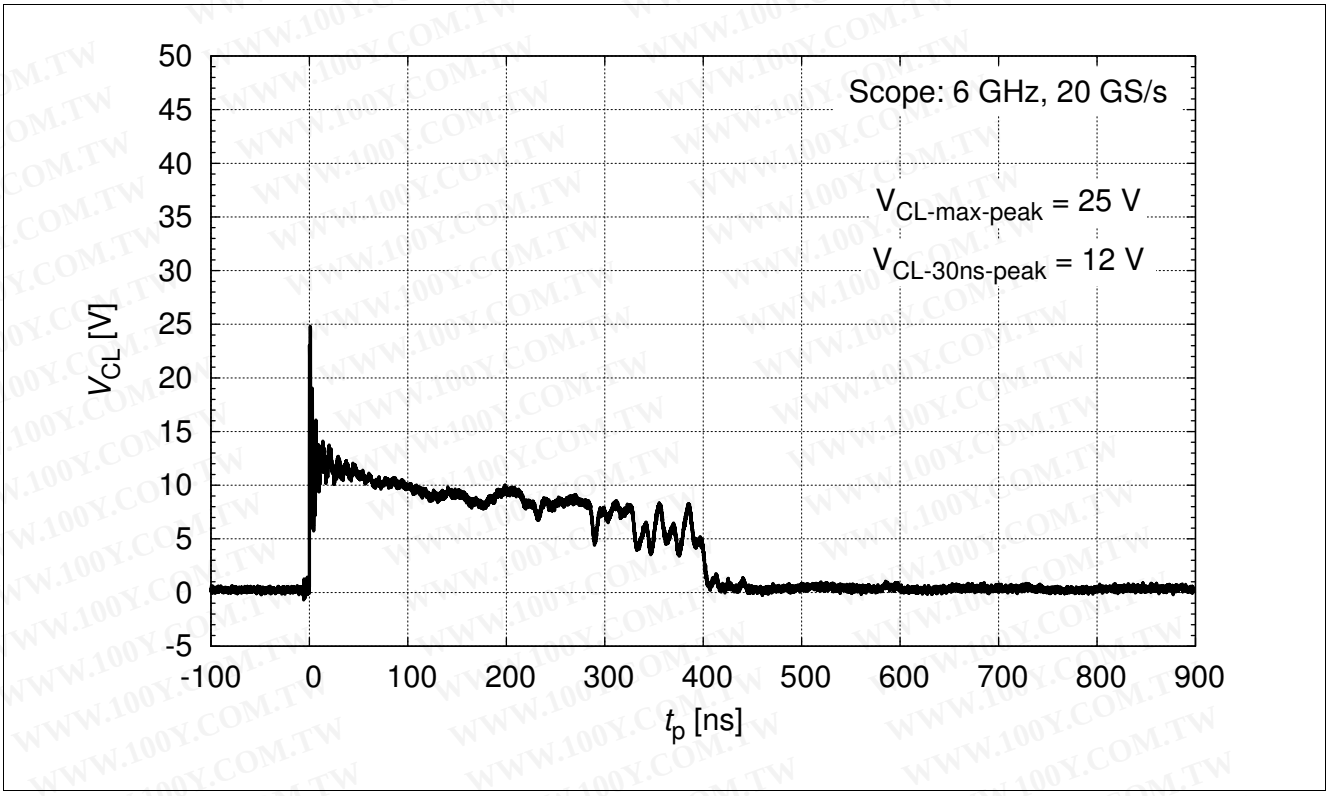

Figure 3-7 IEC61000-4-2: $V_{CL} = f(t)$, +8 kV pulse

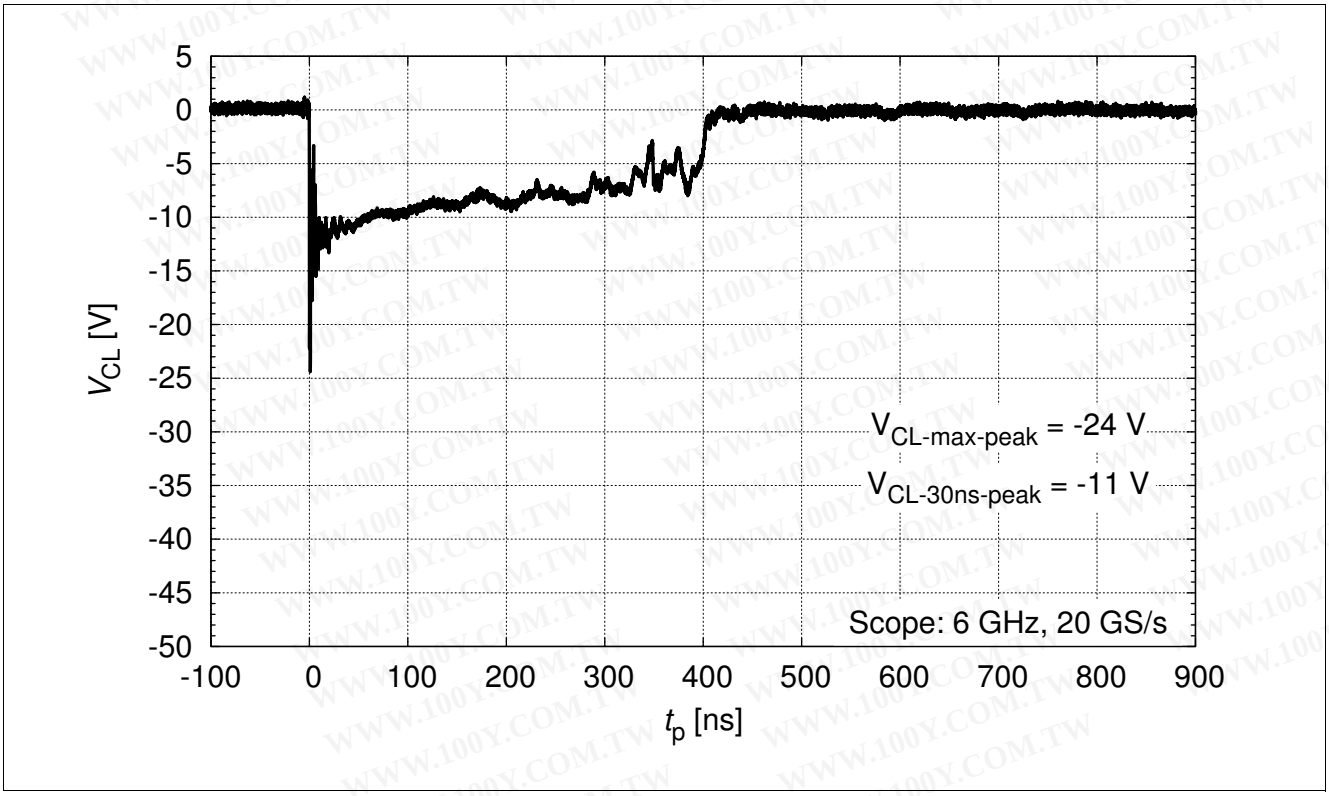

Figure 3-8 IEC61000-4-2: $V_{CL} = f(t)$, -8 kV pulse

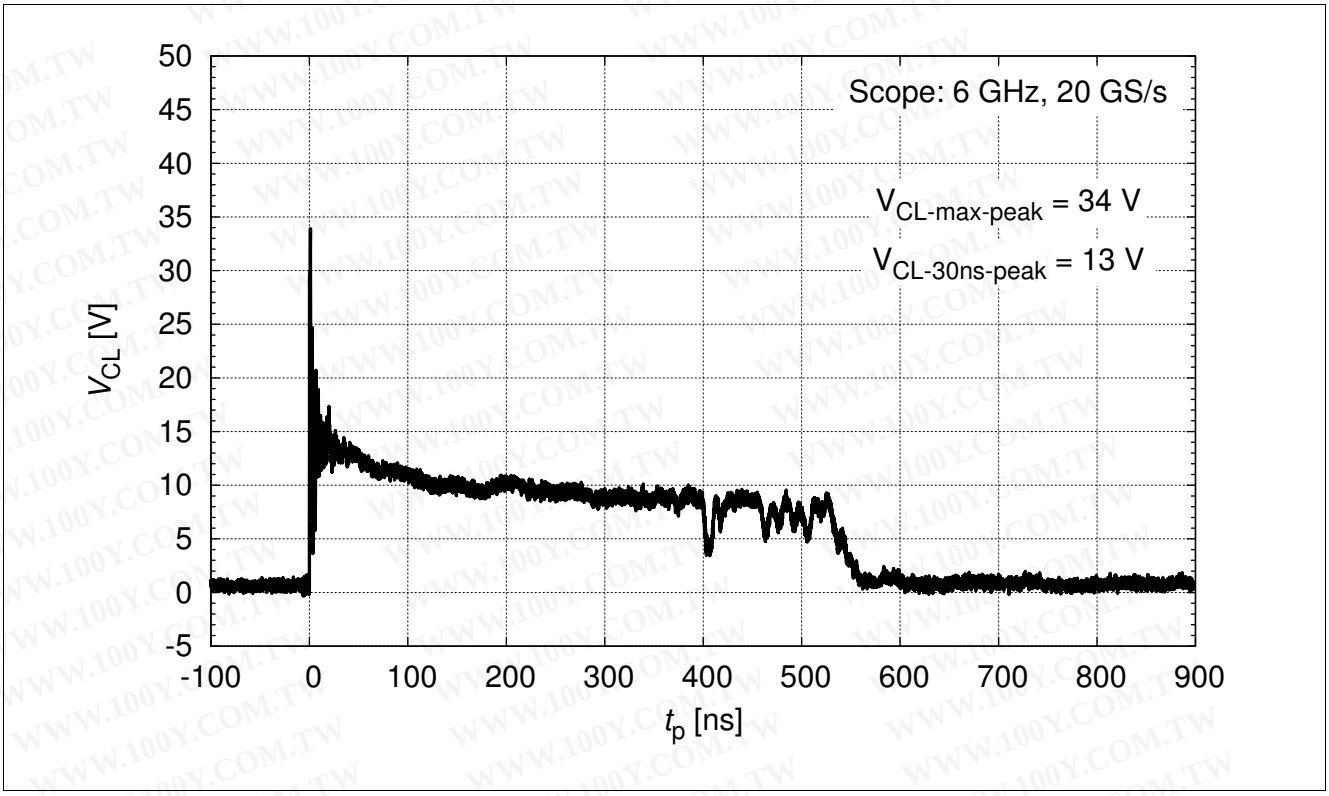

Figure 3-9 IEC61000-4-2: $V_{CL} = f(t)$, +15 kV pulse

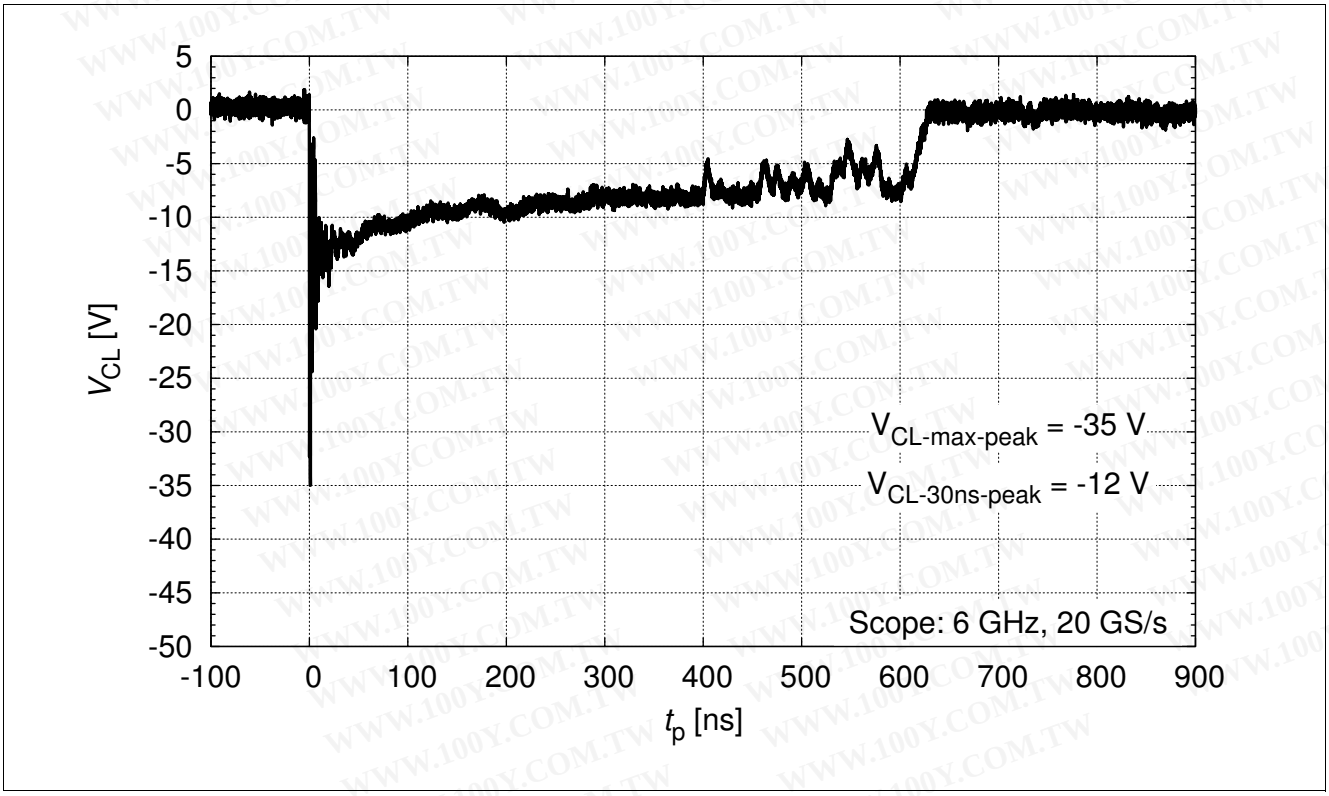

Figure 3-10 IEC61000-4-2: $V_{CL} = f(t)$, -15 kV pulse

4 Application Information

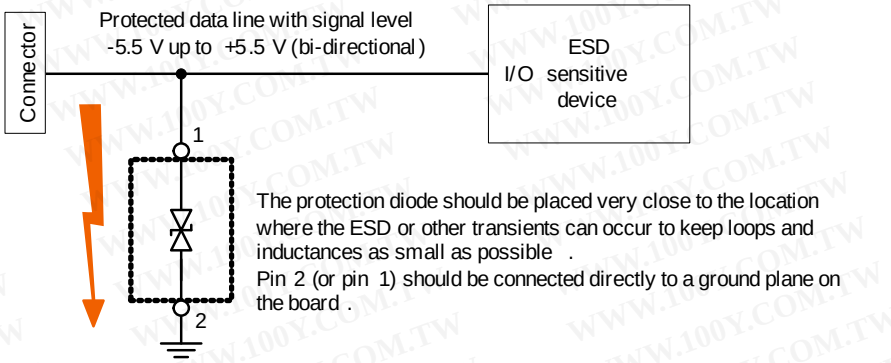

Figure 4-1 Single line, bi-directional ESD / Transient protection

5 Package

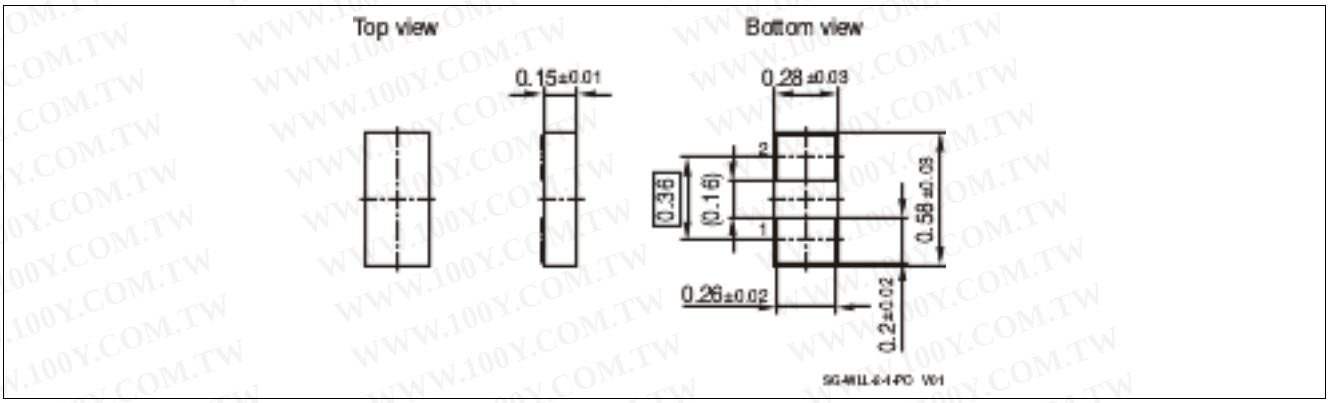

Figure 5-1 WLL-2-1 Package outline (dimension in mm)

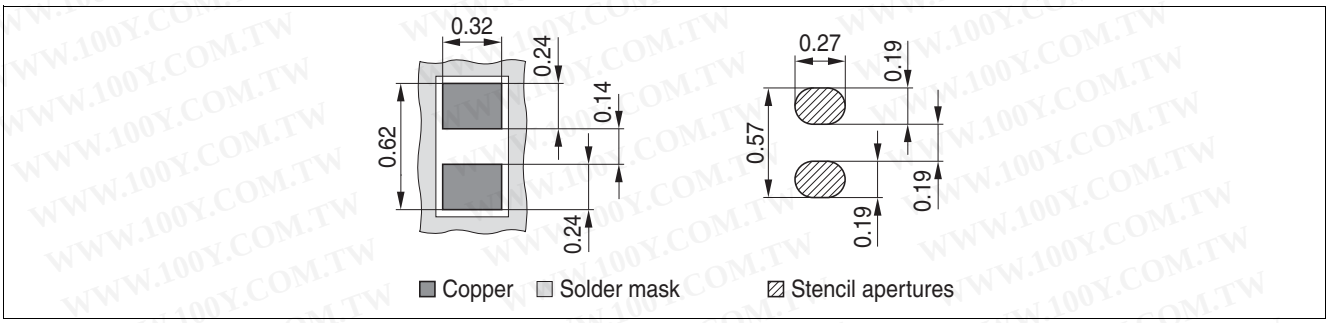

Figure 5-2 WLL-2-1 Footprint (dimension in mm)

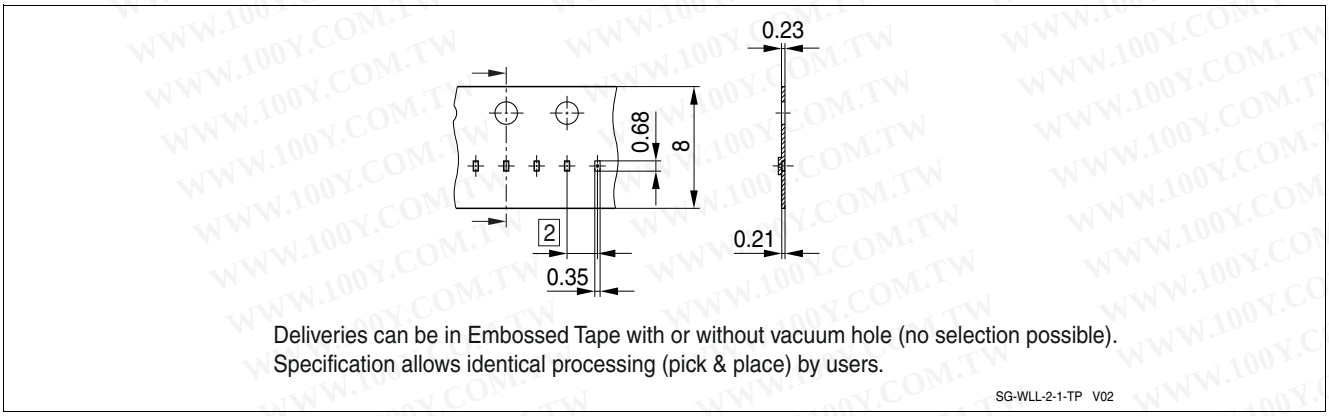

Figure 5-3 WLL-2-1 Packing (dimension in mm)

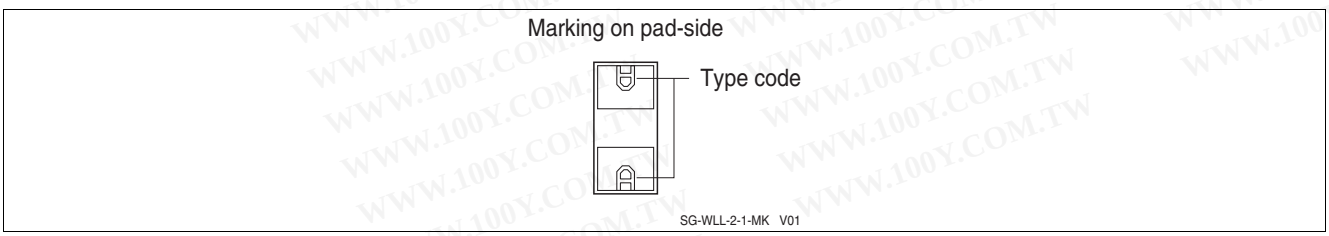

Figure 5-4 WLL-2-1 Marking (example)

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology