

IR2011(S) & (PbF)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational up to +200V
Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Independent low and high side channels
- Input logicHIN/LIN active high
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- CMOS Schmitt-triggered inputs with pull-down
- Matched propagation delay for both channels
- Also available LEAD-FREE (PbF)

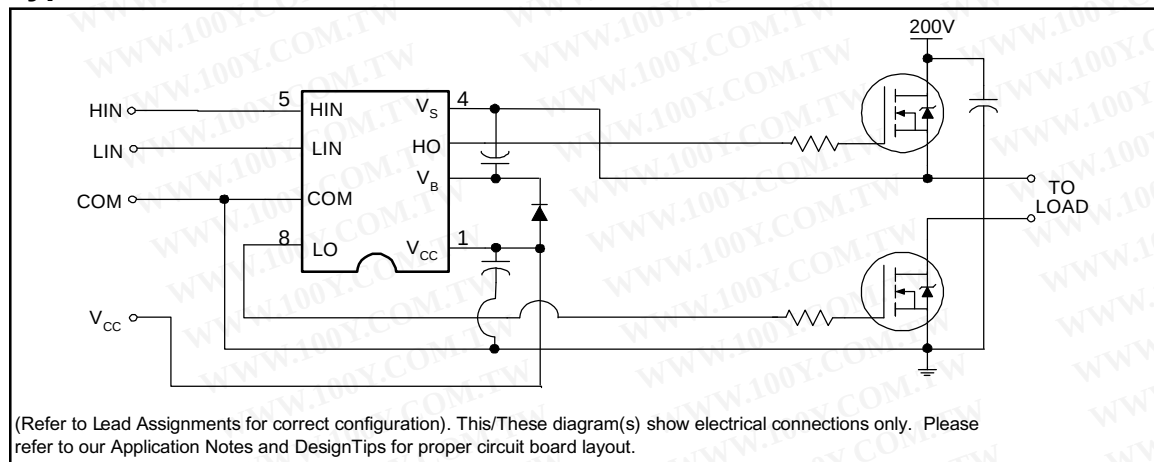
Applications

- Audio Class D amplifiers
- High power DC-DC SMPS converters
- Other high frequency applications

Description

The IR2011 is a high power, high speed power MOSFET driver with independent high and low side referenced output channels, ideal for Audio Class D and DC-DC converter applications. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.0V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 volts. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction.

Typical Connection



Product Summary

V_{OFFSET}	200V max.
$I_{\text{O+/-}}$	1.0A /1.0A typ.
V_{OUT}	10 - 20V
$t_{\text{on/off}}$	80 & 60 ns typ.
Delay Matching	20 ns max.

Packages



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	225	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN & LIN)	-0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$ (8-lead DIP)	—	1.0	W
	(8-lead SOIC)	—	0.625	
R_{THJA}	Thermal resistance, junction to ambient (8-lead DIP)	—	125	$^\circ\text{C/W}$
	(8-lead SOIC)	—	200	
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. The V_S and COM offset ratings are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	COM	5.5	
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +200V. Logic state held for V_S of -4V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified. Figure 1 shows the timing definitions.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t _{on}	Turn-on propagation delay	—	80	—	ns	V _S = 0V
t _{off}	Turn-off propagation delay	—	75	—		V _S = 200V
t _r	Turn-on rise time	—	35	50		
t _f	Turn-off fall time	—	20	35		
DM1	Turn-on delay matching t _{on} (H) - t _{on} (L)	—	—	20		
DM2	Turn-off delay matching t _{off} (H) - t _{off} (L)	—	—	20		

Static Electrical Characteristics

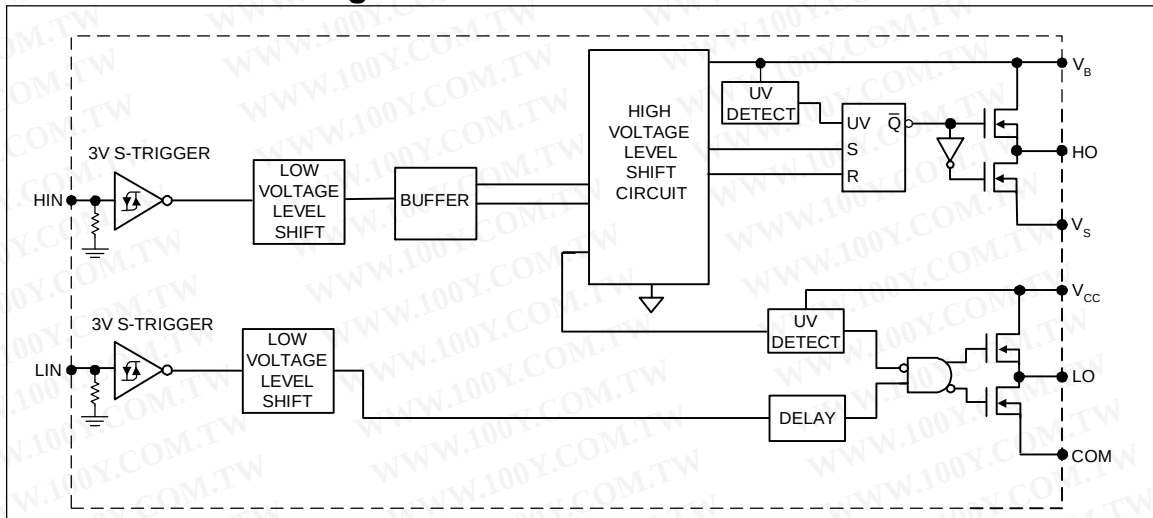
V_{BIAS} (V_{CC}, V_{BS}) = 15V, and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{IH}	Logic "1" input voltage	2.2	—	—	V	V _{CC} = 10V - 20V
V _{IL}	Logic "0" input voltage	—	—	0.7		
V _{OH}	High level output voltage, V _{BIAS} - V _O	—	—	2.0		I _O = 0A
V _{OL}	Low level output voltage, V _O	—	—	0.2		20mA
I _{LK}	Offset supply leakage current	—	—	50	μA	V _B =V _S = 200V
I _{QBS}	Quiescent V _{BS} supply current	—	90	210		V _{IN} = 0V or 3.3V
I _{QCC}	Quiescent V _{CC} supply current	—	140	230		V _{IN} = 0V or 3.3V
I _{IN+}	Logic "1" input bias current	—	7.0	20		V _{IN} = 3.3V
I _{IN-}	Logic "0" input bias current	—	—	1.0		V _{IN} = 0V
V _{BSUV+}	V _{BS} supply undervoltage positive going threshold	8.2	9.0	9.8	V	
V _{BSUV-}	V _{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V _{CCUV+}	V _{CC} supply undervoltage positive going threshold	8.2	9.0	9.8		
V _{CCUV-}	V _{CC} supply undervoltage negative going threshold	7.4	8.2	9.0		
I _{O+}	Output high short circuit pulsed current	—	1.0	—	A	V _O = 0V, PW ≤ 10 μs
I _{O-}	Output low short circuit pulsed current	—	1.0	—		V _O = 15V, PW ≤ 10 μs

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Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

8-Lead PDIP	8-Lead SOIC
IR2011	IR2011S
Part Number	

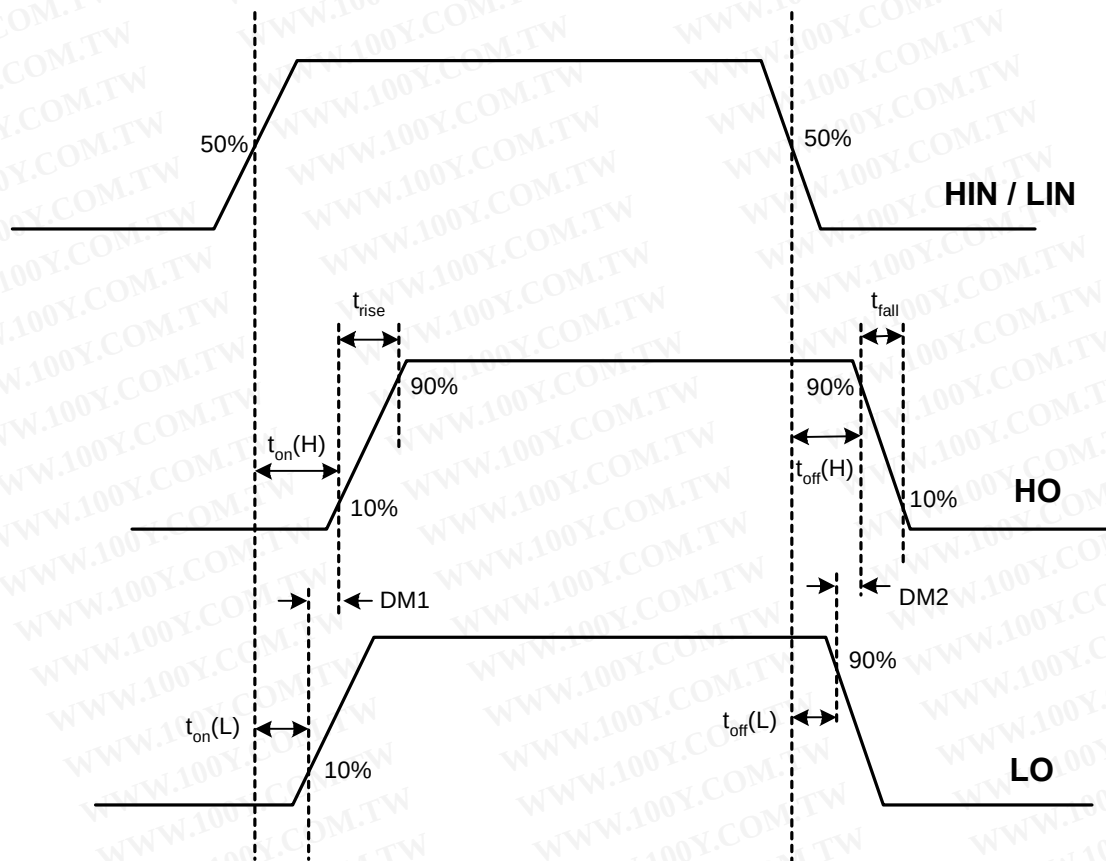


Figure 1. Timing Diagram

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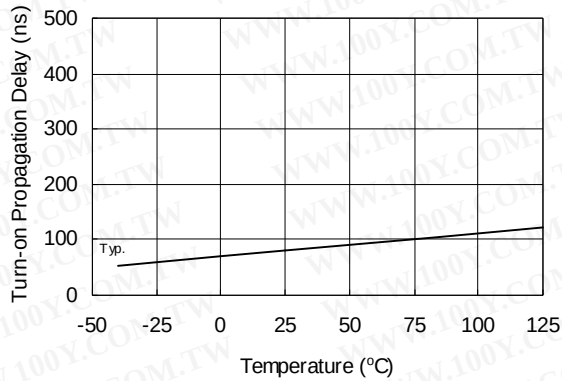


Figure 2A. Turn-on Propagation Delay vs. Temperature

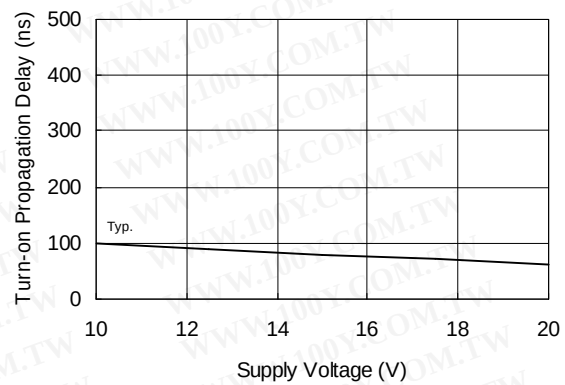


Figure 2B. Turn-on Propagation Delay vs. Supply Voltage

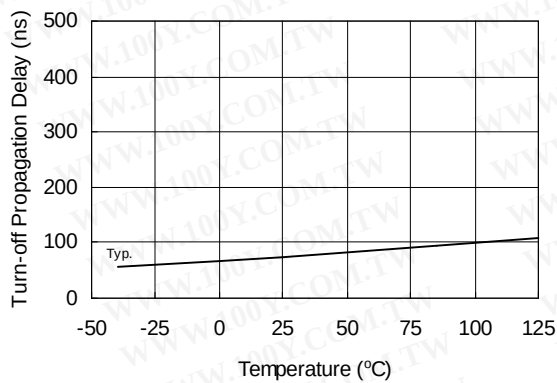


Figure 3A. Turn-off Propagation Delay vs. Temperature

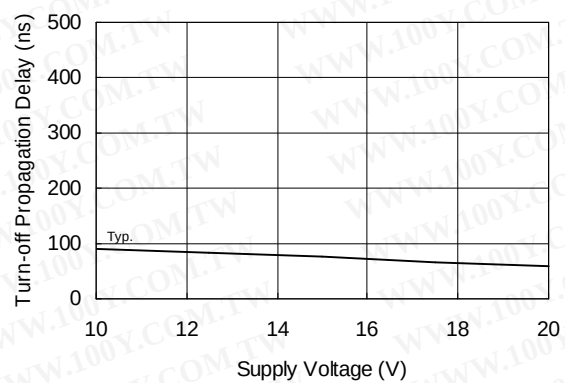


Figure 3B. Turn-off Propagation Delay vs. Supply Voltage

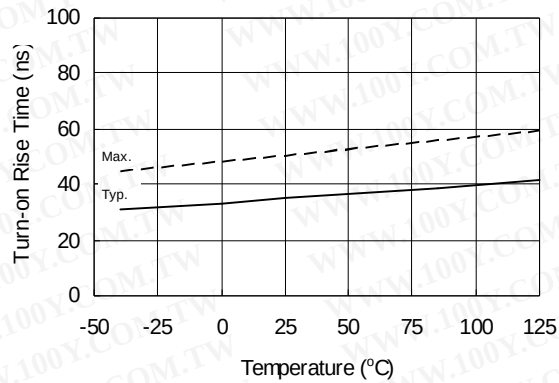


Figure 4A. Turn-on Rise Time vs. Temperature

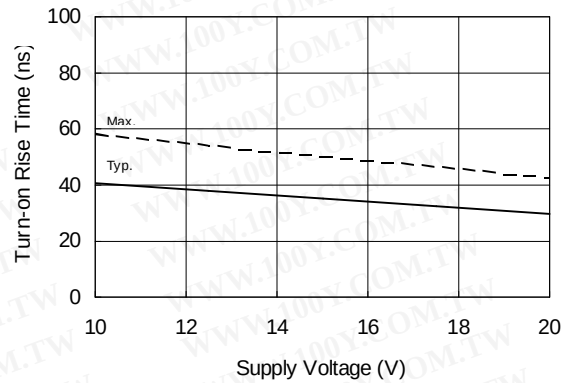


Figure 4B. Turn-on Rise Time vs. Supply Voltage

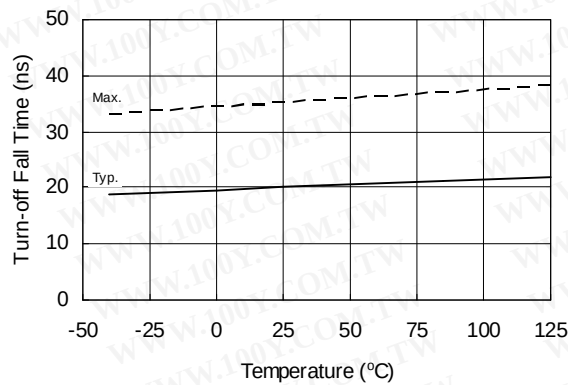


Figure 5A. Turn-off Fall Time vs. Temperature

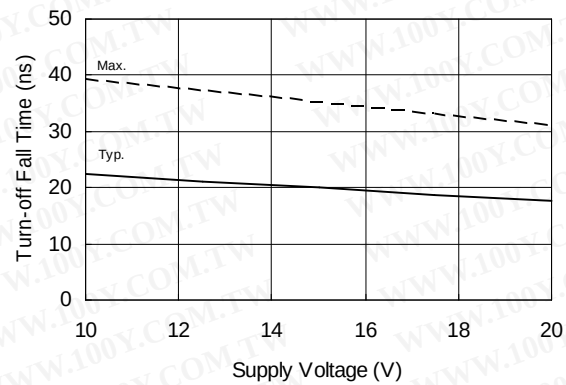


Figure 5B. Turn-off Fall Time vs. Supply Voltage

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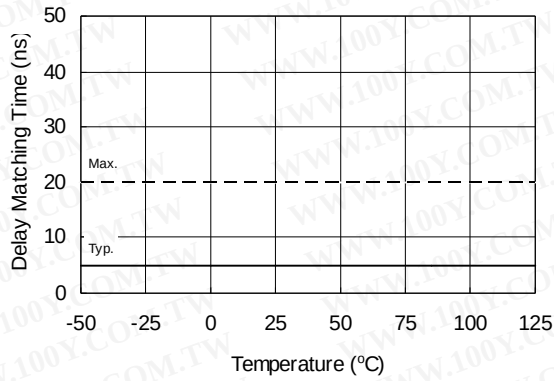


Figure 6A. Turn-on Delay Matching Time vs. Temperature

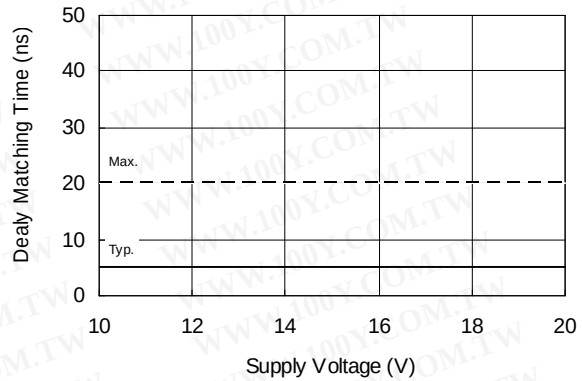


Figure 6B. Turn-on Delay Matching Time vs. Supply Voltage

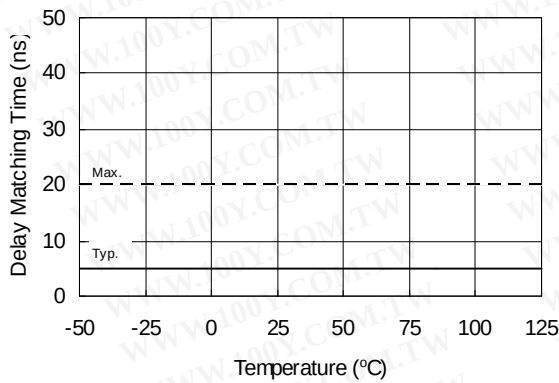


Figure 7A. Turn-off Delay Matching Time vs. Temperature

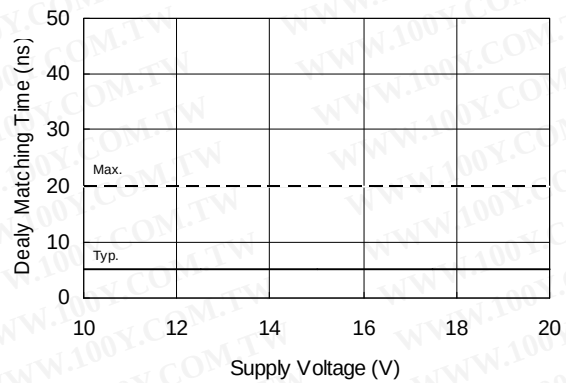


Figure 7B. Turn-off Delay Matching Time vs. Supply Voltage

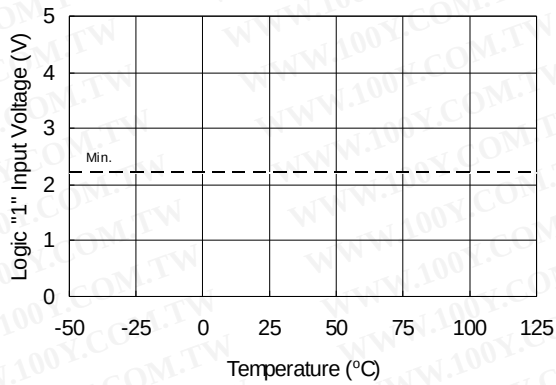


Figure 8A. Logic "1" Input Voltage vs. Temperature

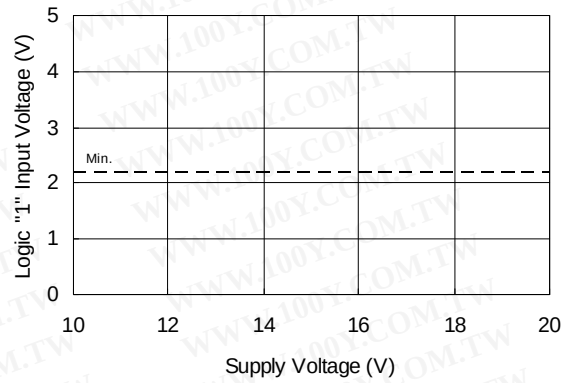


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

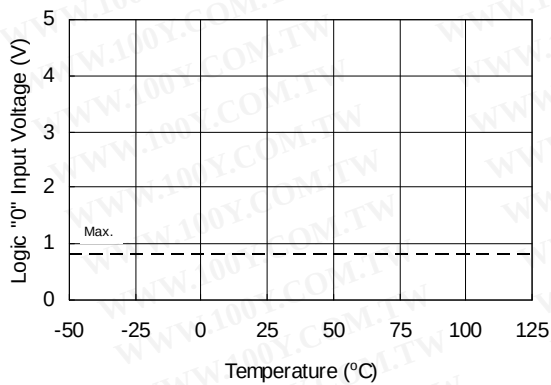


Figure 9A. Logic "0" Input Voltage vs. Temperature

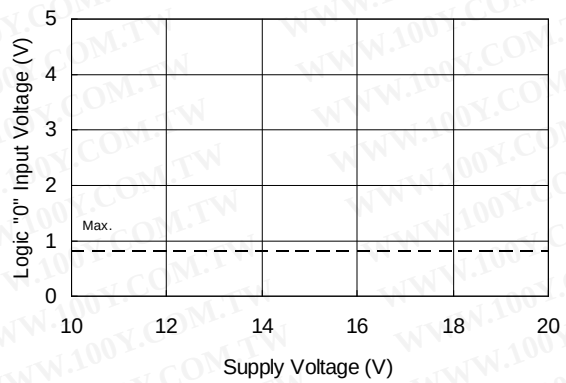


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

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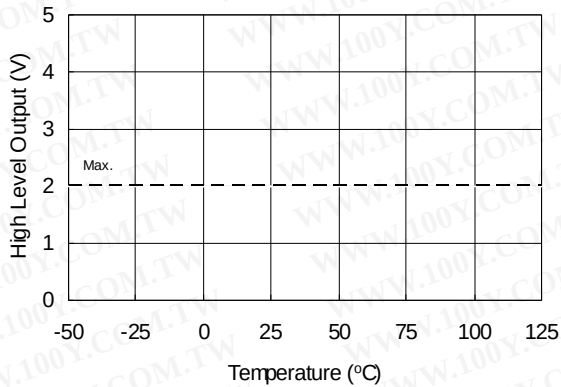


Figure 10A. High Level Output vs. Temperature

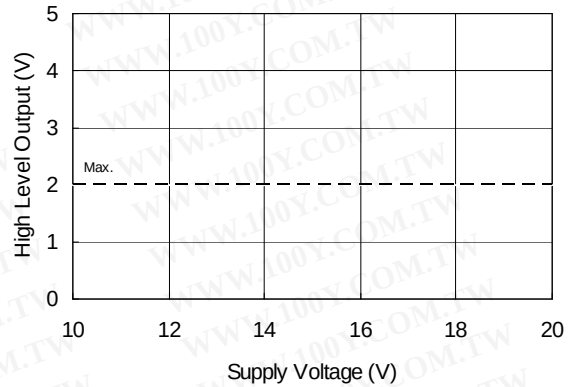


Figure 10B. High Level Output vs. Supply Voltage

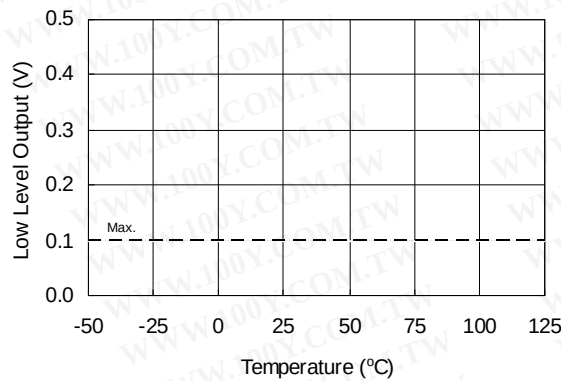


Figure 11A. Low Level Output vs. Temperature

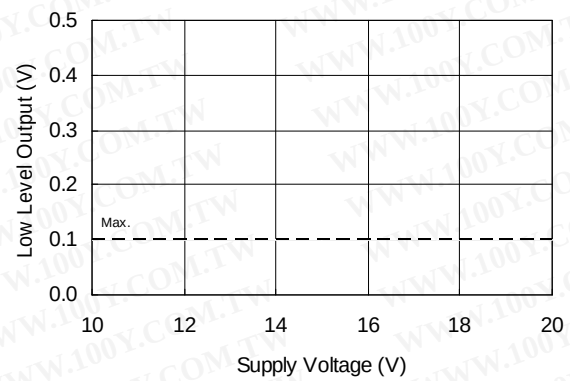


Figure 11B. Low Level Output vs. Supply Voltage

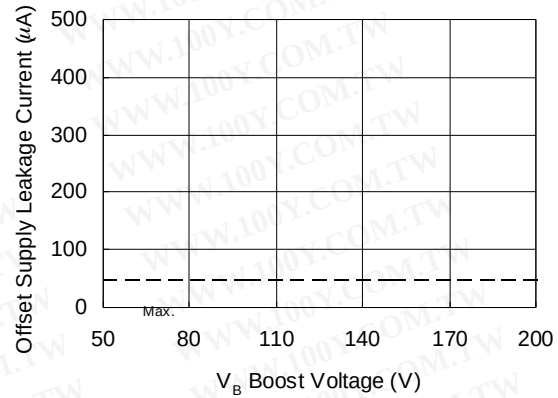
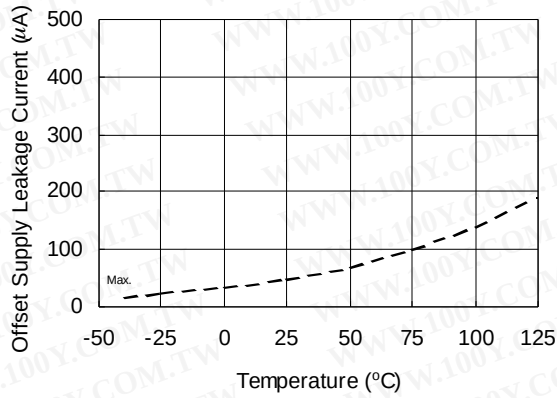
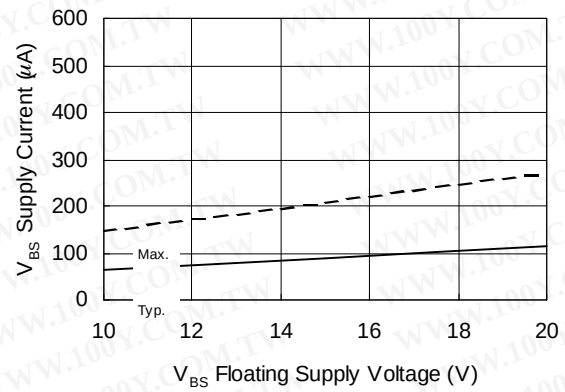
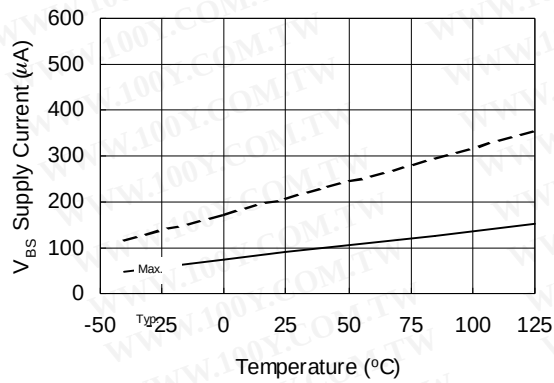


Figure 12A. Offset Supply Leakage Current vs. Temperature



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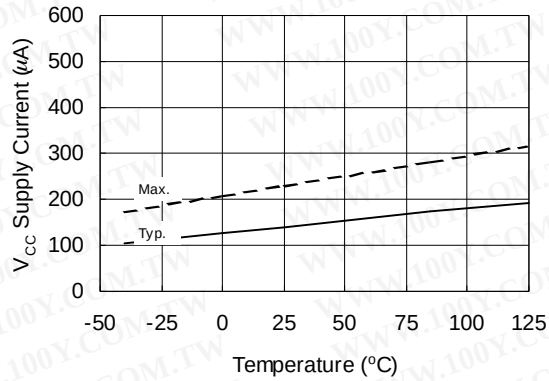


Figure 14A. V_{CC} Supply Current vs. Temperature

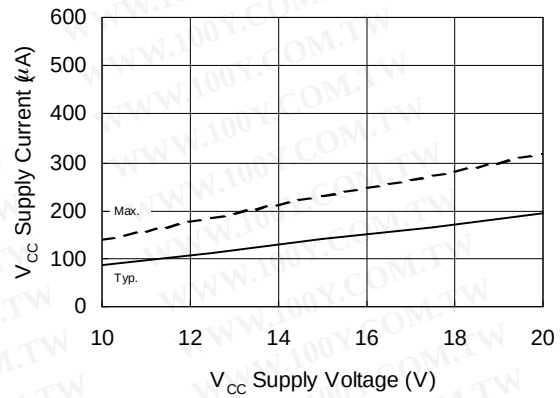


Figure 14B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

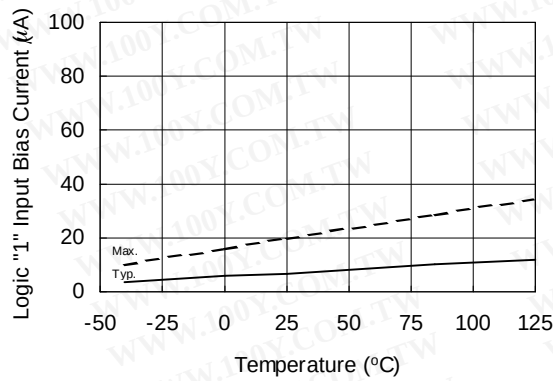
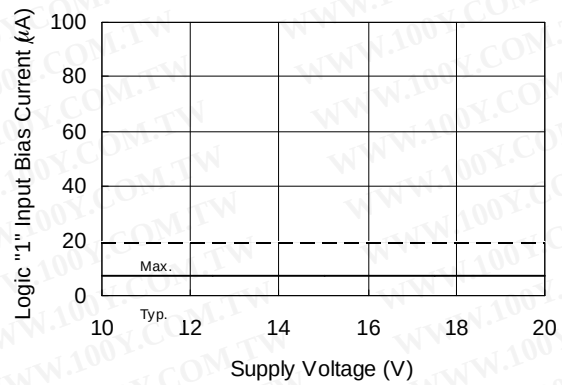


Figure 15A. Logic "1" Input Bias Current vs. Temperature



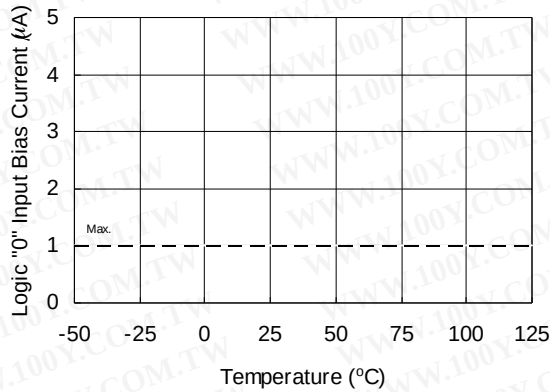


Figure 16A. Logic "0" Input Bias Current vs. Temperature

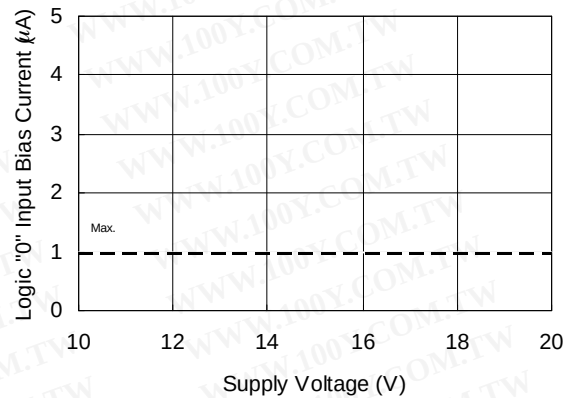


Figure 16B. Logic "0" Input Bias Current vs. Supply Voltage

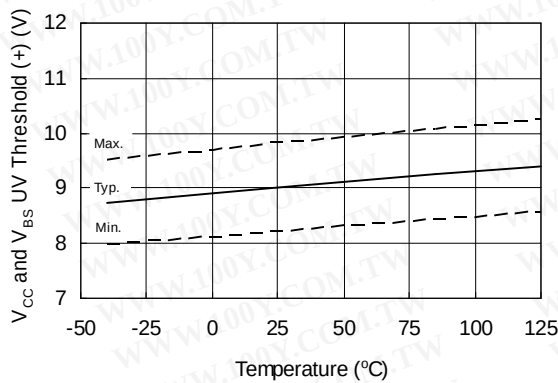


Figure 17. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

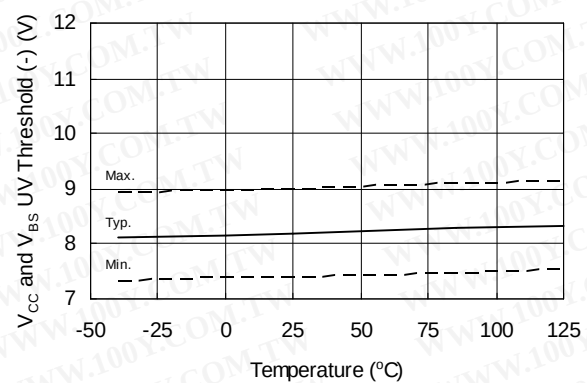


Figure 18. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

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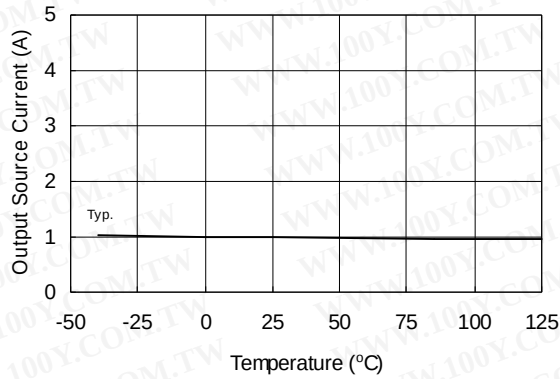


Figure 19A. Output Source Current vs. Temperature

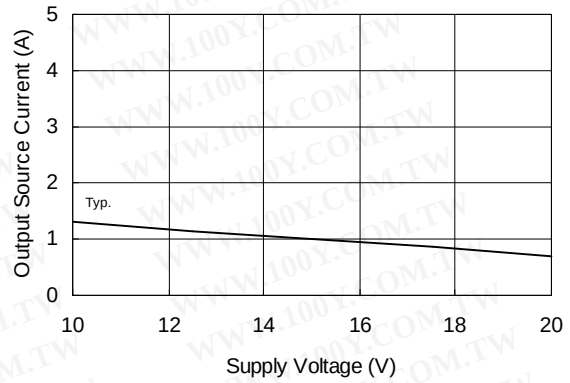


Figure 19B. Output Source Current vs. Supply Voltage

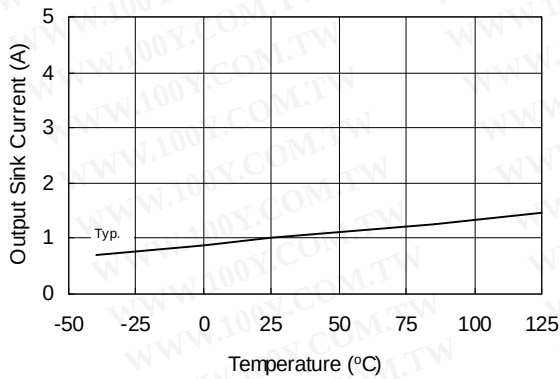


Figure 20A. Output Sink Current vs. Temperature

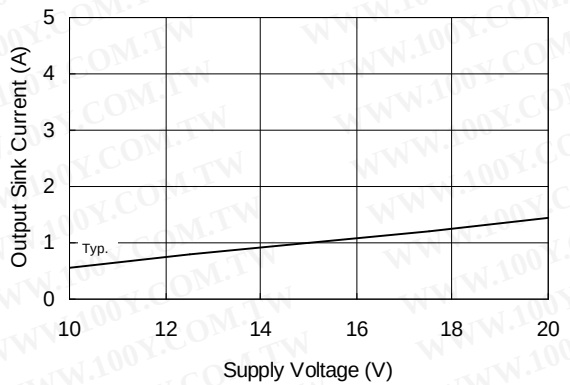
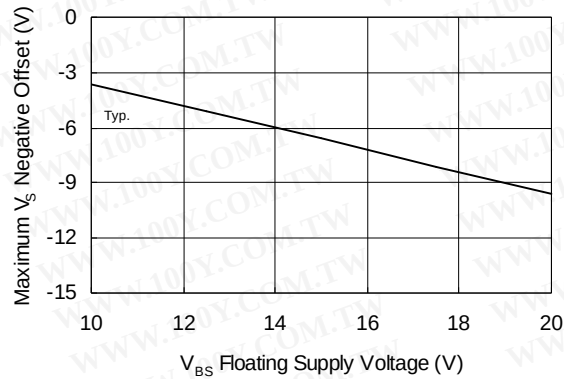


Figure 20B. Output Sink Current vs. Supply Voltage

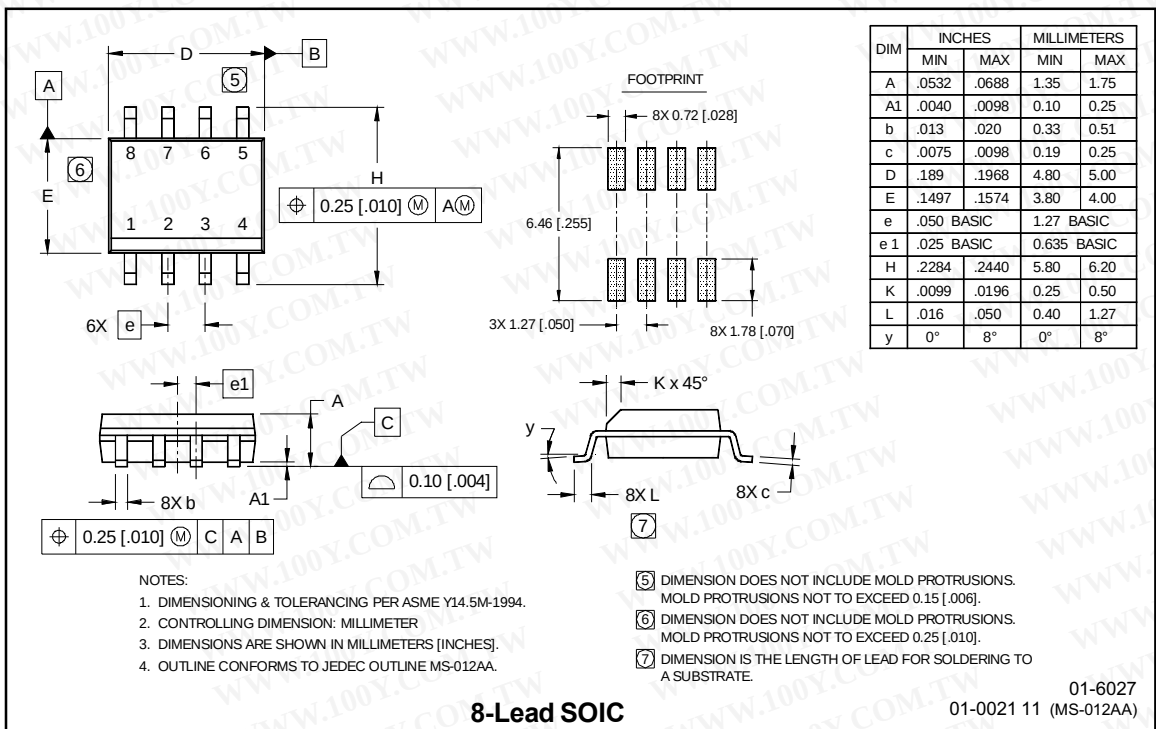
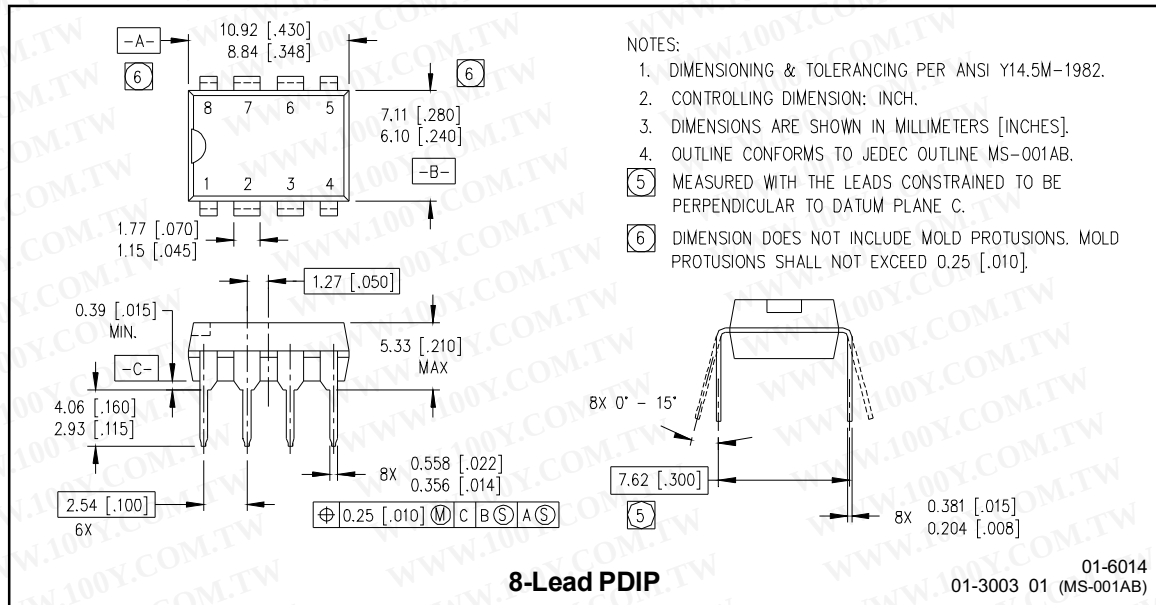


**Figure 21. Maximum V_s Negative Offset
vs. V_{BS} Floating Supply Voltage**

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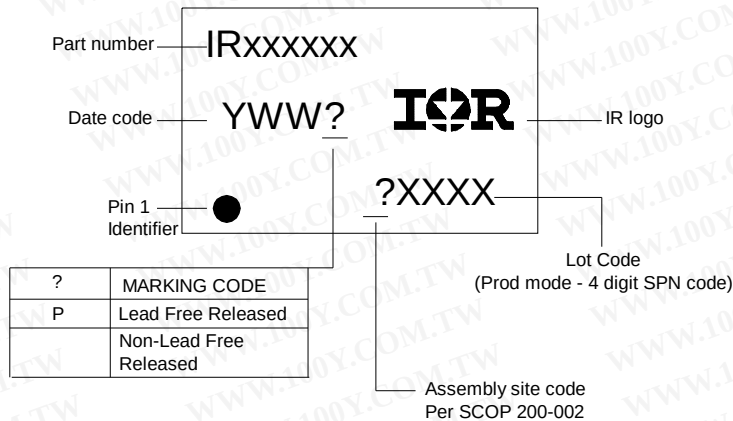
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Case outlines



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LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

8-Lead PDIP IR2011 order IR2011

8-Lead SOIC IR2011S order IR2011S

Leadfree Part

8-Lead PDIP IR2011 order IR2011PbF

8-Lead SOIC IR2011S order IR2011SPbF