

International IR Rectifier

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PD-90369

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-204AA/AE)

IRF140 100V, N-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF140	100V	0.077Ω	28A



The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 0V, TC = 25°C	Continuous Drain Current	28	A
ID @ VGS = 0V, TC = 100°C	Continuous Drain Current	20	
IDM	Pulsed Drain Current ①	112	
PD @ TC = 25°C	Max. Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	250	mJ
IAR	Avalanche Current ①	28	A
EAR	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I _D = 1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.077	Ω	V _{GS} = 10V, I _D = 20A ④
		—	—	0.089		V _{GS} = 10V, I _D = 28A ④
VGS(th)	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
gfs	Forward Transconductance	9.1	—	—	S (Ω)	V _{DS} > 15V, I _{DS} = 20A ④
IDSS	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V V _{GS} = 0V, T _J = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Qg	Total Gate Charge	30	—	59	nC	V _{GS} = 10V, I _D = 28A V _{DS} = 50V
Qgs	Gate-to-Source Charge	2.4	—	12		
Qgd	Gate-to-Drain ('Miller') Charge	12	—	30.7		
td(on)	Turn-On Delay Time	—	—	21	ns	V _{DD} = 50V, I _D = 28A, R _G = 9.1Ω
tr	Rise Time	—	—	145		
td(off)	Turn-Off Delay Time	—	—	21		
tf	Fall Time	—	—	105		
L _S + L _D	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
Ciss	Input Capacitance	—	1660	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
Coss	Output Capacitance	—	550	—		
Crss	Reverse Transfer Capacitance	—	120	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	28	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	112		
VSD	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 28A, V _{GS} = 0V ④
trr	Reverse Recovery Time	—	—	400	nS	T _J = 25°C, I _F = 28A, di/dt ≤ 100A/μs
QRR	Reverse Recovery Charge	—	—	2.9	μC	V _{DD} ≤ 50V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	1.0	°C/W	Typical socket mount
R _{thJA}	Junction to Ambient	—	—	30		

For footnotes refer to the last page

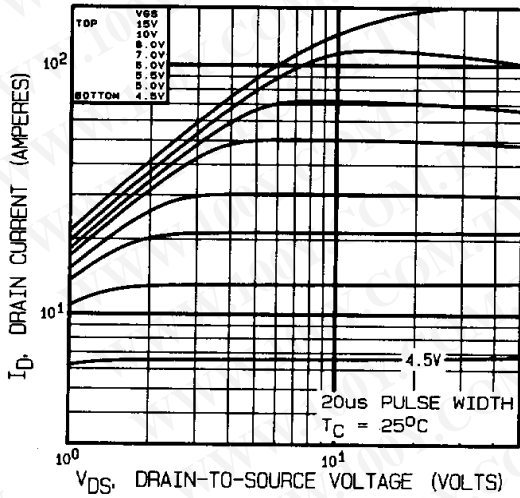


Fig 1. Typical Output Characteristics

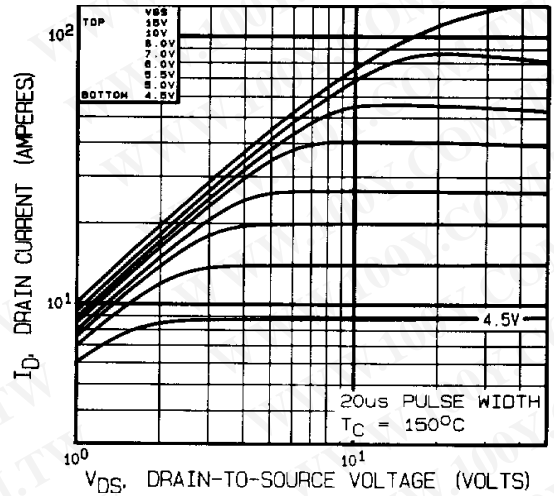


Fig 2. Typical Output Characteristics

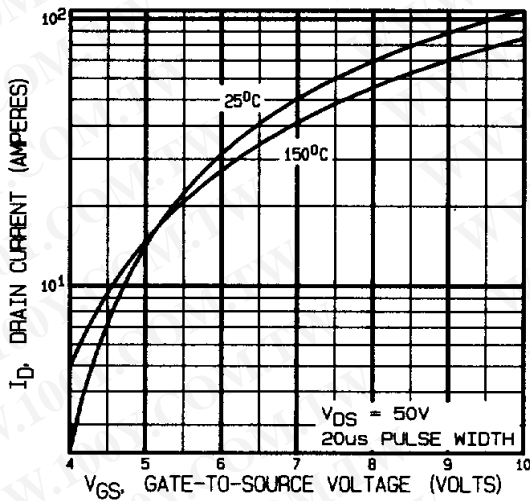


Fig 3. Typical Transfer Characteristics

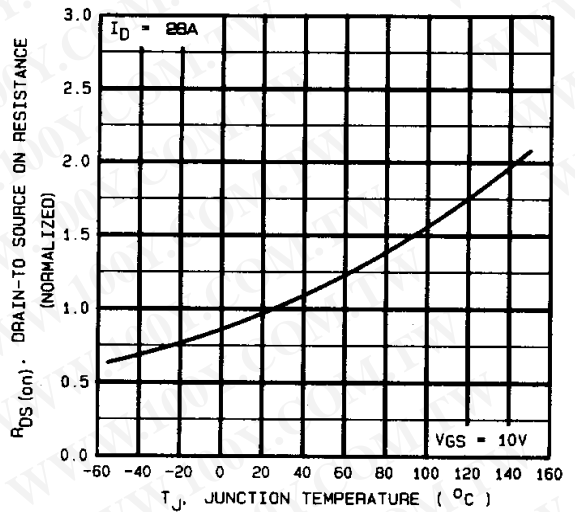


Fig 4. Normalized On-Resistance Vs. Temperature

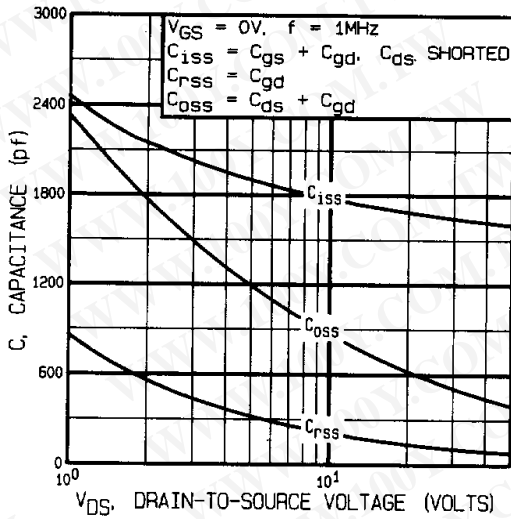


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

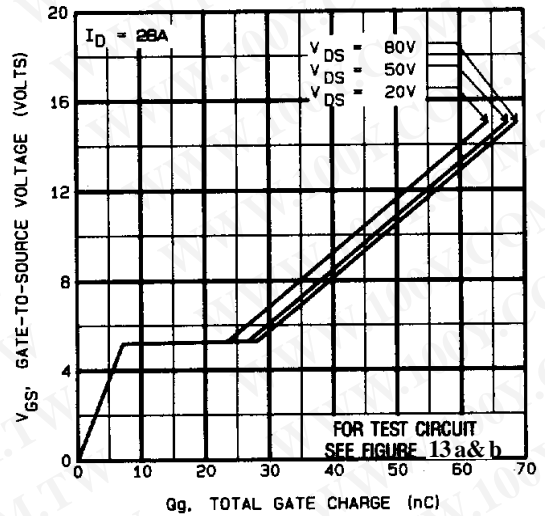


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

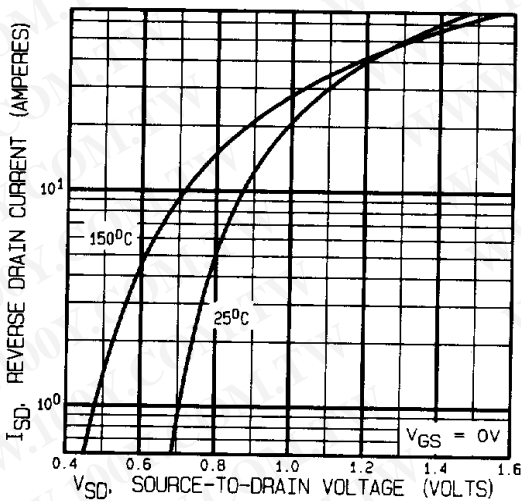


Fig 7. Typical Source-Drain Diode Forward Voltage

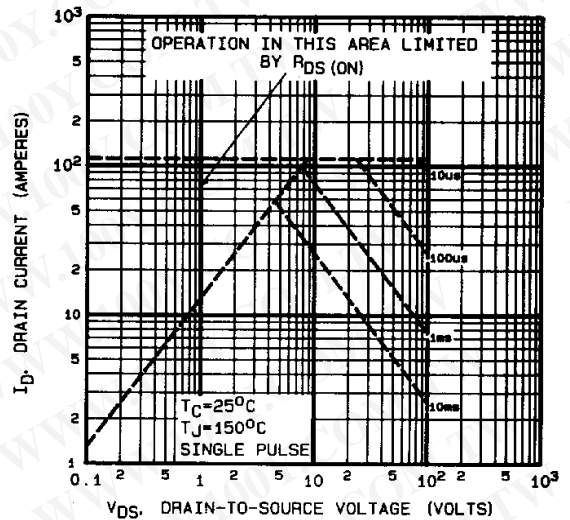


Fig 8. Maximum Safe Operating Area

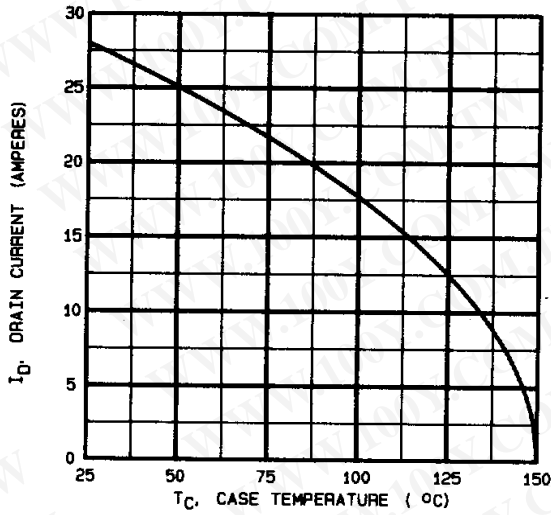


Fig9. Maximum Drain Current Vs. Case Temperature

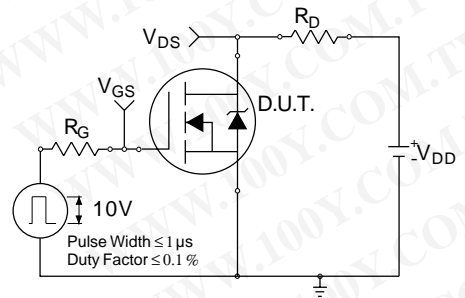


Fig 10a. Switching Time Test Circuit

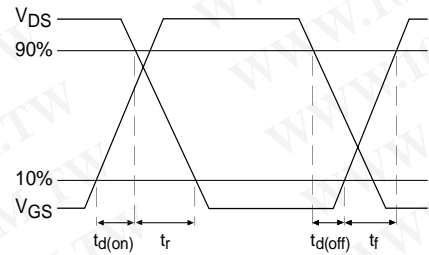


Fig 10b. Switching Time Waveforms

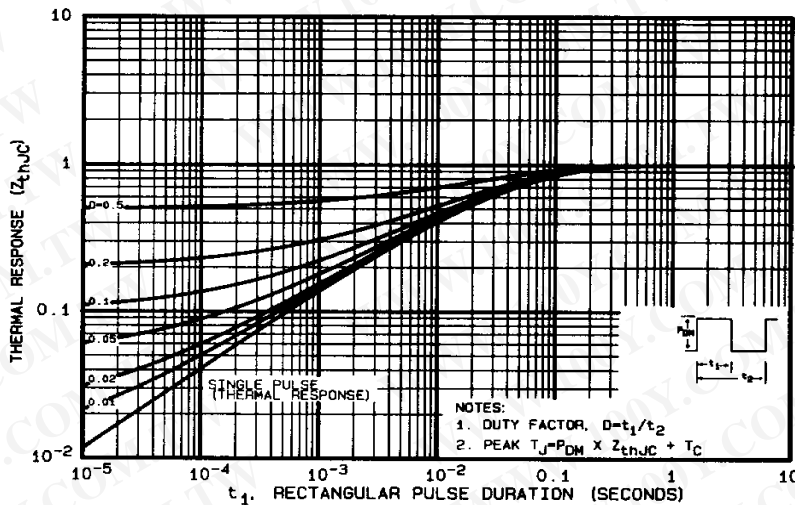


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

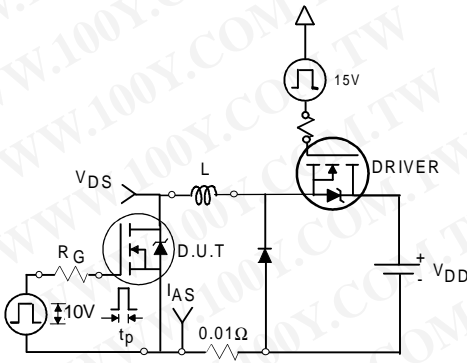


Fig 12a. Unclamped Inductive Test Circuit

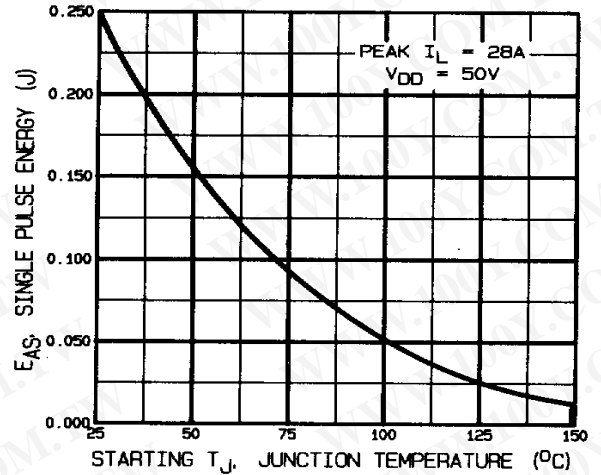


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

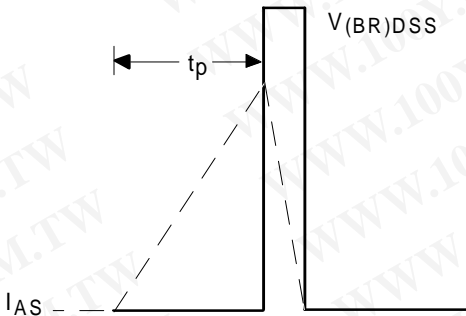


Fig 12b. Unclamped Inductive Waveforms

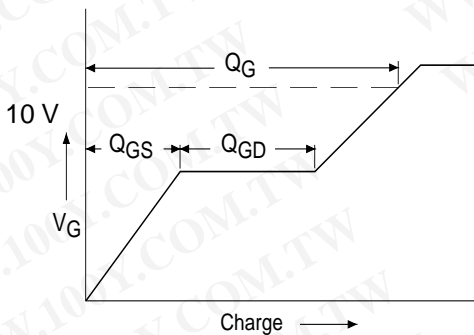


Fig 13a. Basic Gate Charge Waveform

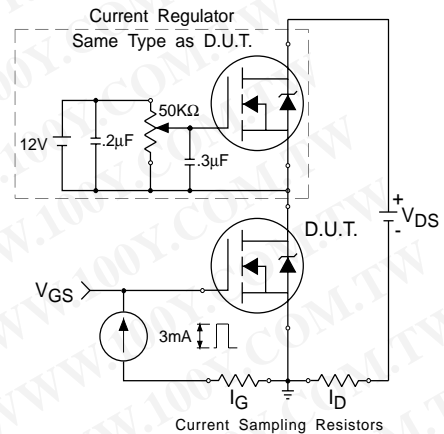
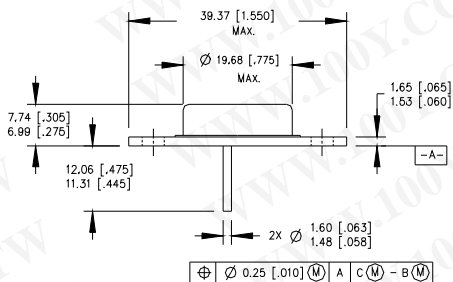


Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$, Peak $I_L = 28A$,
- ③ $I_{SD} \leq 28A$, $di/dt \leq 170A/\mu s$, $V_{DD} \leq 100V$, $T_J \leq 150^{\circ}C$
Suggested $R_G = 9.1 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-204AE (Modified TO-3)



PIN ASSIGNMENTS

- 1 - SOURCE
- 2 - GATE
- 3 - DRAIN (CASE)

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204AE.

