

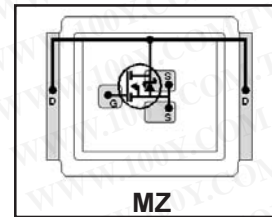
IRF6674TRPbF

DirectFET™ Power MOSFET ②

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	R_{DS(on)}
60V max	±20V max	9.0mΩ @ 10V
Q_{g tot}	Q_{gd}	V_{gs(th)}
24nC	8.3nC	4.0V

- RoHS Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SH	SJ	SP	MZ	MN					
----	----	----	-----------	----	--	--	--	--	--

Description

The IRF6674PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of an Micro8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6674PbF is optimized for primary side sockets in forward and push-pull isolated DC-DC topologies, for 48V and 36V-60V input voltage range systems. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	60	V
V _{GS}	Gate-to-Source Voltage	±20	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V ③	13.4	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V ③	10.7	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ④	67	
I _{DM}	Pulsed Drain Current ⑤	134	
E _{AS}	Single Pulse Avalanche Energy ⑥	98	mJ
I _{AS}	Avalanche Current ⑥	13.4	A

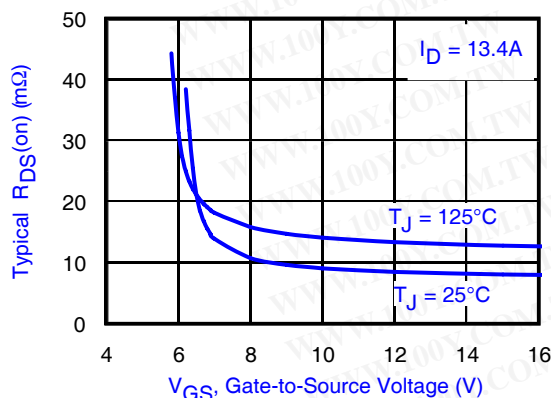


Fig 1. Typical On-Resistance vs. Gate Voltage

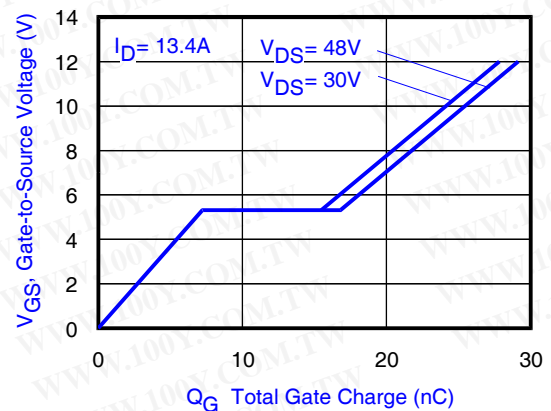


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

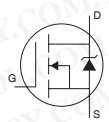
- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting T_J = 25°C, L = 0.272mH, R_G = 25Ω, I_{AS} = 13.4A.

Electrical Characteristic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$B_{V_{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta B_{V_{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	9.0	11	m Ω	$V_{GS} = 10V, I_D = 13.4A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	3.0	4.0	4.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
gfs	Forward Transconductance	16	—	—	S	$V_{DS} = 25V, I_D = 13.4A$
Q_g	Total Gate Charge	—	24	36	nC	$V_{DS} = 30V$ $V_{GS} = 10V$ $I_D = 13.4A$ See Fig. 15
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	5.4	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.9	—		
Q_{gd}	Gate-to-Drain Charge	—	8.3	12		
Q_{godr}	Gate Charge Overdrive	—	8.4	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	10.2	—		
Q_{oss}	Output Charge	—	14	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.0	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD} = 30V, V_{GS} = 10V$ ② $I_D = 13.4A$ $R_G = 6.2\ \Omega$
t_r	Rise Time	—	12	—		
$t_{d(off)}$	Turn-Off Delay Time	—	12	—		
t_f	Fall Time	—	8.7	—		
C_{iss}	Input Capacitance	—	1350	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	390	—		
C_{riss}	Reverse Transfer Capacitance	—	105	—		
C_{oss}	Output Capacitance	—	1580	—		$V_{GS} = 0V, V_{DS} = 1.0V, f=1.0\text{MHz}$
C_{oss}	Output Capacitance	—	290	—		$V_{GS} = 0V, V_{DS} = 48V, f=1.0\text{MHz}$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) $T_J = 25^\circ\text{C}$	—	—	67	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	134		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 13.4A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	32	48	ns	$T_J = 25^\circ\text{C}, I_F = 13.4A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	36	54	nC	$di/dt = 100A/\mu s$ ①



Notes:

- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	3.6	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	2.3	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
T_P	Peak Soldering Temperature	270	$^\circ\text{C}$
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	35	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑩	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	

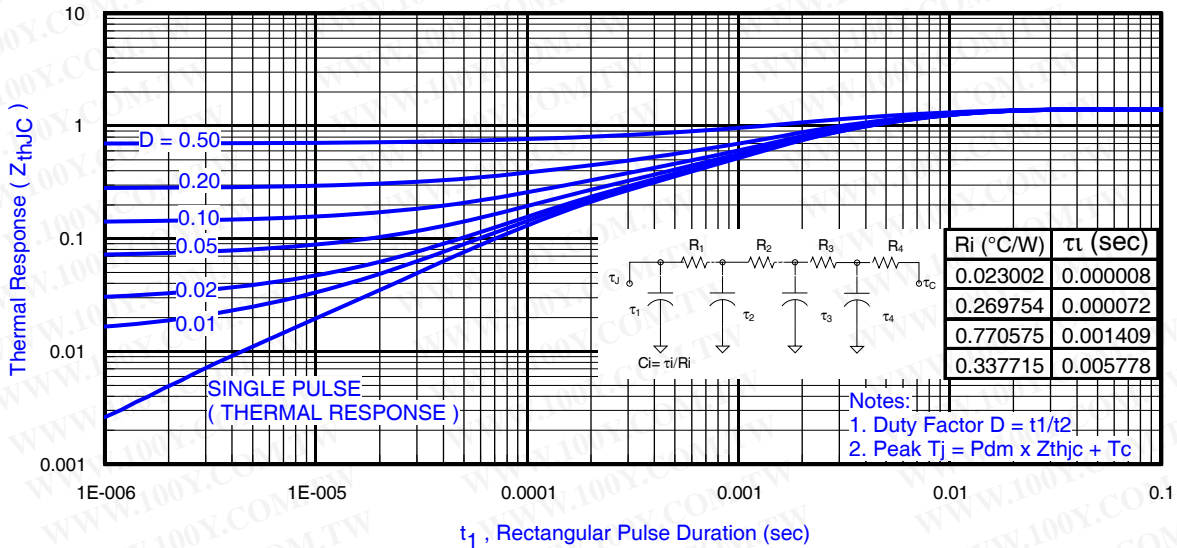


Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case ①

Notes:

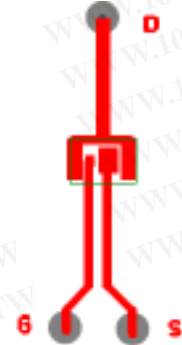
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④ T_C measured with thermocouple incontact with top (Drain) of part.
- ⑧ Used double sided cooling, mounting pad with large heatsink.
- ⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑩ R_{θ} is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu board (still air).



⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink. (still air)



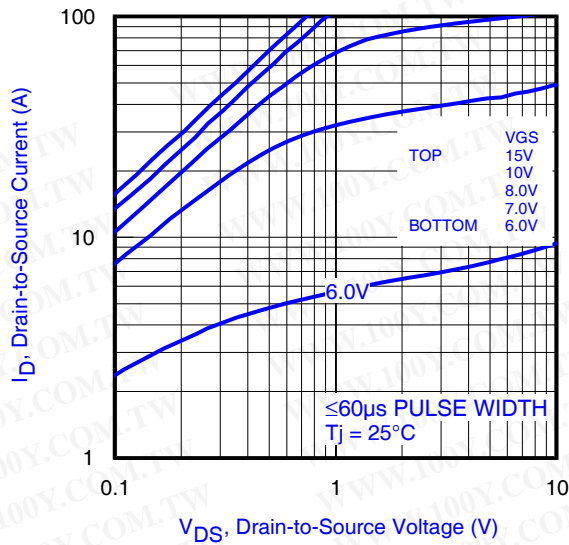


Fig 4. Typical Output Characteristics

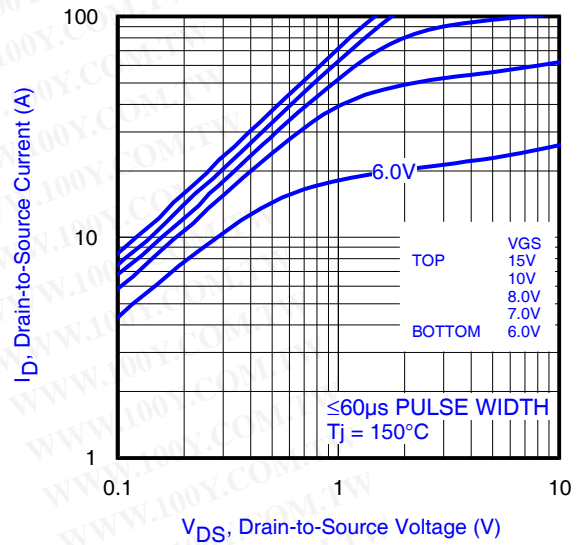


Fig 5. Typical Output Characteristics

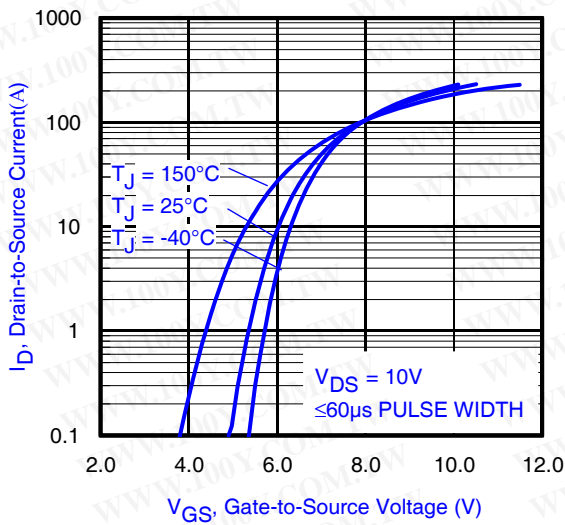


Fig 6. Typical Transfer Characteristics

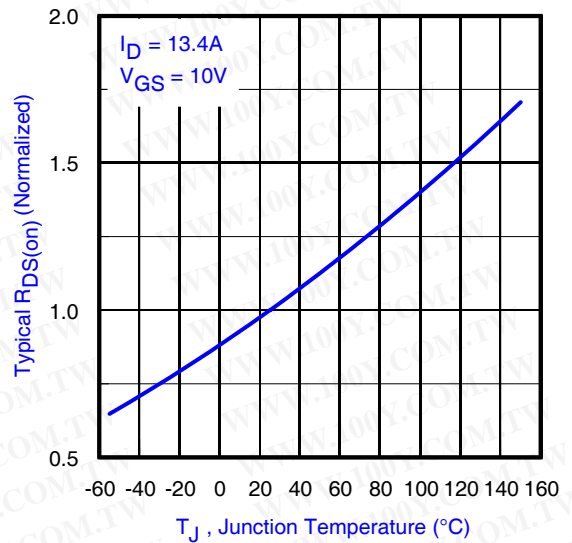


Fig 7. Normalized On-Resistance vs. Temperature

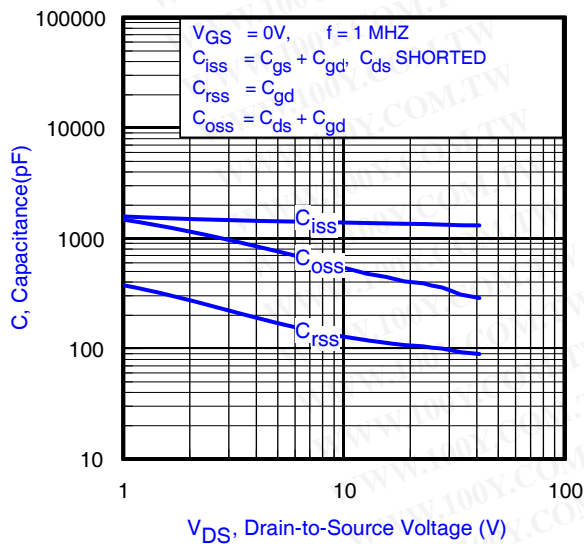


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

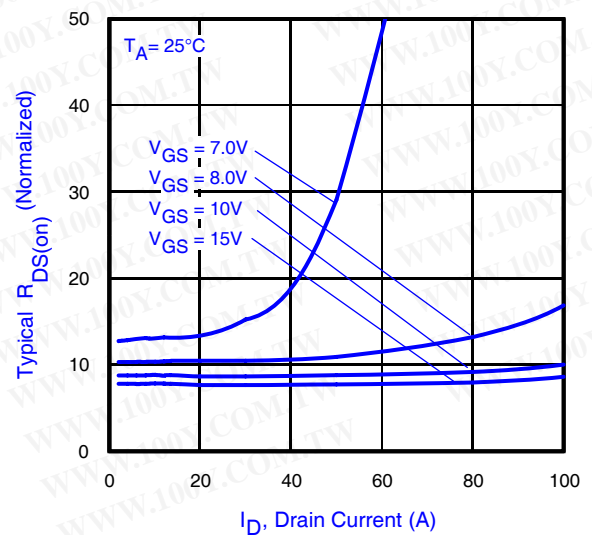


Fig 9. Typical On-Resistance vs. Drain Current

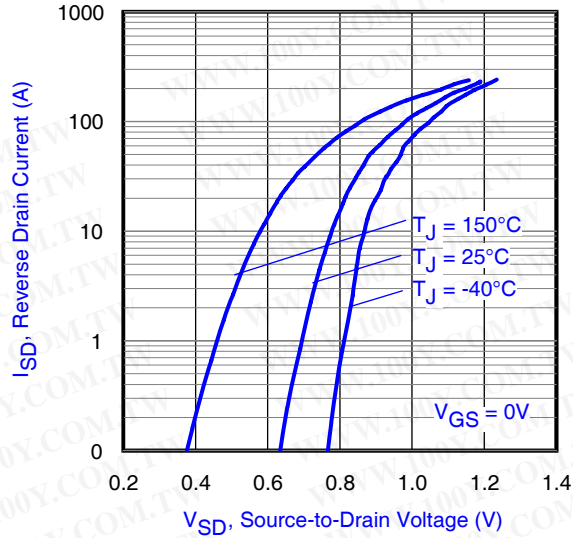


Fig 10. Typical Source-Drain Diode Forward Voltage

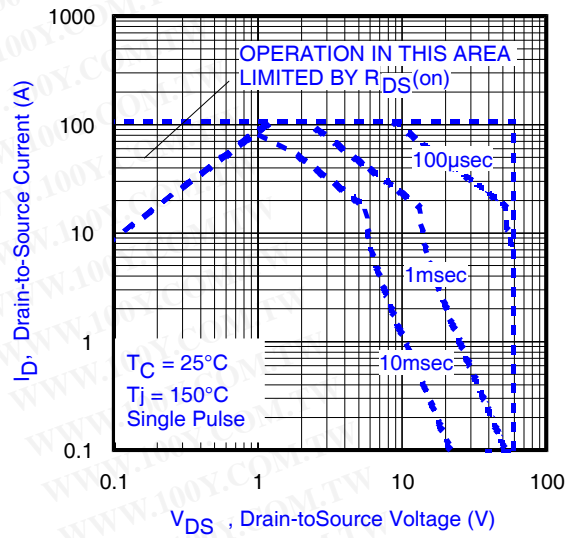


Fig 11. Maximum Safe Operating Area

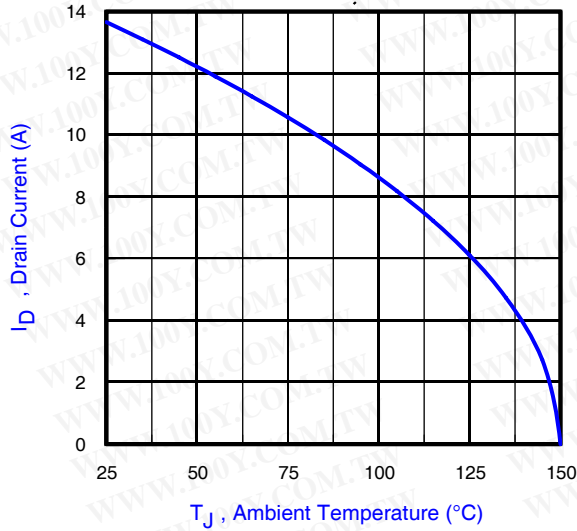


Fig 12. Maximum Drain Current vs. Ambient Temperature

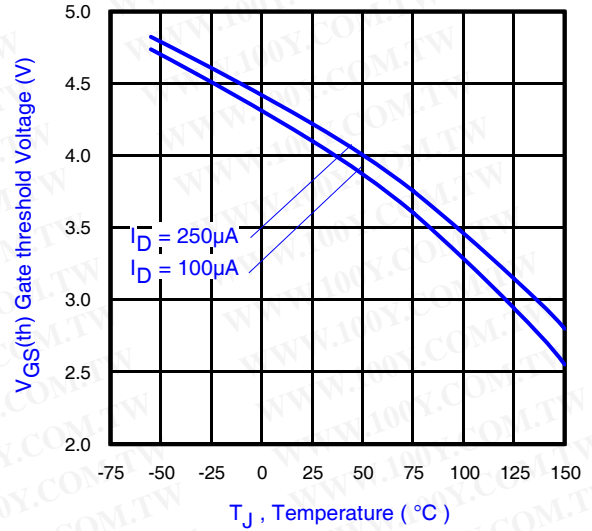


Fig 13. Typical Threshold Voltage vs. Junction Temperature

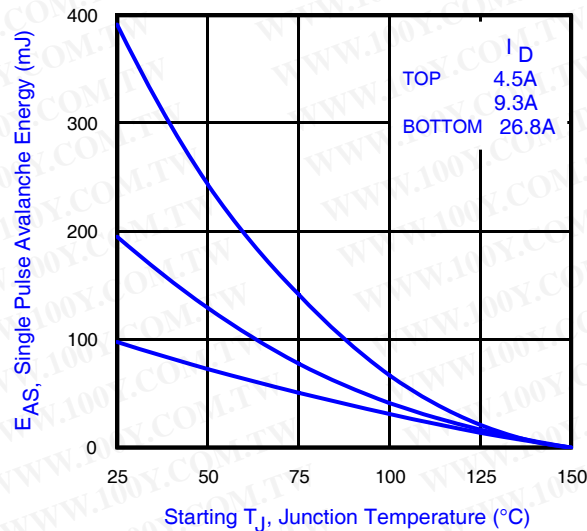


Fig 14. Maximum Avalanche Energy vs. Drain Current

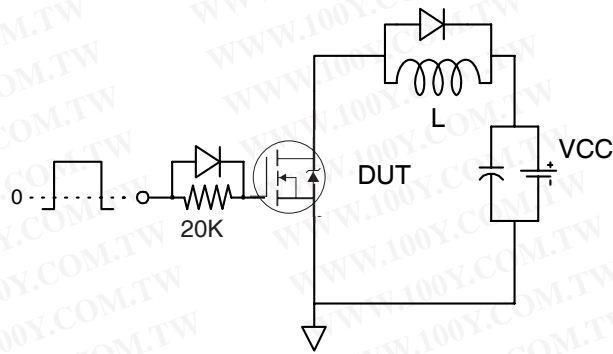


Fig 15a. Gate Charge Test Circuit

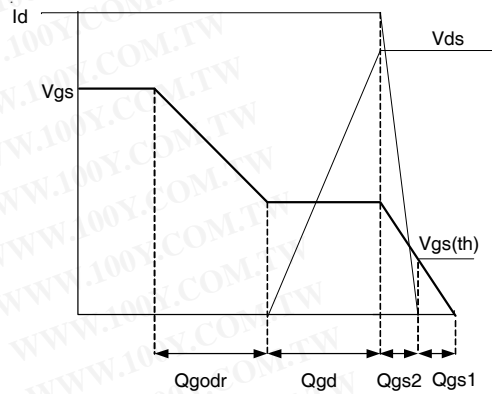


Fig 15b. Gate Charge Waveform

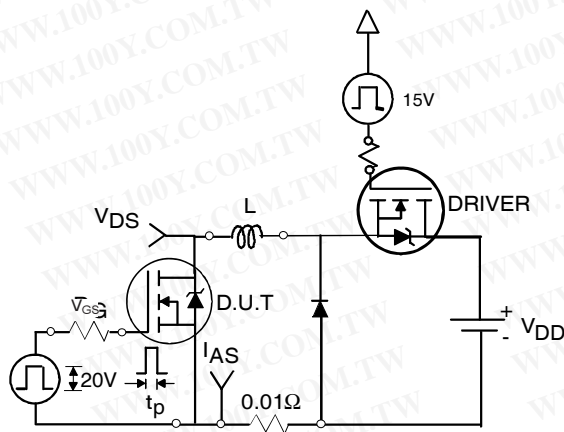


Fig 16a. Unclamped Inductive Test Circuit

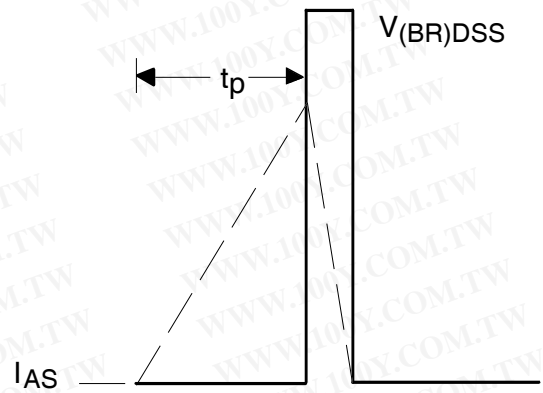


Fig 16b. Unclamped Inductive Waveforms

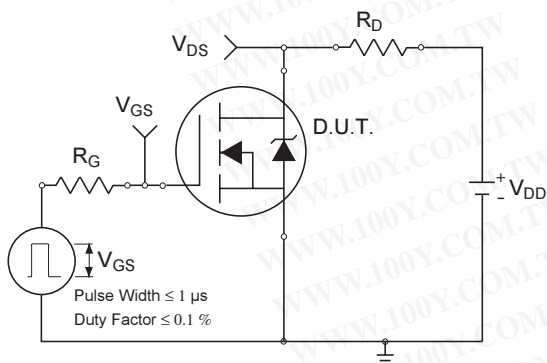


Fig 17a. Switching Time Test Circuit

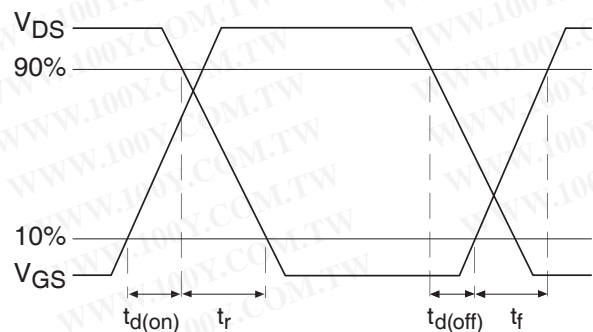


Fig 17b. Switching Time Waveforms

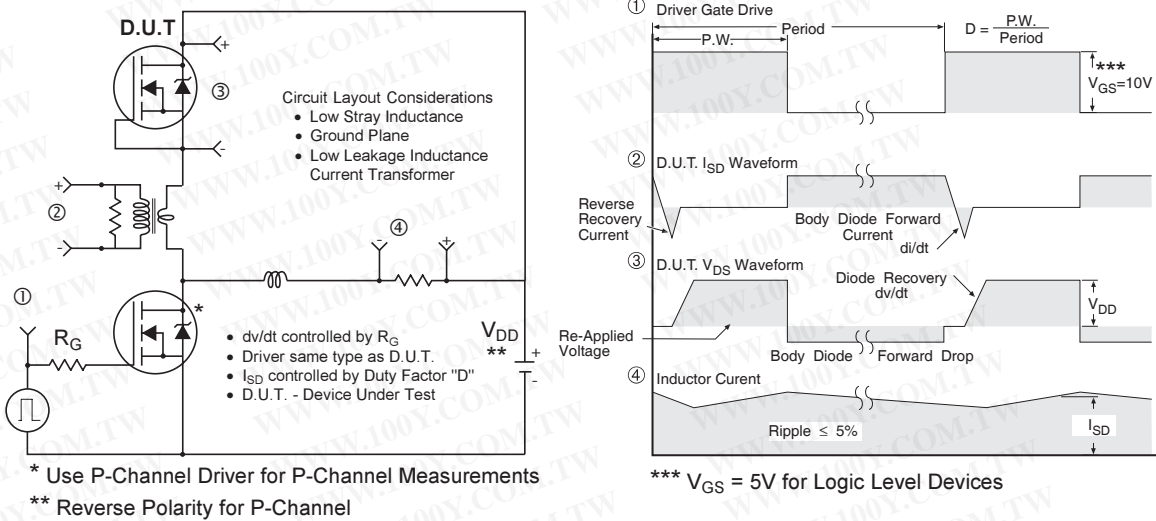
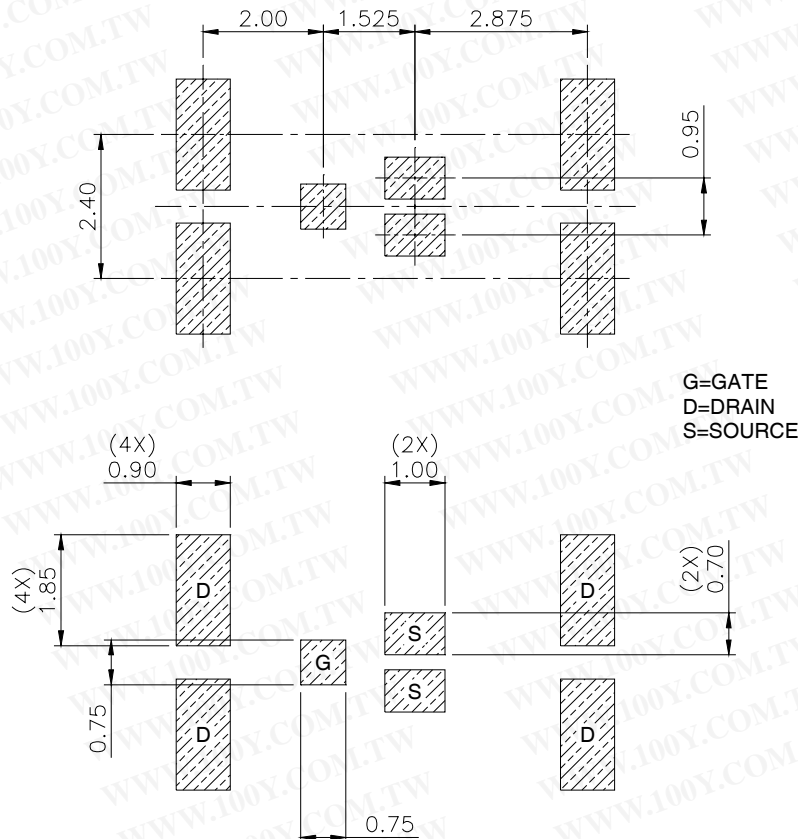


Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

DirectFET™ Substrate and PCB Layout, MZ Outline (Medium Size Can, Z-Designation).

Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations

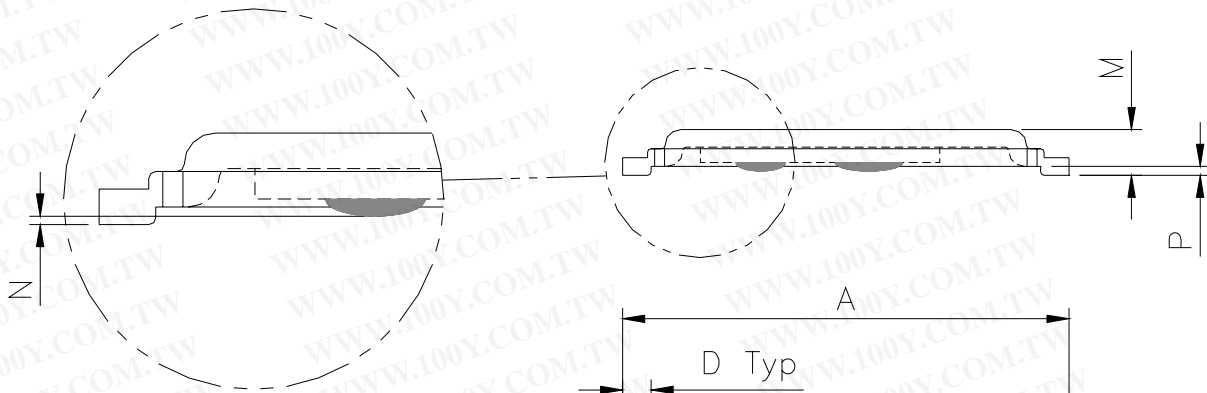


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>
www.irf.com

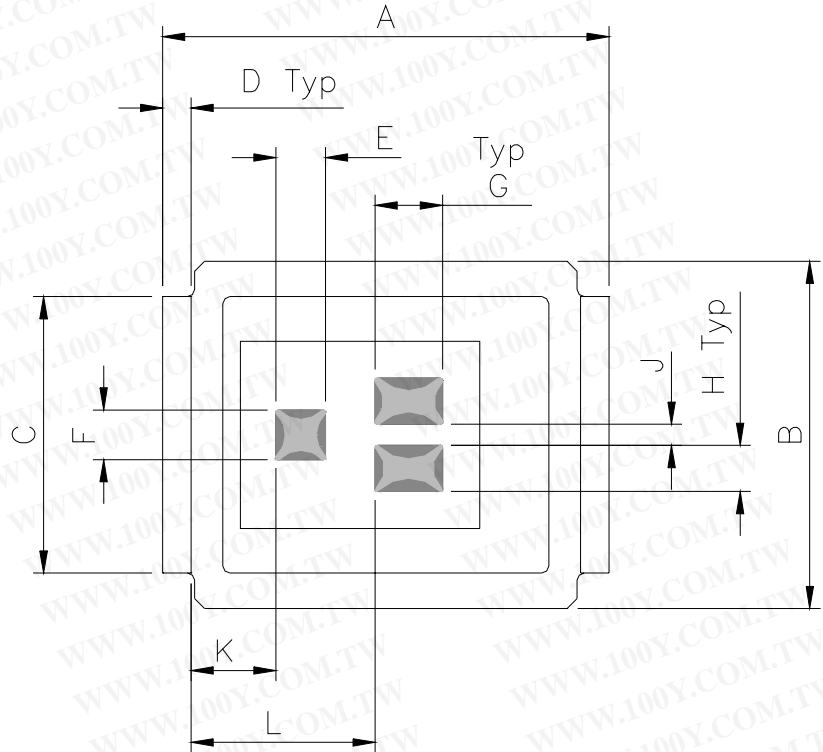
IRF6674TRPbF

DirectFET™ Outline Dimension, MZ Outline (Medium Size Can, Z-Designation).

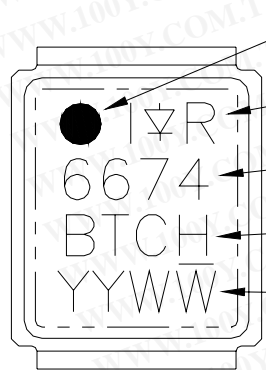
Please see AN-1035 for DirectFET assembly details and stencil and substrate design recommendations



DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	0.93	0.97	0.037	0.038
H	0.63	0.67	0.025	0.026
J	0.28	0.32	0.011	0.013
K	1.13	1.26	0.044	0.050
L	2.53	2.66	0.100	0.105
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007



DirectFET™ Part Marking



GATE MARKING

LOGO

PART NUMBER

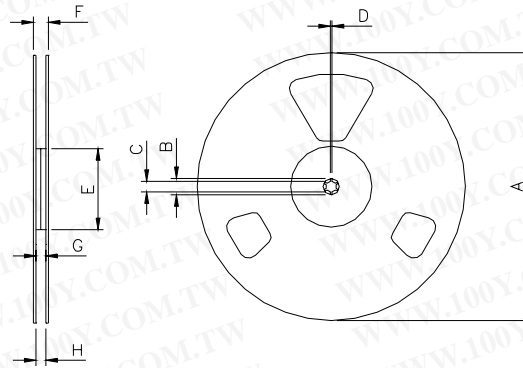
BATCH NUMBER

DATE CODE

Line above the last character of the date code indicates "Lead-Free"

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

DirectFET™ Tape & Reel Dimension (Showing component orientation).

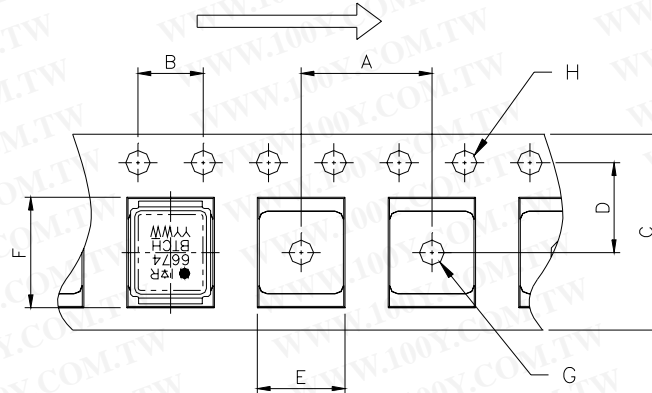


勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

NOTE: Controlling dimensions in mm
 Std reel quantity is 4800 parts. (ordered as IRF6674MTRPbF). For 1000 parts on 7" reel, order IRF6674MTR1PbF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.