International
IOR Rectifier

PD - 95728A

IRF9910PbF

HEXFET® Power MOSFET

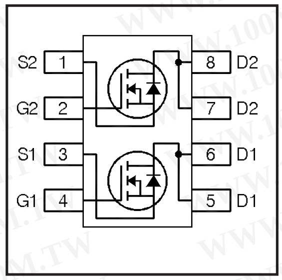
Applications

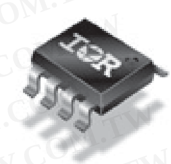
- Dual SO-8 MOSFET for POL converters in desktop, servers, graphics cards, game consoles and set-top box
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max		I_D
20V	Q1	13.4mΩ@V_{GS} = 10V	10A
	Q2	9.3mΩ@V_{GS} = 10V	12A

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating





SO-8

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	20		V
V_{GS}	Gate-to-Source Voltage	± 20		
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	10	12	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	8.3	9.9	
I_{DM}	Pulsed Drain Current ①	83	98	
P_D @T_A = 25°C	Power Dissipation	2.0		W
P_D @T_A = 70°C	Power Dissipation	1.3		
	Linear Derating Factor	0.016		W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	—	62.5	

Notes ① through ⑤ are on page 10

07/23/08

Static @ T_J = 25°C (unless otherwise specified)

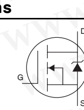
	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	20	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	—	0.0061	—	V/°C	Reference to 25°C, I_D = 1mA
		Q2	—	0.014	—		
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	—	10.7	13.4	mΩ	V_{GS} = 10V, I_D = 10A ③
			—	14.6	18.3		V_{GS} = 4.5V, I_D = 8.3A ③
		Q2	—	7.4	9.3		V_{GS} = 10V, I_D = 12A ③
			—	9.1	11.3		V_{GS} = 4.5V, I_D = 9.8A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1&Q2	1.65	—	2.55	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	—	-4.9	—	mV/°C	
		Q2	—	-5.0	—		
I_{DSS}	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V_{DS} = 16V, V_{GS} = 0V
		Q1&Q2	—	—	100		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	Q1	19	—	—	S	V_{DS} = 10V, I_D = 8.3A
		Q2	27	—	—		V_{DS} = 10V, I_D = 9.8A
Q_g	Total Gate Charge	Q1	—	7.4	11	nC	Q1 V_{DS} = 10V V_{GS} = 4.5V, I_D = 8.3A Q2 V_{DS} = 10V V_{GS} = 4.5V, I_D = 9.8A
		Q2	—	15	23		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	—	2.6	—		
		Q2	—	4.3	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	—	0.85	—		
		Q2	—	1.4	—		
Q_{gd}	Gate-to-Drain Charge	Q1	—	2.5	—		
		Q2	—	5.4	—		
Q_{godr}	Gate Charge Overdrive	Q1	—	1.5	—		
		Q2	—	3.9	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	—	3.4	—		
		Q2	—	6.8	—		
Q_{oss}	Output Charge	Q1	—	4.0	—	nC	V_{DS} = 10V, V_{GS} = 0V
		Q2	—	8.7	—		
$t_{d(on)}$	Turn-On Delay Time	Q1	—	6.3	—	ns	Q1 V_{DD} = 16V, V_{GS} = 4.5V I_D = 8.3A Q2 V_{DD} = 16V, V_{GS} = 4.5V I_D = 9.8A Clamped Inductive Load
		Q2	—	8.3	—		
t_r	Rise Time	Q1	—	10	—		
		Q2	—	14	—		
$t_{d(off)}$	Turn-Off Delay Time	Q1	—	9.2	—		
		Q2	—	15	—		
t_f	Fall Time	Q1	—	4.5	—		
		Q2	—	7.5	—		
C_{iss}	Input Capacitance	Q1	—	900	—	pF	V_{GS} = 0V V_{DS} = 10V f = 1.0MHz
		Q2	—	1860	—		
C_{oss}	Output Capacitance	Q1	—	290	—		
		Q2	—	600	—		
C_{rss}	Reverse Transfer Capacitance	Q1	—	140	—		
		Q2	—	310	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	33	26	mJ
I_{AR}	Avalanche Current ①	—	8.3	9.8	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	Q1&Q2	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	Q1	—	—	83	A	
		Q2	—	—	98		
V_{SD}	Diode Forward Voltage	Q1	—	—	1.0	V	T_J = 25°C, I_S = 8.3A, V_{GS} = 0V ③
		Q2	—	—	1.0		T_J = 25°C, I_S = 9.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	Q1	—	11	17	ns	Q1 T_J = 25°C, I_F = 8.3A, V_{DD} = 10V, di/dt = 100A/μs ③
		Q2	—	16	24		
Q_{rr}	Reverse Recovery Charge	Q1	—	3.1	4.7	nC	Q2 T_J = 25°C, I_F = 9.8A, V_{DD} = 10V, di/dt = 100A/μs ③
		Q2	—	4.9	7.3		



Q1 - Control FET **Q2 - Synchronous FET**

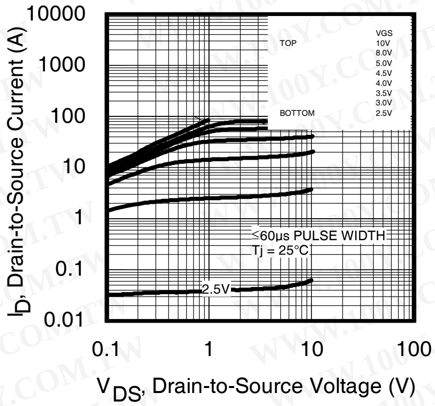


Fig 1. Typical Output Characteristics

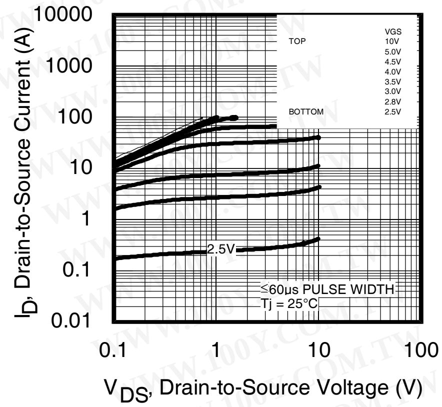


Fig 2. Typical Output Characteristics

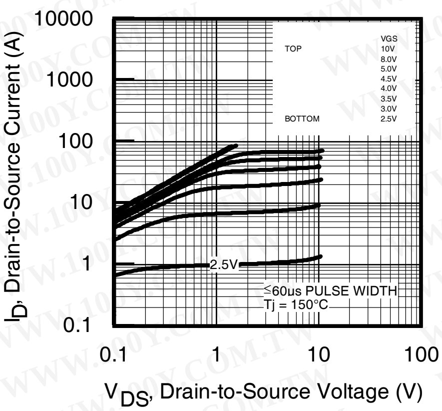


Fig 3. Typical Output Characteristics

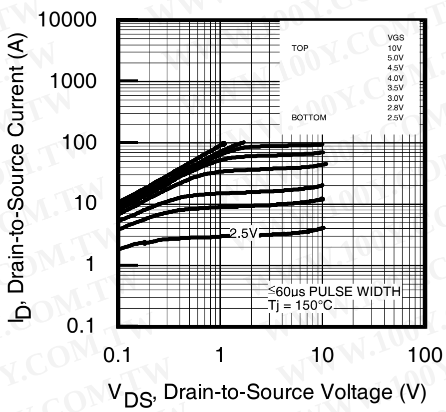


Fig 4. Typical Output Characteristics

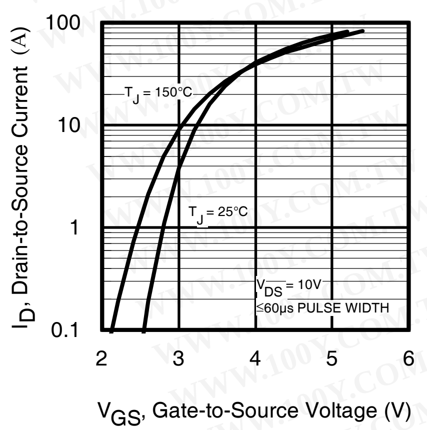


Fig 5. Typical Transfer Characteristics

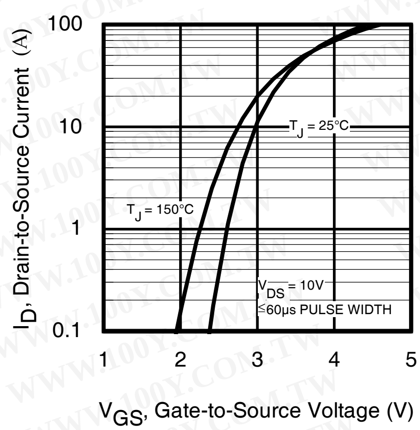


Fig 6. Typical Transfer Characteristics

Q1 - Control FET | **Q2 - Synchronous FET**

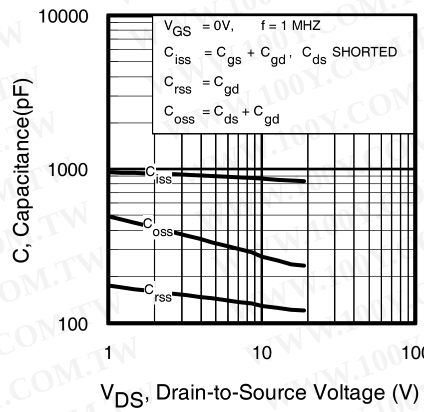


Fig 7. Typical Capacitance Vs.Drain-to-Source Voltage

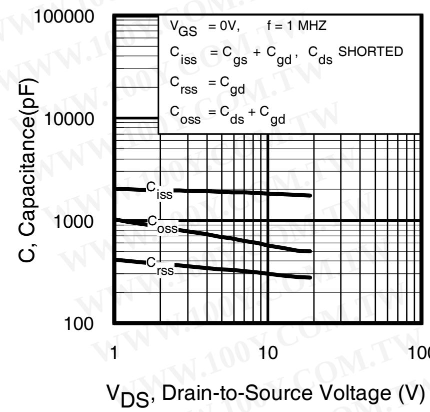


Fig 8. Typical Capacitance Vs.Drain-to-Source Voltage

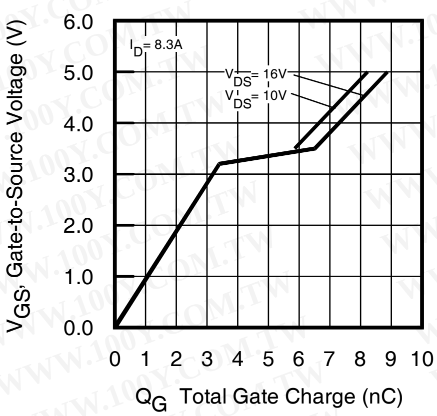


Fig. 9. Gate-to-Source Voltage vs Typical Gate Charge

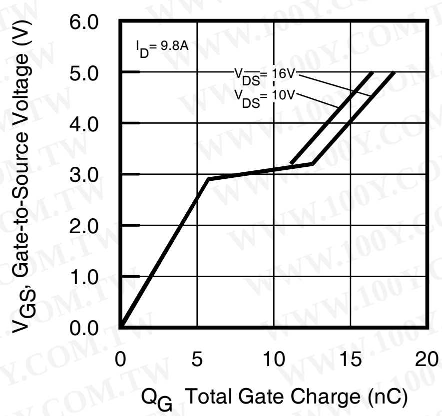


Fig. 10. Gate-to-Source Voltage vs Typical Gate Charge

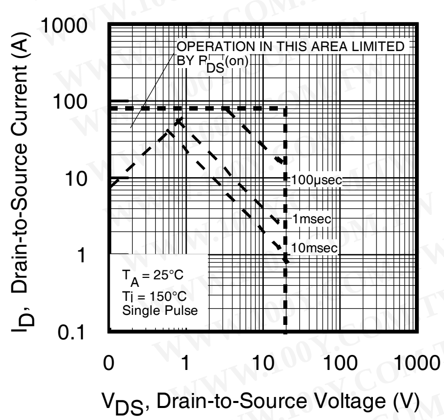


Fig 11. Maximum Safe Operating Area

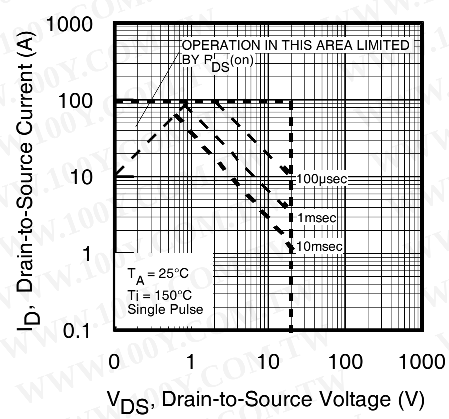


Fig 12. Maximum Safe Operating Area

Q1 - Control FET

Q2 - Synchronous FET

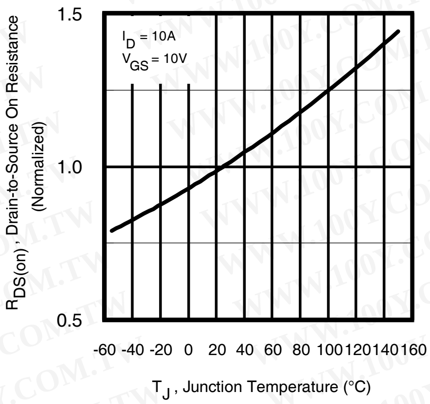


Fig 13. Normalized On-Resistance vs. Temperature

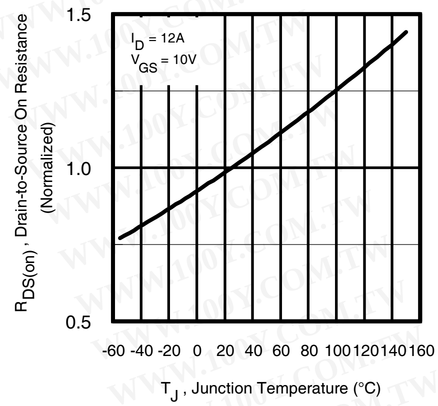


Fig 14. Normalized On-Resistance vs. Temperature

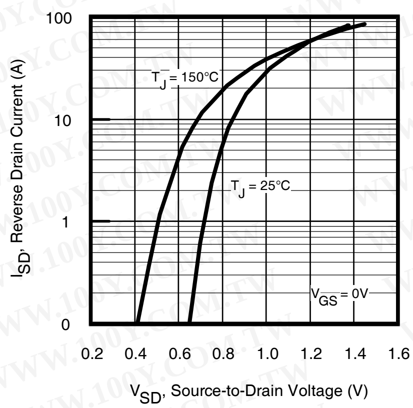


Fig 15. Typical Source-Drain Diode Forward Voltage

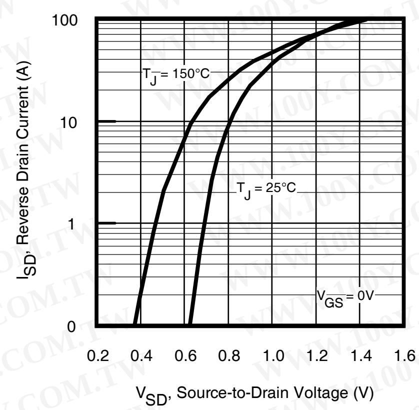


Fig 16. Typical Source-Drain Diode Forward Voltage

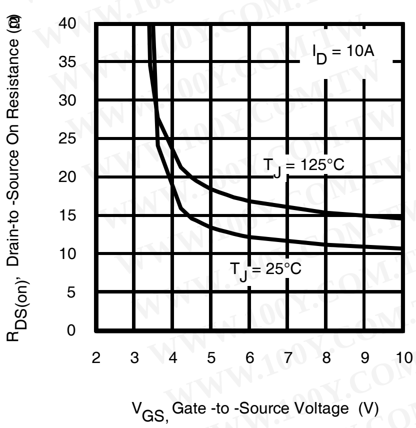


Fig 17. Typical On-Resistance vs. Gate Voltage

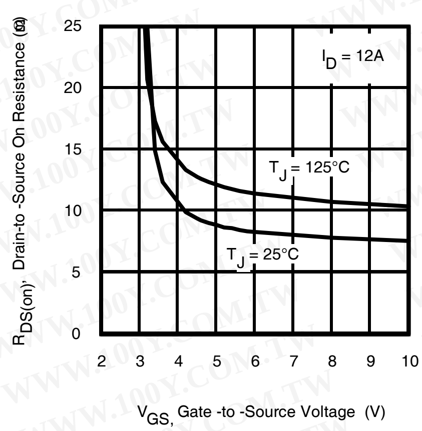


Fig 18. Typical On-Resistance vs. Gate Voltage

Q1 - Control FET

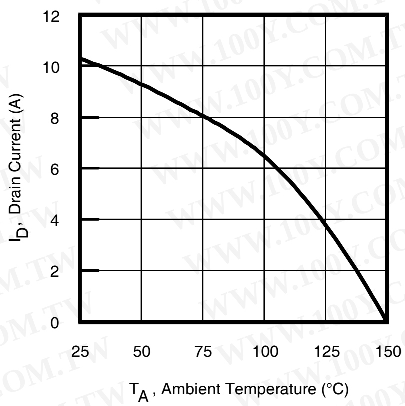


Fig 19. Maximum Drain Current vs. Ambient Temperature

Q2 - Synchronous FET

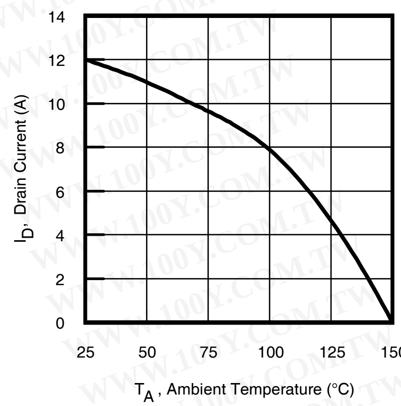


Fig 20. Maximum Drain Current vs. Ambient Temperature

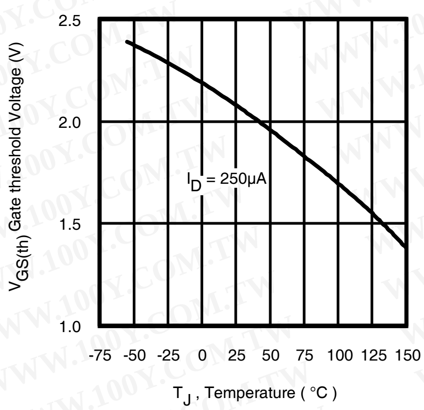


Fig 21. Threshold Voltage vs. Temperature

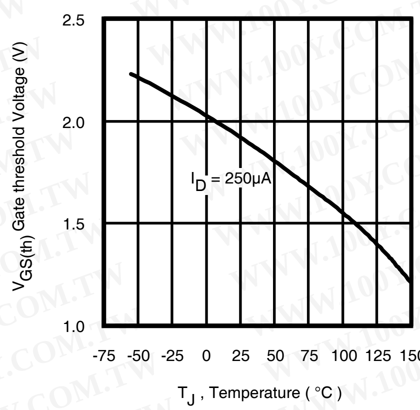


Fig 22. Threshold Voltage vs. Temperature

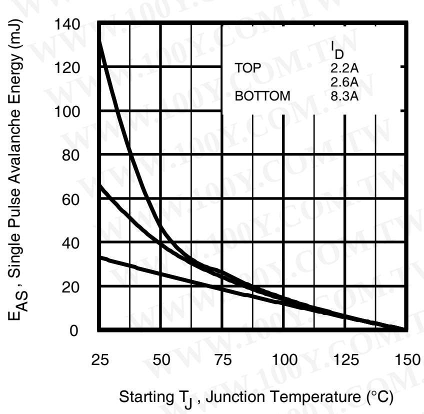


Fig 23. Maximum Avalanche Energy vs. Drain Current

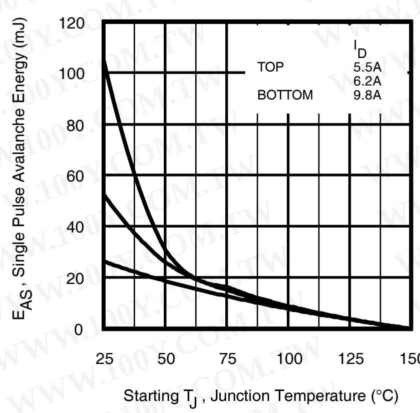
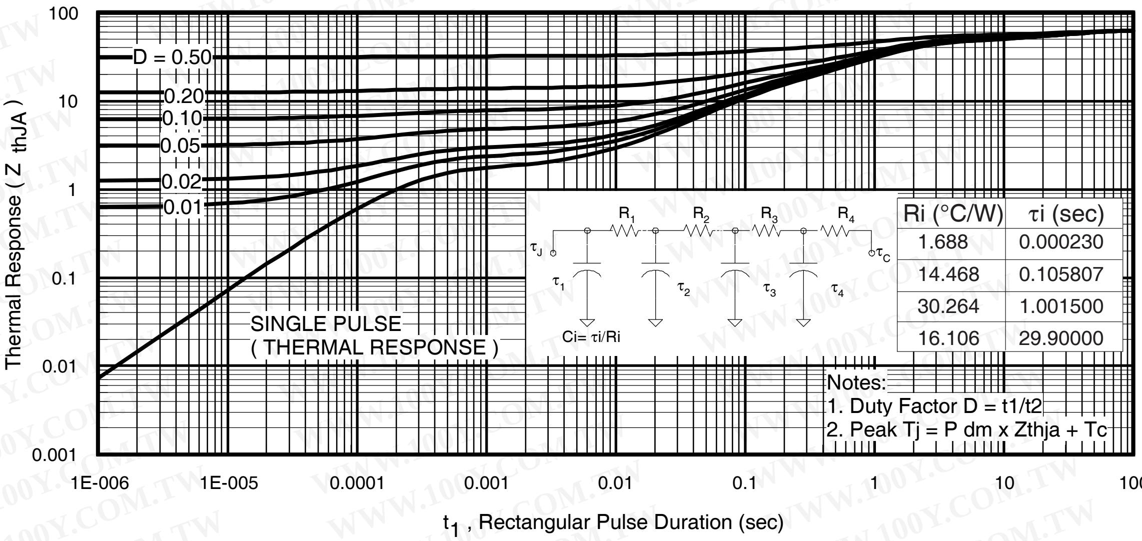


Fig 24. Maximum Avalanche Energy vs. Drain Current



Ri (°C/W)	τi (sec)
1.688	0.000230
14.468	0.105807
30.264	1.001500
16.106	29.90000

Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

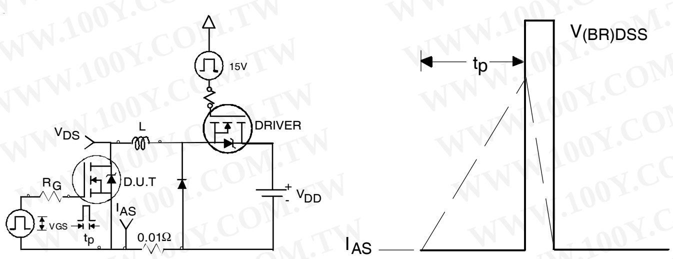


Fig 26. Unclamped Inductive Test Circuit and Waveform

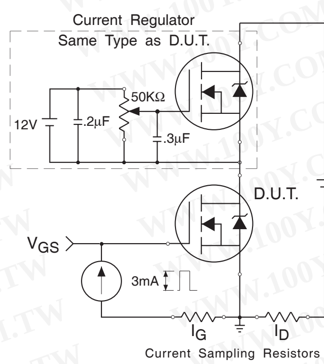


Fig 27. Gate Charge Test Circuit

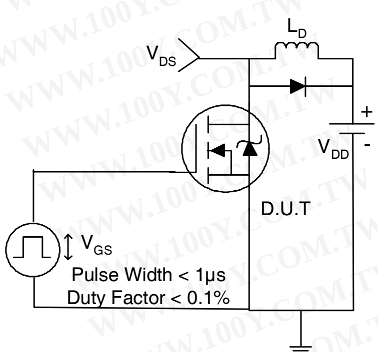


Fig 28. Switching Time Test Circuit

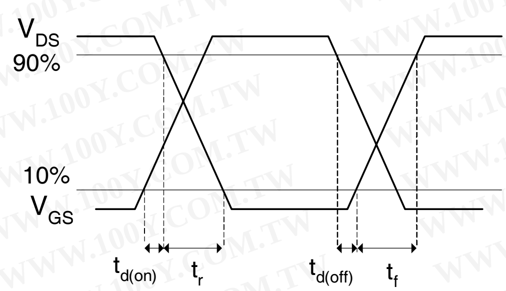
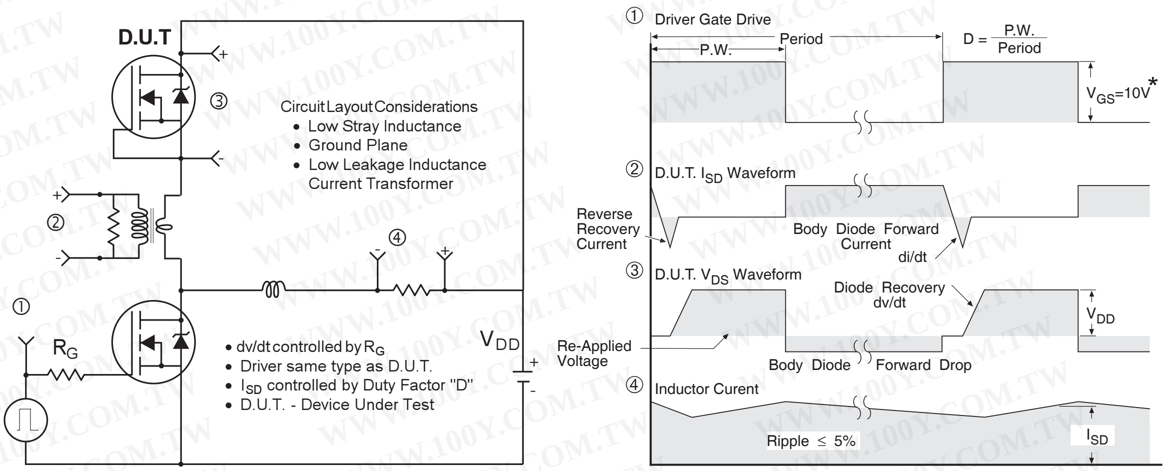


Fig 29. Switching Time Waveforms



* V_{GS} = 5V for Logic Level Devices

Fig 30. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

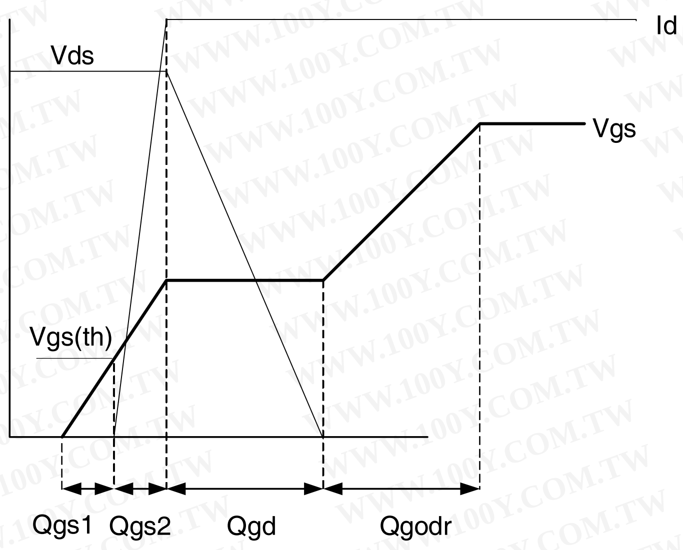
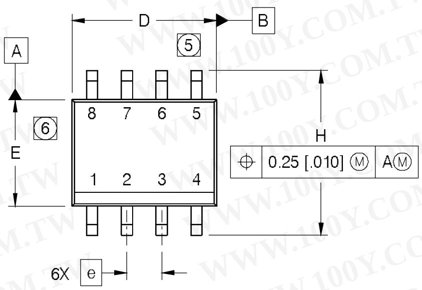


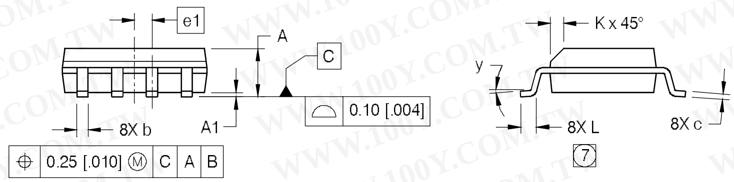
Fig 31. Gate Charge Waveform

SO-8 Package Outline(Mosfet & Fetky)

Dimensions are shown in milimeters (inches)

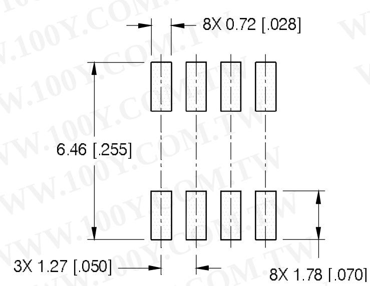


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



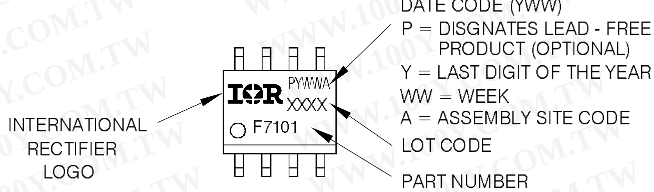
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information

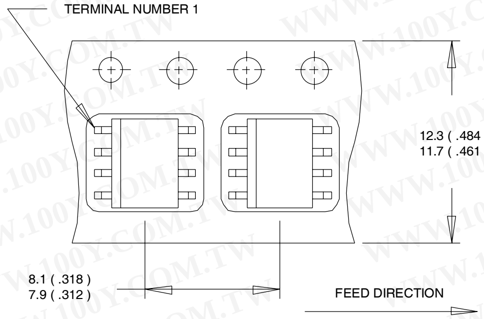
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



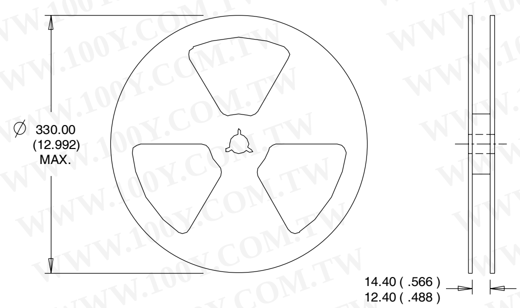
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, Q1: L = 0.95mH $R_G = 25\Omega$, $I_{AS} = 8.3A$; Q2: L = 0.54mH $R_G = 25\Omega$, $I_{AS} = 9.8A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

International IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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