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 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
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PD - 95473

International  
**IR** Rectifier

SMPS MOSFET

**IRFB260NPbF**

HEXFET® Power MOSFET

**Applications**

- High frequency DC-DC converters
- Lead-Free

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>200V</b>	<b>0.040Ω</b>	<b>56A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>oss</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	56	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	40	
I <sub>DM</sub>	Pulsed Drain Current ①	220	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	10	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.40	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient	—	62	

Notes ① through ③ are on page 8

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.040	$\Omega$	$V_{GS} = 10V, I_D = 34A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

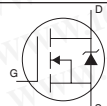
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	29	—	—	S	$V_{DS} = 50V, I_D = 34A$
$Q_g$	Total Gate Charge	—	150	220	nC	$I_D = 34A$
$Q_{gs}$	Gate-to-Source Charge	—	24	37		$V_{DS} = 160V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	67	100		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	17	—		$V_{DD} = 100V$
$t_r$	Rise Time	—	64	—	ns	$I_D = 34A$
$t_{d(off)}$	Turn-Off Delay Time	—	52	—		$R_G = 1.8\Omega$
$t_f$	Fall Time	—	50	—		$V_{GS} = 10V$ ④
$C_{iss}$	Input Capacitance	—	4220	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	580	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	140	—		$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	5080	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	230	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	500	—		$V_{GS} = 0V, V_{DS} = 0V\ \text{to}\ 160V$ ⑤

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	450	mJ
$I_{AR}$	Avalanche Current①	—	34	A
$E_{AR}$	Repetitive Avalanche Energy①	—	38	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	220		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 34A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	240	360	ns	$T_J = 25^\circ\text{C}, I_F = 34A$
$Q_{rr}$	Reverse Recovery Charge	—	2.1	3.2	$\mu\text{C}$	$di/dt = 100A/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

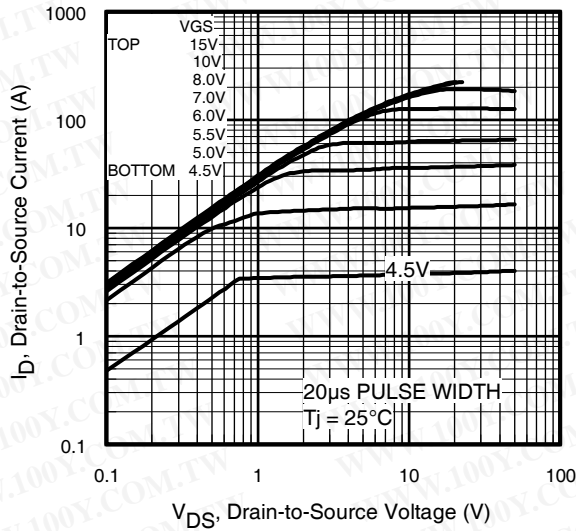


Fig 1. Typical Output Characteristics

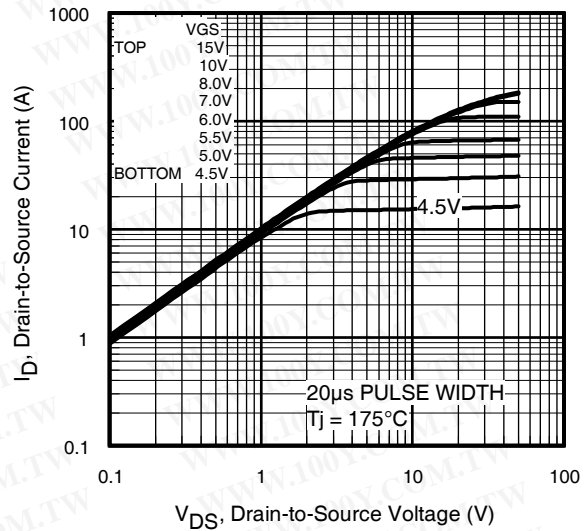


Fig 2. Typical Output Characteristics

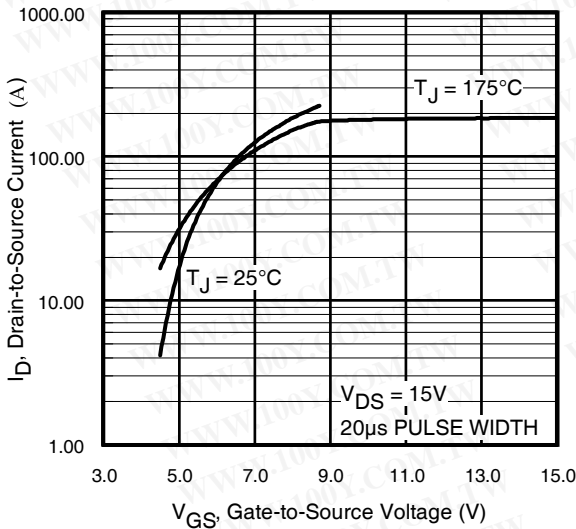


Fig 3. Typical Transfer Characteristics

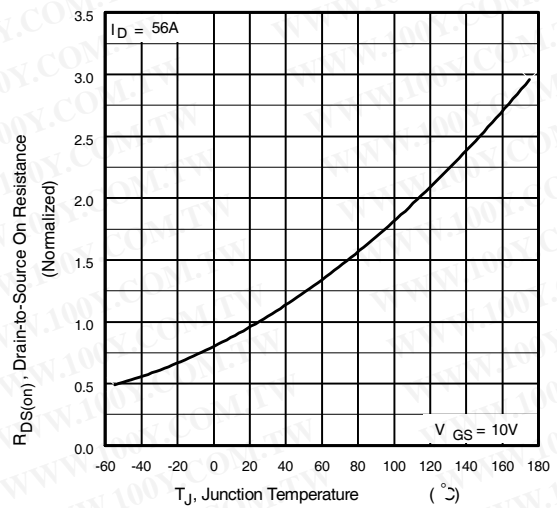
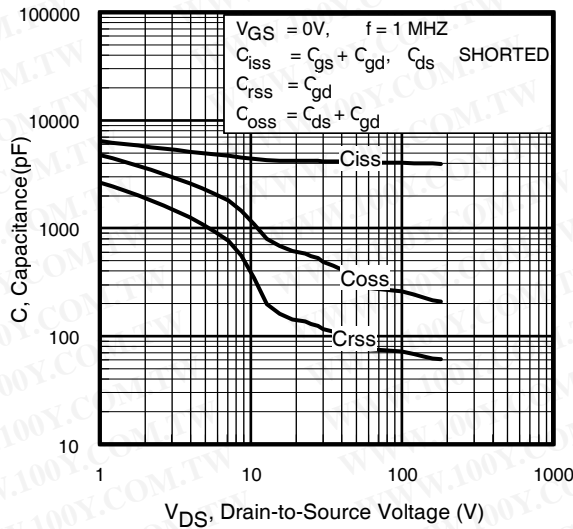


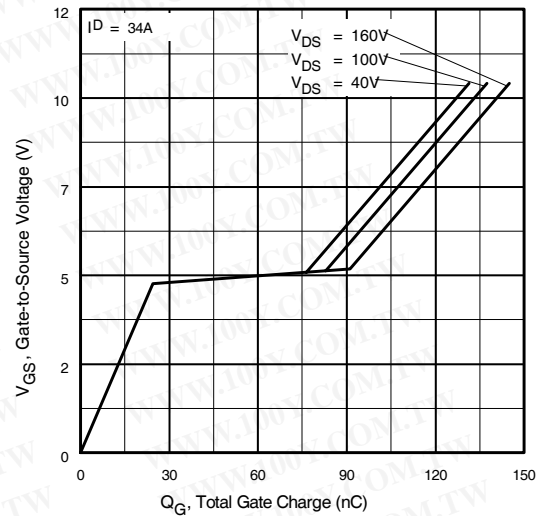
Fig 4. Normalized On-Resistance Vs. Temperature

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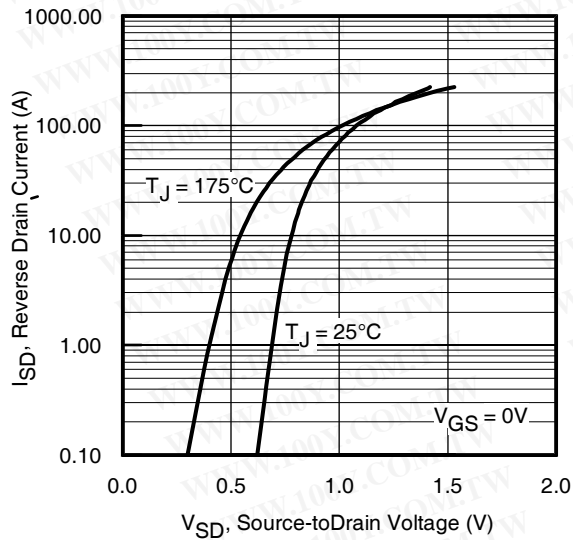
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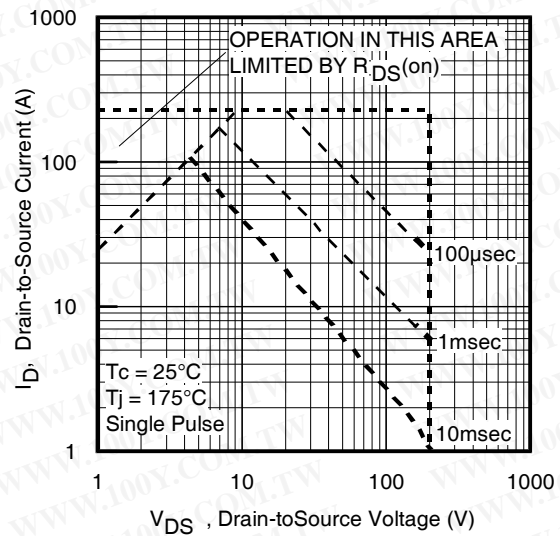
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



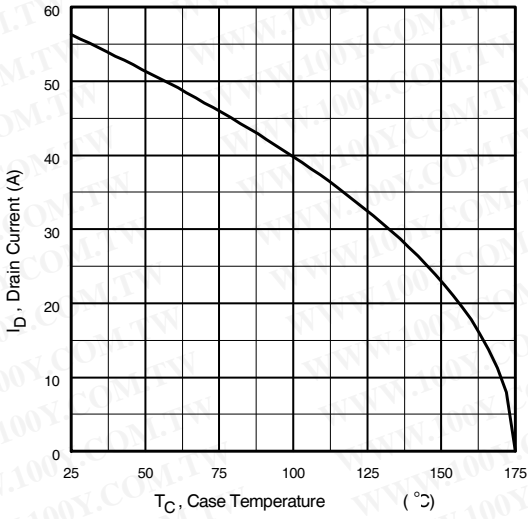
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



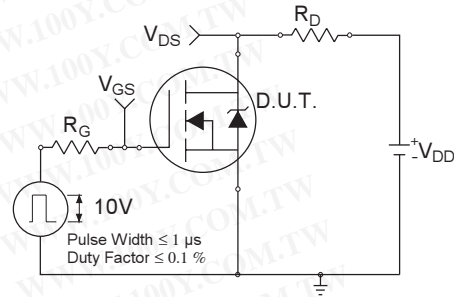
**Fig 7.** Typical Source-Drain Diode Forward Voltage



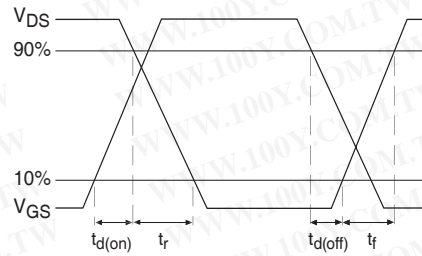
**Fig 8.** Maximum Safe Operating Area



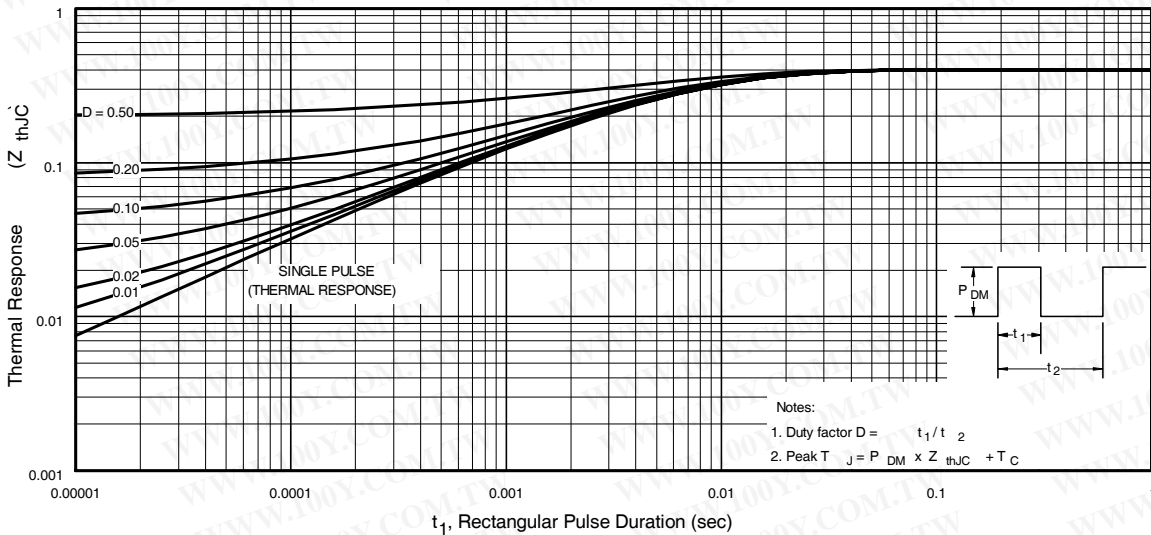
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



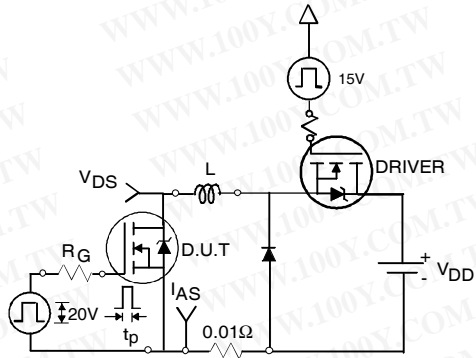
**Fig 10b.** Switching Time Waveforms



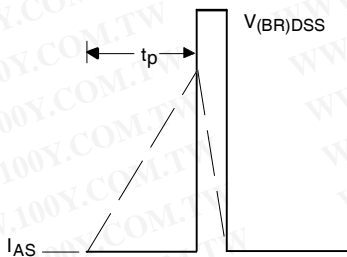
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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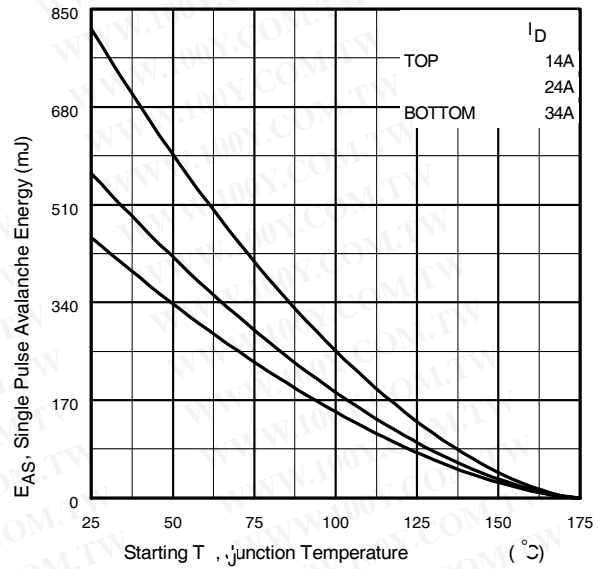
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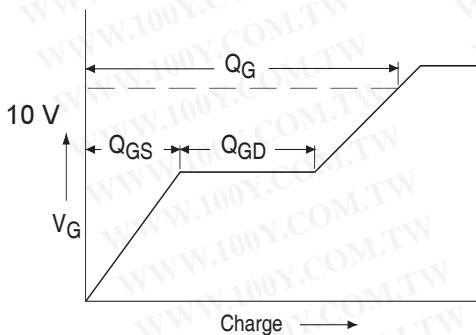
**Fig 12a.** Unclamped Inductive Test Circuit



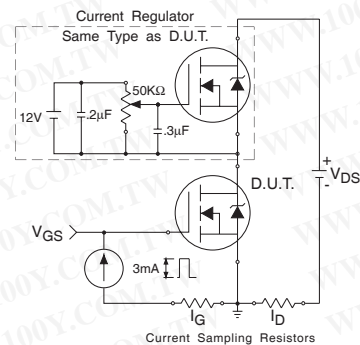
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



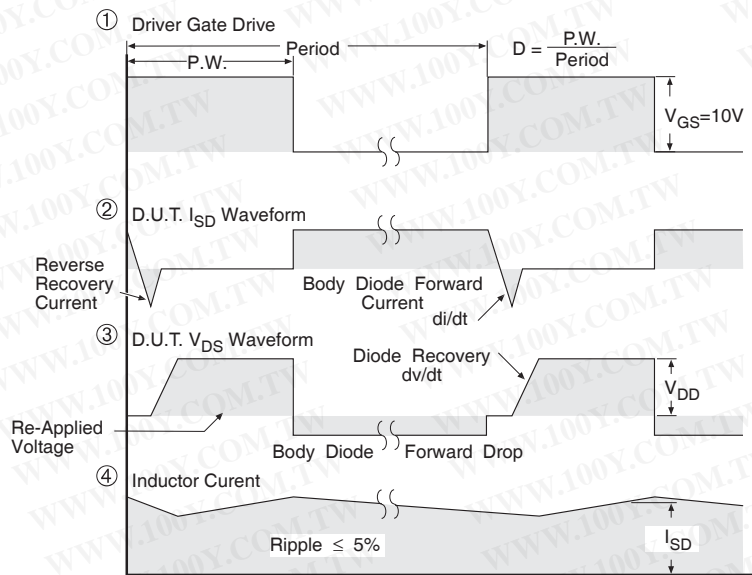
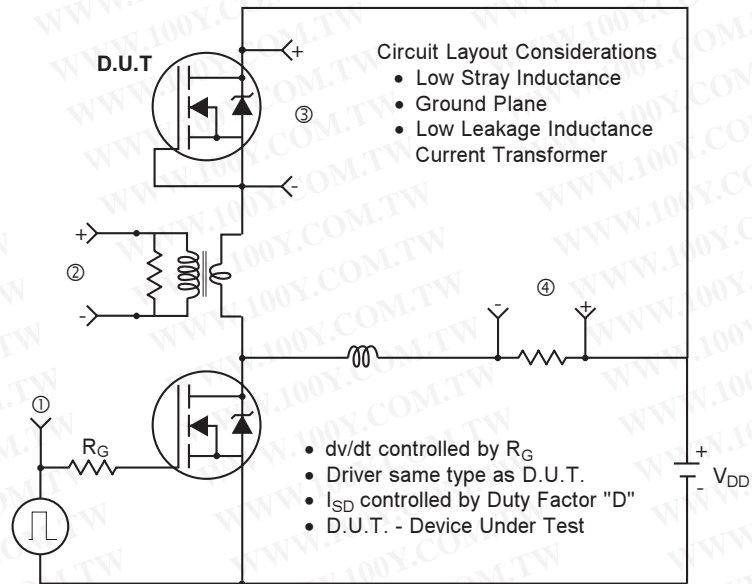
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

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## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

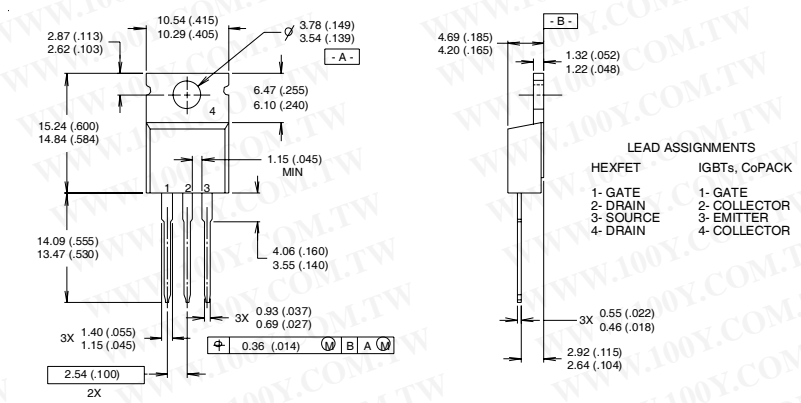
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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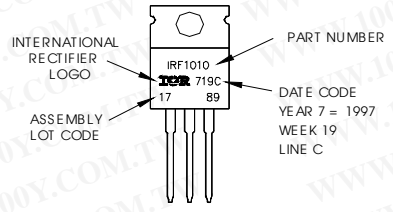
## TO-220AB Package Outline



NOTES:  
 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.  
 2 CONTROLLING DIMENSION : INCH  
 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.  
 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.78\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 34\text{A}$ .
- ③  $I_{SD} \leq 34$ ,  $di/dt \leq 480\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

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