PD - 95509A

International IR Rectifier

IRFP1405PbF

HEXFET® Power MOSFET

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

$V_{DSS} = 55V$

$R_{DS(on)} = 5.3m\Omega$

$I_D = 95A$

Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

TO-247AC
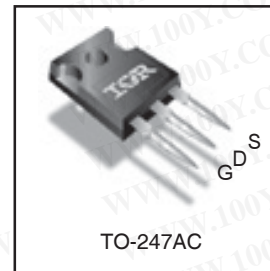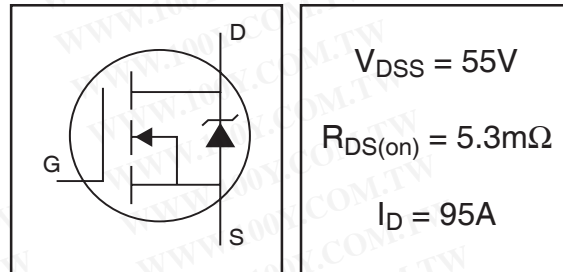
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	160	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	110	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	95	
I_{DM}	Pulsed Drain Current ①	640	
P_D @T_C = 25°C	Power Dissipation	310	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy②	530	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	1060	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case *	——	0.49	
$R_{\theta cs}$	Case-to-Sink, Flat, Greased Surface	0.24	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient *	——	40	

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* R_θ is measured at T_J approximately 90°C

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.058	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.2	5.3	mΩ	V_{GS} = 10V, I_D = 95A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
gfs	Forward Transconductance	77	——	——	S	V_{DS} = 25V, I_D = 95A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 55V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	120	180		I_D = 95A
Q_{gs}	Gate-to-Source Charge	——	30	——	nC	V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	53	——		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	——	12	——		V_{DD} = 28V
t_r	Rise Time	——	160	——		I_D = 95A
$t_{d(off)}$	Turn-Off Delay Time	——	140	——	ns	R_G = 2.6 Ω
t_f	Fall Time	——	150	——		V_{GS} = 10V ③
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	13	——		
C_{iss}	Input Capacitance	——	5600	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	1310	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	350	——	pF	f = 1.0MHz
C_{oss}	Output Capacitance	——	6550	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	920	——		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	1750	——		V_{GS} = 0V, V_{DS} = 0V to 44V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	95	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	640		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 95A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	70	110	ns	T_J = 25°C, I_F = 95A, V_{DD} = 28V
Q_{rr}	Reverse Recovery Charge	——	170	260	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.12mH R_G = 25Ω, I_{AS} = 95A, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

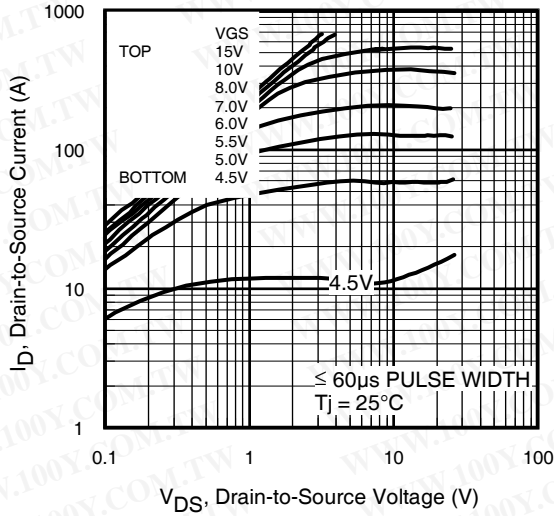⑥ This value determined from sample failure population. 100% tested to this value in production.
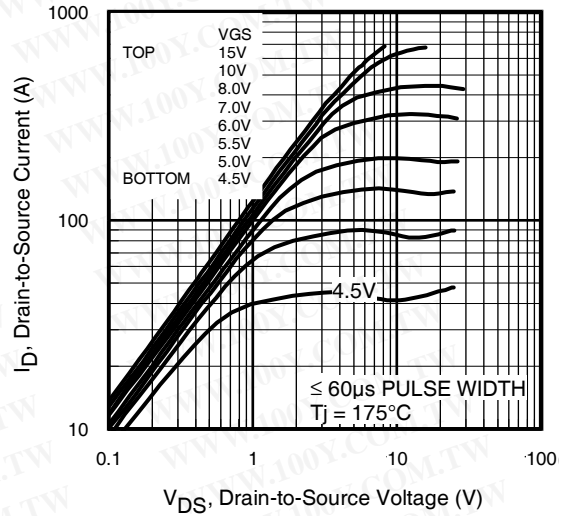
Fig 1. Typical Output Characteristics

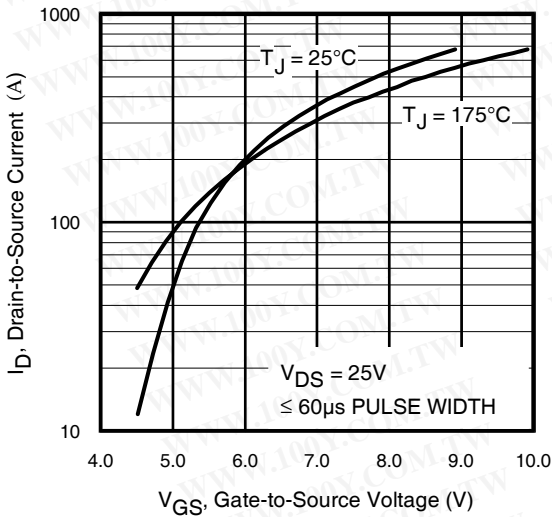**Fig 2.** Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

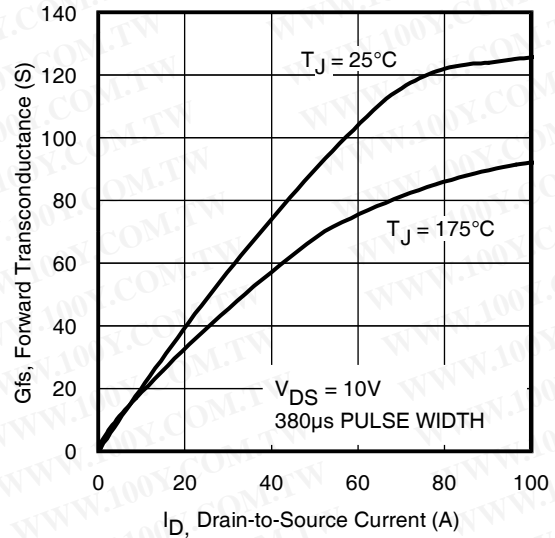**Fig 4.** Typical Forward Transconductance
Vs. Drain Current
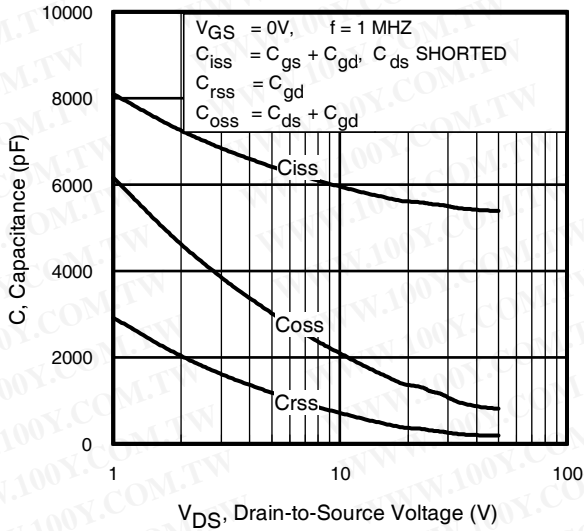
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Fig 5. Typical Capacitance Vs.
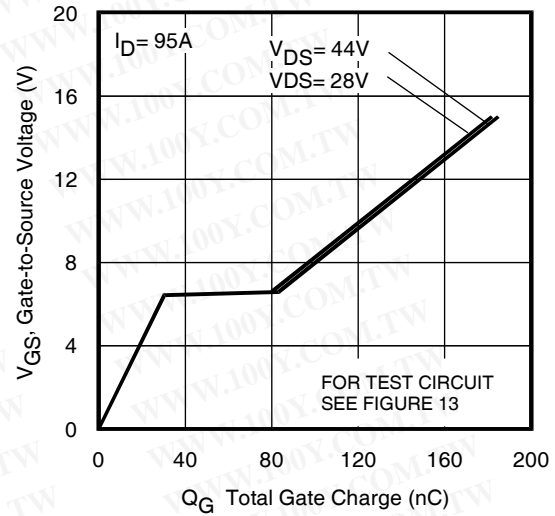Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

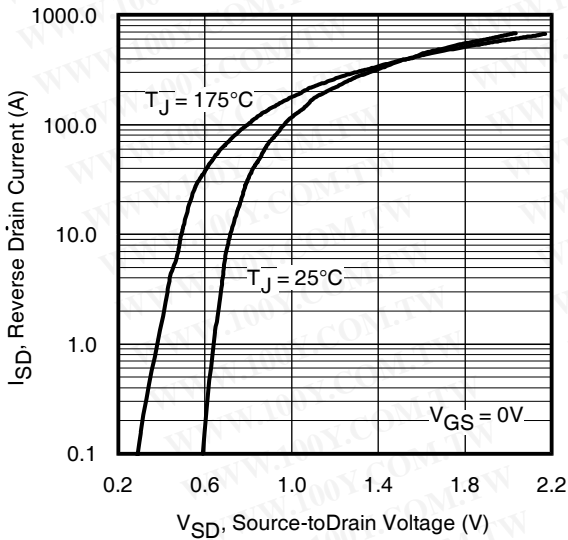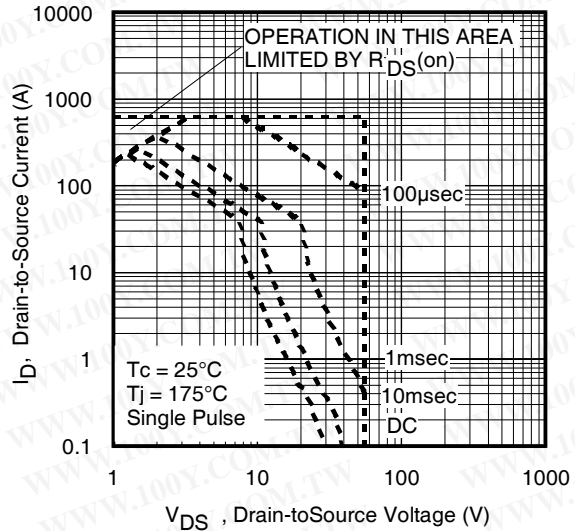**Fig 7.** Typical Source-Drain Diode
Forward Voltage

Fig 8. Maximum Safe Operating Area
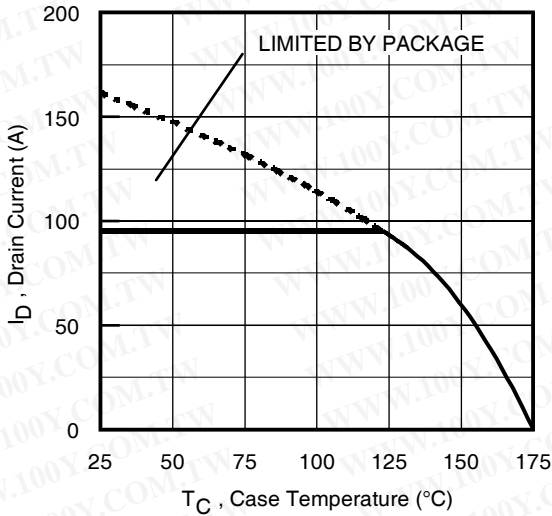
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Fig 9. Maximum Drain Current Vs. Case Temperature
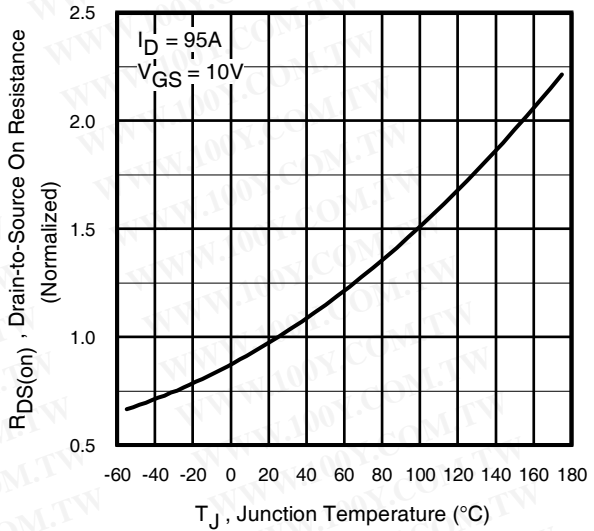
Fig 10. Normalized On-Resistance Vs. Temperature

Ri (°C/W)	τi (sec)
0.2529	0.00080
0.2368	0.014283

$C_i = \tau_i / R_i$

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

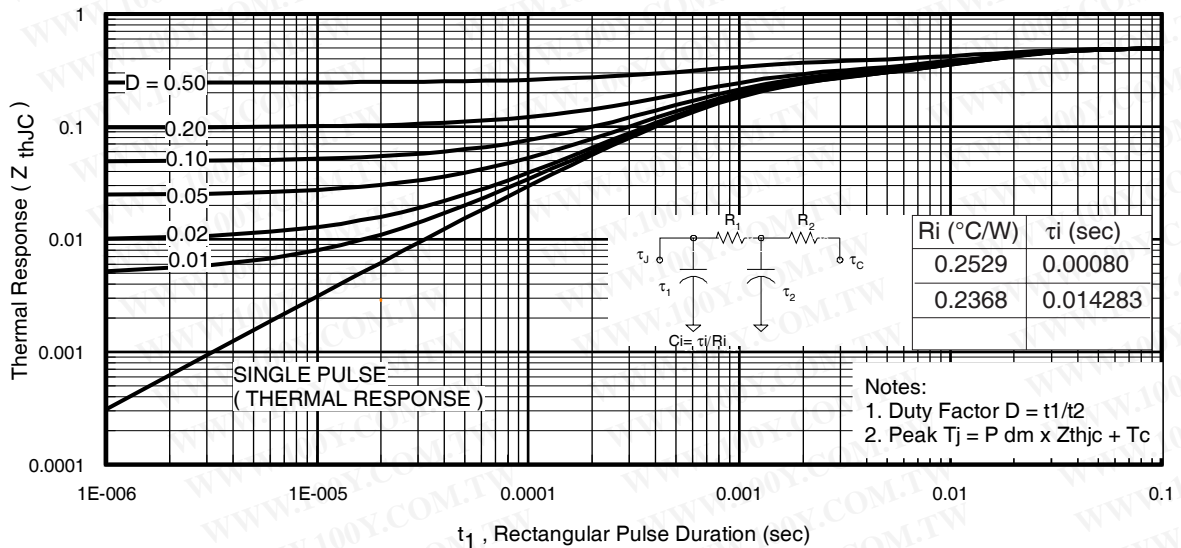**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case
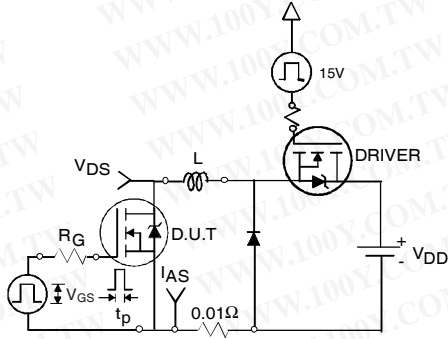
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Fig 12a. Unclamped Inductive Test Circuit
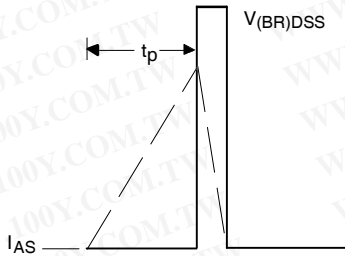

Fig 12b. Unclamped Inductive Waveforms
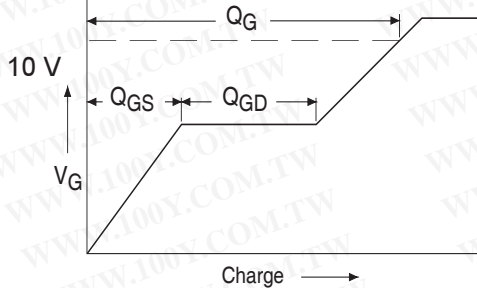
Fig 13a. Basic Gate Charge Waveform
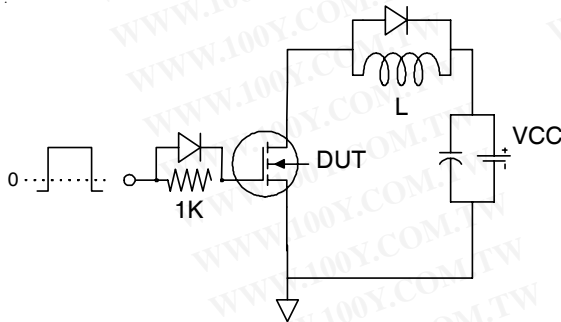
Fig 13b. Gate Charge Test Circuit

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$$I_D$$
TOP   16A
          20A
BOTTOM   95A
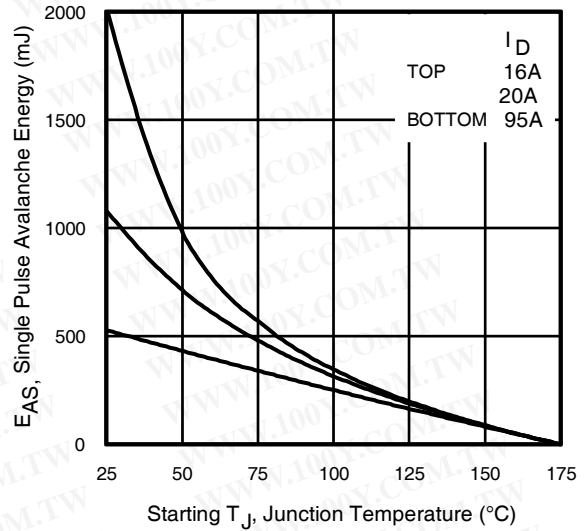
Fig 12c. Maximum Avalanche Energy
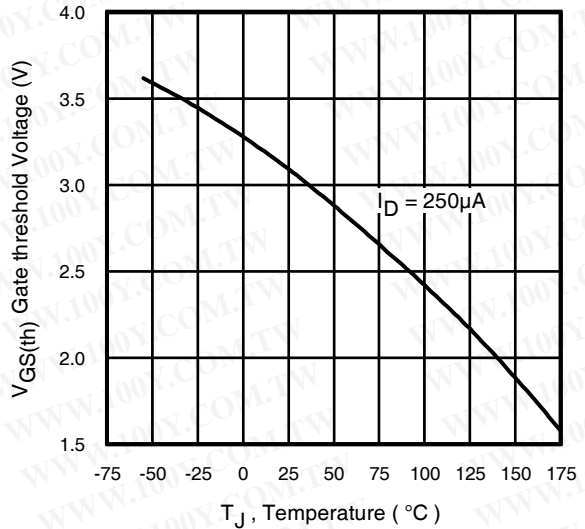Vs. Drain Current

$I_D = 250\mu A$

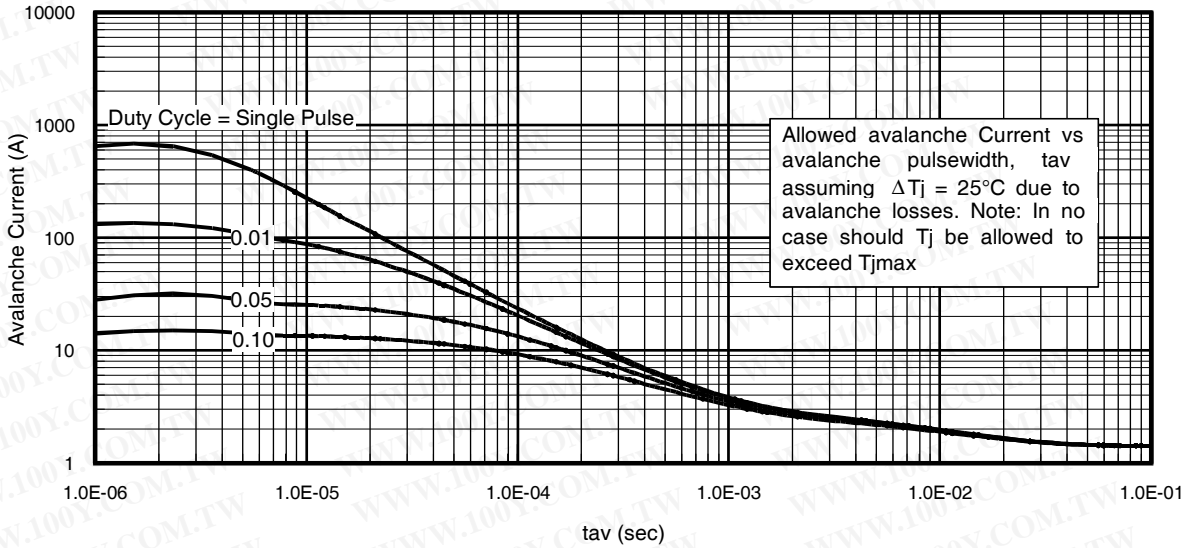**Fig 14.** Threshold Voltage Vs. Temperature

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Fig 15. Typical Avalanche Current Vs.Pulsewidth
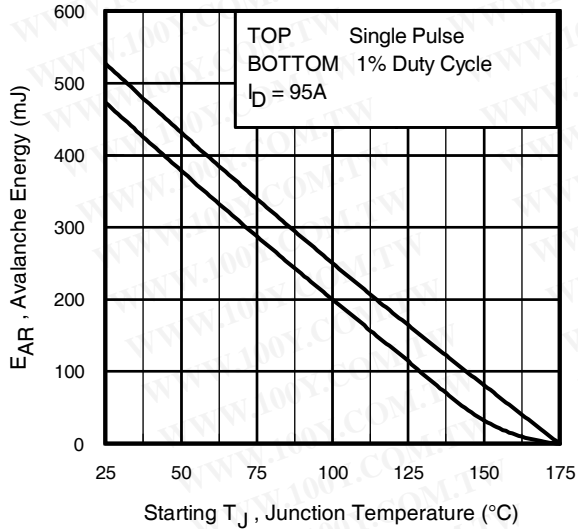
Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.

4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

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Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs

* V_{GS} = 5V for Logic Level Devices
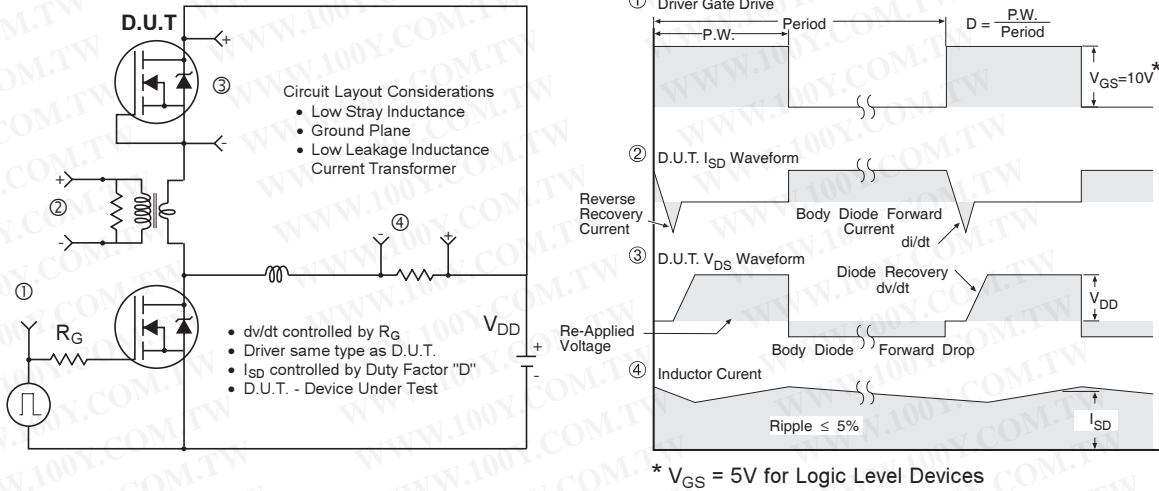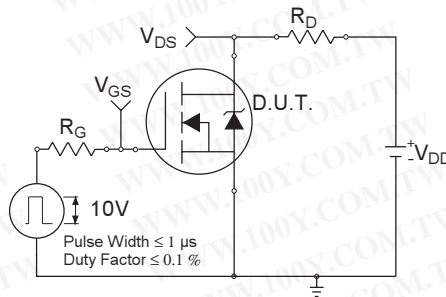

Fig 18a. Switching Time Test Circuit
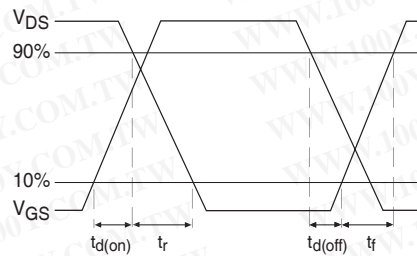
Fig 18b. Switching Time Waveforms

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TO-247AC Package Outline

Dimensions are shown in millimeters (inches)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

DIMENSIONS

SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.013	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.640	–	15.72	–	
e	.215 BSC		5.46 BSC		
øP	.100		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3				
Q	.140	.144	3.56	3.66	
øP1	–	.275	–	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

IGBTs, CoPACK
1 - GATE
2 - COLLECTOR
3 - EMITTER
4 - COLLECTOR

DIODES
1 - ANODE/OPEN
2 - CATHODE
3 - ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 35
LINE H

IRFPE30
ICR 035H
56 57
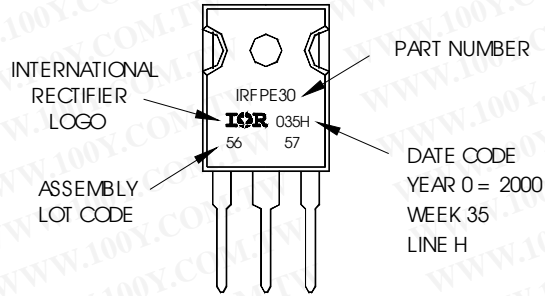
TO-247AC packages are not recommended for Surface Mount Application.

Notes:
1. For an Automotive Qualified version of this part please see http://www.irf.com/product-info/auto/
2. For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.

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