



Power MOSFET

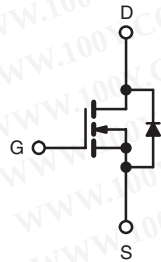
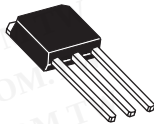
PRODUCT SUMMARY

V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.8
Q_g (Max.) (nC)	20	
Q_{gs} (nC)	3.3	
Q_{gd} (nC)	11	
Configuration	Single	

DPAK
(TO-252)



IPAK
(TO-251)



N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR320/SiHFR320)
- Straight Lead (IRFU320/SiHFU320)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR320PbF	IRFR320TRLPbF ^a	IRFR320TRPbF ^a	IRFR320TRRPbF ^a	IRFU320PbF
	SiHFR320-E3	SiHFR320TL-E3 ^a	SiHFR320T-E3 ^a	SiHFR320TR-E3 ^a	SiHFU320-E3
SnPb	IRFR320	IRFR320TRL ^a	IRFR320TR ^a	IRFR320TRR ^a	IRFU320
	SiHFR320	SiHFR320TL ^a	SiHFR320T ^a	SiHFR320TR ^a	SiHFU320

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	400	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	I_D	3.1	A
		$T_C = 100^\circ\text{C}$		2.0	
Pulsed Drain Current ^a			I_{DM}	12	
Linear Derating Factor				0.33	W/ $^\circ\text{C}$
Linear Derating Factor (PCB Mount) ^e				0.020	
Single Pulse Avalanche Energy ^b			E_{AS}	160	mJ
Repetitive Avalanche Current ^a			I_{AR}	3.1	A
Repetitive Avalanche Energy ^a			E_{AR}	4.2	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$		P_D	42	W
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25^\circ\text{C}$			2.5	
Peak Diode Recovery dV/dt ^c			dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)		for 10 s		260 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 29\text{ mH}$, $R_G = 25\ \Omega$, $I_{AS} = 3.1\text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.1\text{ A}$, $dI/dt \leq 65\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- * Pb containing terminations are not RoHS compliant, exemptions may apply

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THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		400	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.51	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.9 A ^b	-	-	1.8	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.9 A		1.7	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	350	-	pF
Output Capacitance	C _{oss}			-	120	-	
Reverse Transfer Capacitance	C _{rss}			-	47	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 3.3 A, V _{DS} = 320 V, see fig. 6 and 13 ^b	-	-	20	nC
Gate-Source Charge	Q _{gs}			-	-	3.3	
Gate-Drain Charge	Q _{gd}			-	-	11	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 200 V, I _D = 3.3 A, R _G = 18 Ω, R _D = 56 Ω, see fig. 10 ^b		-	10	-	ns
Rise Time	t _r			-	14	-	
Turn-Off Delay Time	t _{d(off)}			-	30	-	
Fall Time	t _f			-	13	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.1	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	12	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 3.1 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 3.3 A, dI/dt = 100 A/μs ^b		-	270	600	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.4	3.0	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

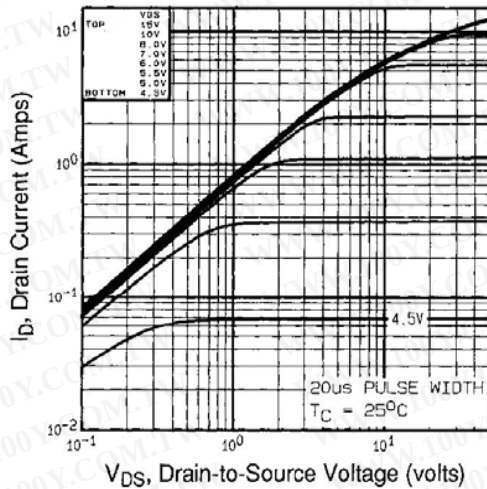


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

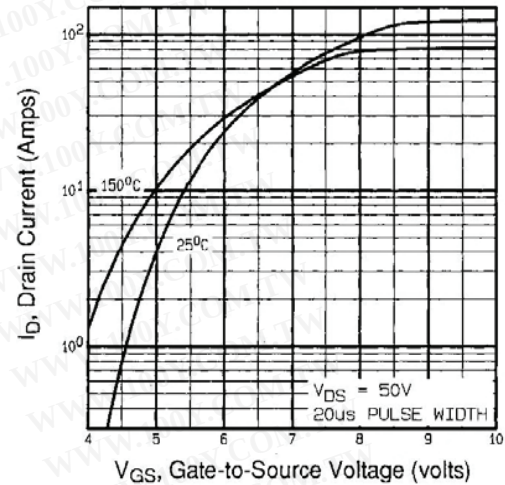


Fig. 3 - Typical Transfer Characteristics

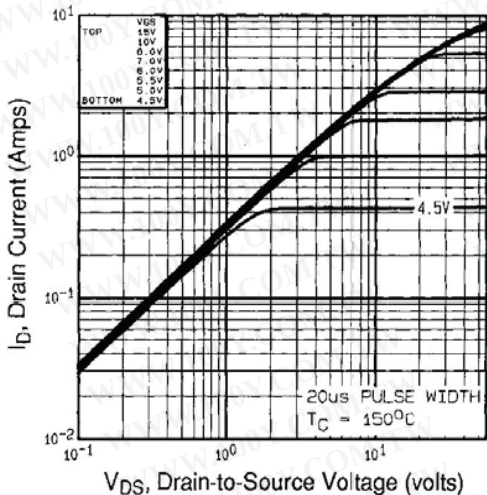


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

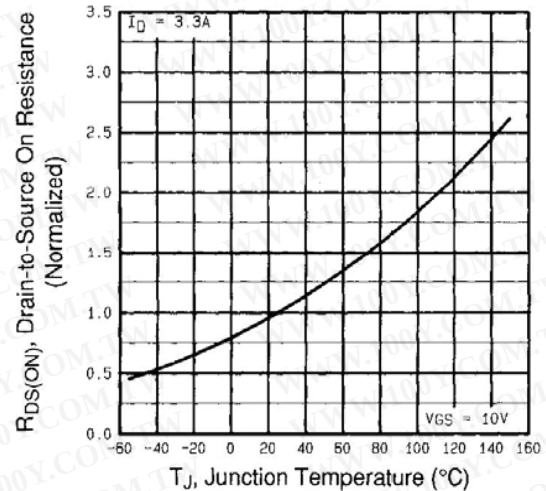


Fig. 4 - Normalized On-Resistance vs. Temperature

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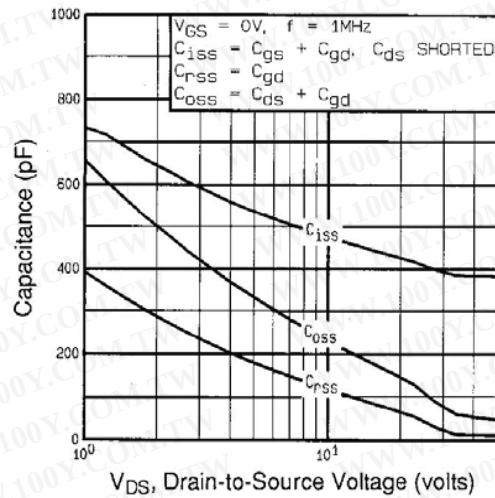


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

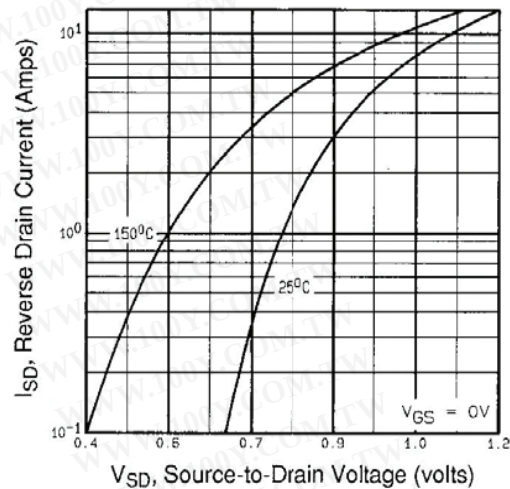


Fig. 7 - Typical Source-Drain Diode Forward Voltage

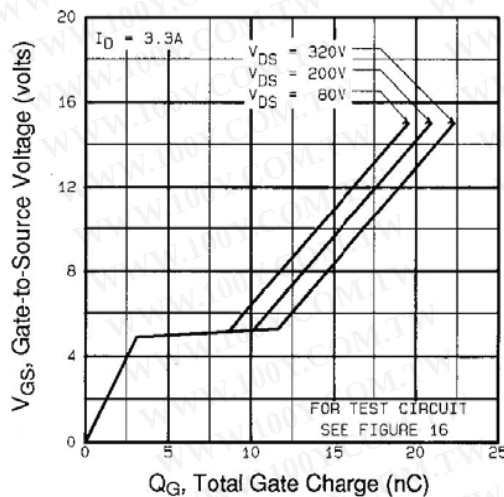


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

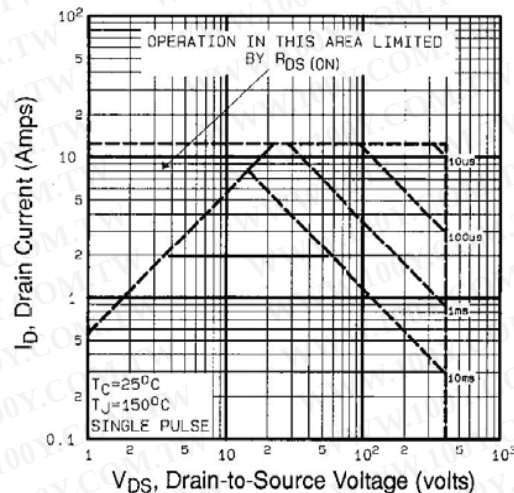


Fig. 8 - Maximum Safe Operating Area

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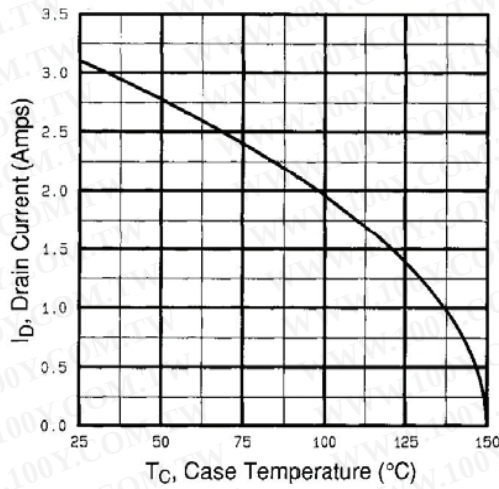


Fig. 9 - Maximum Drain Current vs. Case Temperature

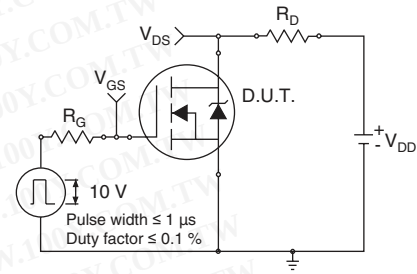


Fig. 10a - Switching Time Test Circuit

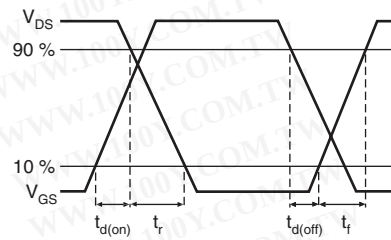


Fig. 10b - Switching Time Waveforms

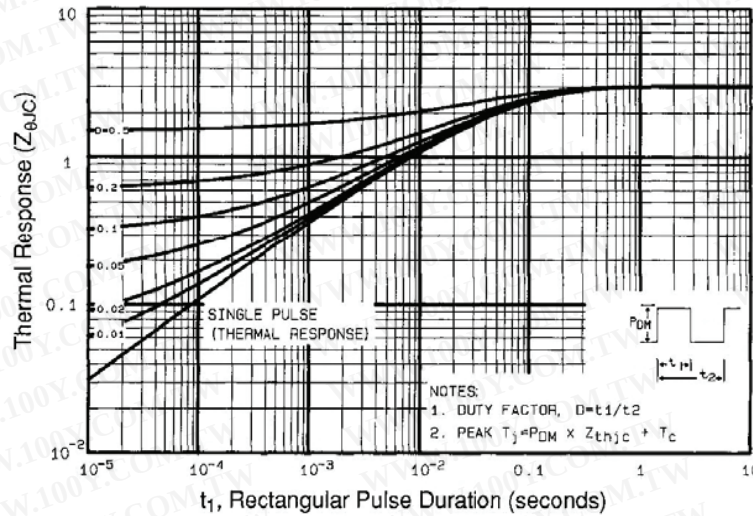


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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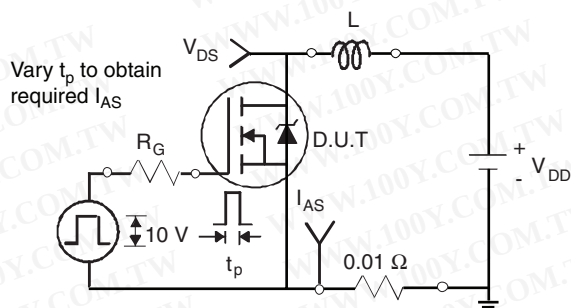


Fig. 12a - Unclamped Inductive Test Circuit

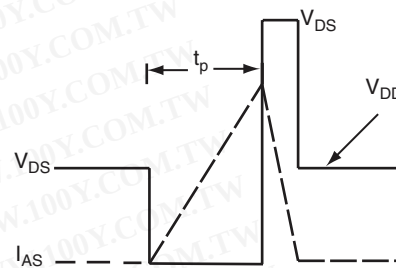


Fig. 12b - Unclamped Inductive Waveforms

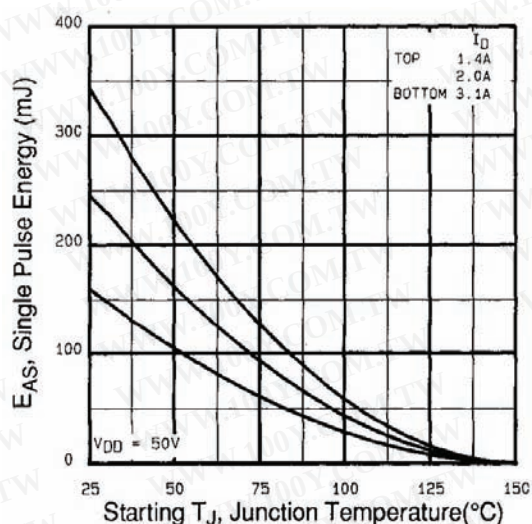


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

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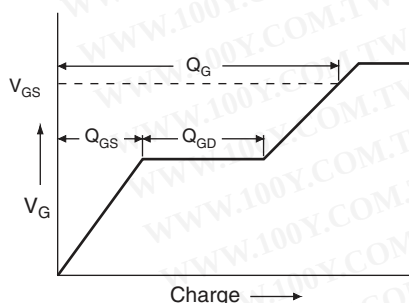


Fig. 13a - Basic Gate Charge Waveform

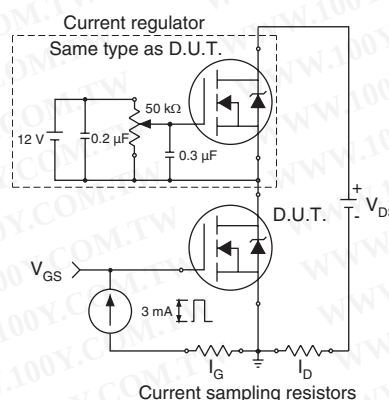


Fig. 13b - Gate Charge Test Circuit

Fig. 14 - For N-Channel



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