

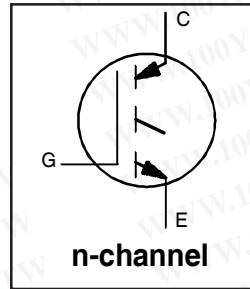
International **IR** Rectifier

IRG4PC30WPbF

INSULATED GATE BIPOLAR TRANSISTOR

Features

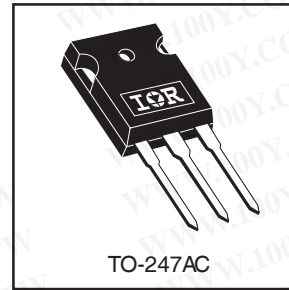
- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Lead-Free



$V_{CES} = 600V$
$V_{CE(on) \max.} = 2.70V$
@ $V_{GE} = 15V, I_C = 12A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	23	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	12	
I_{CM}	Pulsed Collector Current ①	92	
I_{LM}	Clamped Inductive Load Current ②	92	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	180	mJ
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	100	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	42	
T_J	Operating Junction and Storage Temperature Range	-55 to + 150	°C
T_{STG}			
	Mounting torque, 6-32 or M3 screw.	10 lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6 (0.21)	—	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	$V_{GE} = 0V, I_C = 1.0A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.34	—	V/°C	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.1	2.7	V	$I_C = 12A$ $I_C = 23A$ $I_C = 12A, T_J = 150^\circ\text{C}$ $V_{GE} = 15V$ See Fig.2, 5
		—	2.45	—		
		—	1.95	—		
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ⑤	11	16	—	S	$V_{CE} = 100V, I_C = 12A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$ $V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$ $V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
		—	—	2.0		
		—	—	1000		
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	51	76	nC	$I_C = 12A$ $V_{CC} = 400V$ $V_{GE} = 15V$ See Fig.8
Q_{ge}	Gate - Emitter Charge (turn-on)	—	7.6	11		
Q_{gc}	Gate - Collector Charge (turn-on)	—	18	27		
$t_{d(on)}$	Turn-On Delay Time	—	25	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 12A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail" See Fig. 10, 11, 13, 14
t_r	Rise Time	—	16	—		
$t_{d(off)}$	Turn-Off Delay Time	—	99	150		
t_f	Fall Time	—	67	100		
E_{on}	Turn-On Switching Loss	—	0.13	—		
E_{off}	Turn-Off Switching Loss	—	0.13	—	mJ	See Fig. 10, 11, 13, 14
E_{ts}	Total Switching Loss	—	0.26	0.35		
$t_{d(on)}$	Turn-On Delay Time	—	24	—	ns	$T_J = 150^\circ\text{C}$, $I_C = 12A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 23\Omega$ Energy losses include "tail" See Fig. 13, 14
t_r	Rise Time	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	—	150	—		
t_f	Fall Time	—	150	—		
E_{ts}	Total Switching Loss	—	0.55	—		
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	980	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$ See Fig. 7
C_{oes}	Output Capacitance	—	71	—		
C_{res}	Reverse Transfer Capacitance	—	18	—		

Notes:

- ① Repetitive rating; $V_{GE} = 20V$, pulse width limited by max. junction temperature. (See fig. 13b)
- ② $V_{CC} = 80\%(V_{CES})$, $V_{GE} = 20V$, $L = 10\mu H$, $R_G = 23\Omega$, (See fig. 13a)
- ③ Repetitive rating; pulse width limited by maximum junction temperature.
- ④ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ⑤ Pulse width $5.0\mu s$, single shot.

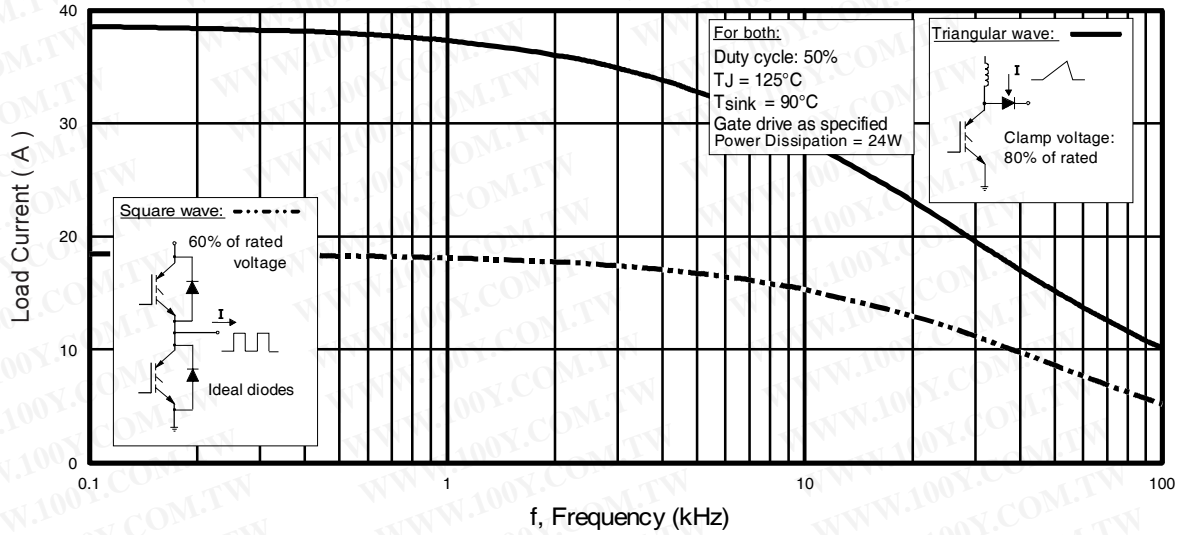


Fig. 1 - Typical Load Current vs. Frequency
 (For square wave, $I = I_{RMS}$ of fundamental; for triangular wave, $I = I_{PK}$)

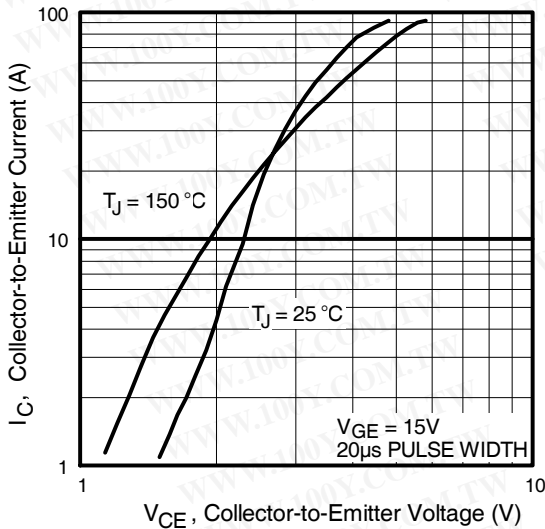


Fig. 2 - Typical Output Characteristics

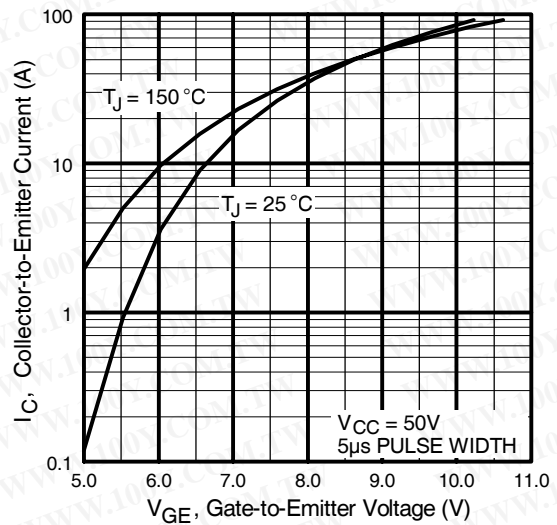


Fig. 3 - Typical Transfer Characteristics

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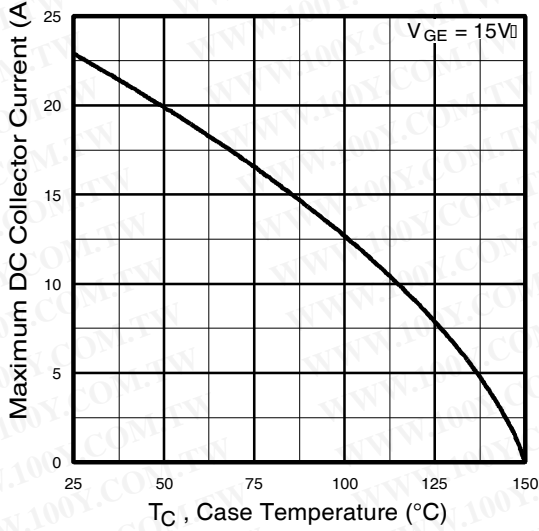


Fig. 4 - Maximum Collector Current vs. Case Temperature

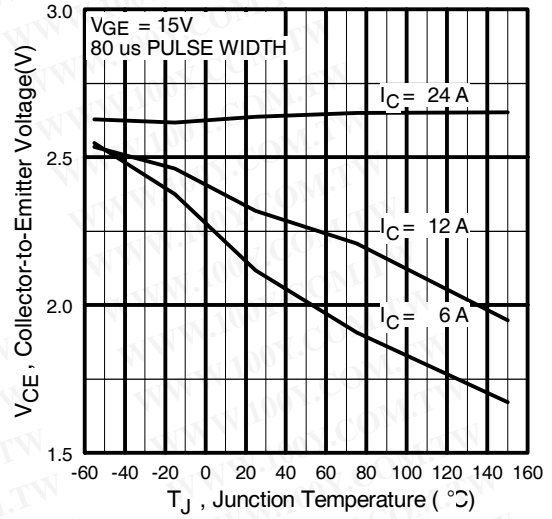


Fig. 5 - Collector-to-Emitter Voltage vs. Junction Temperature

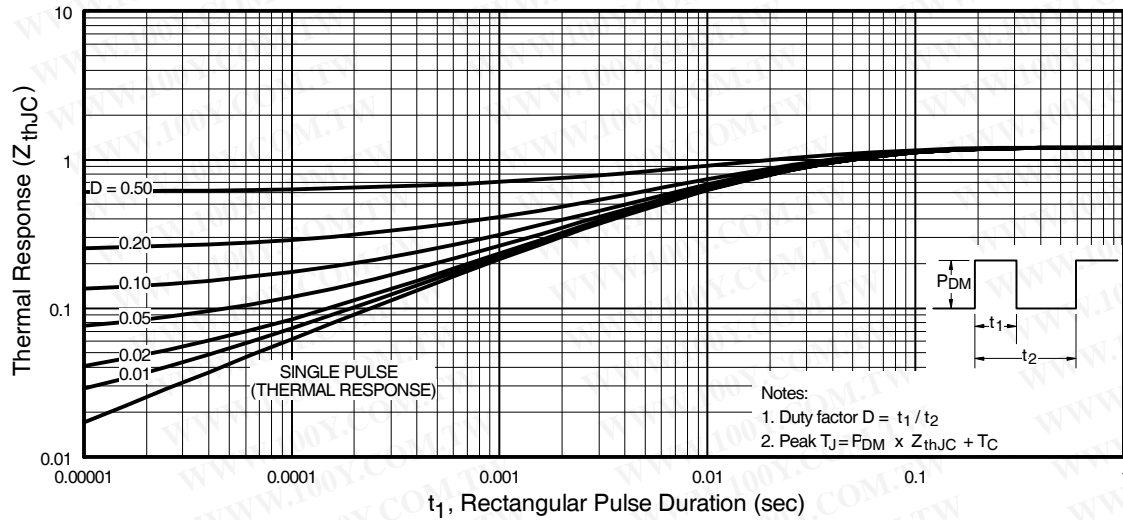


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

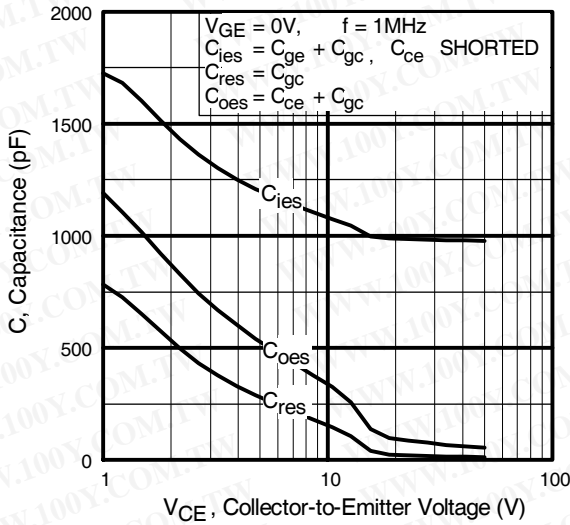


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

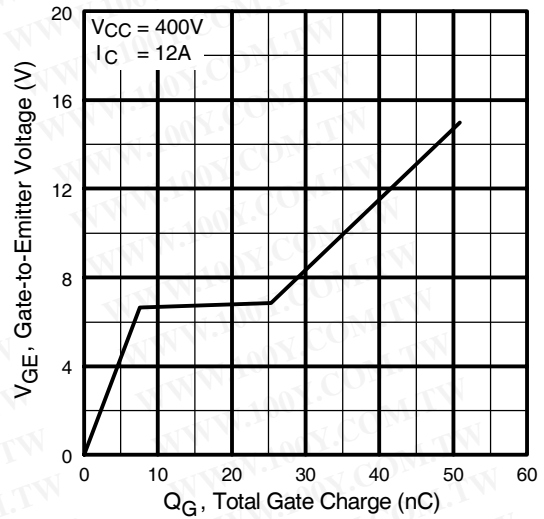


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

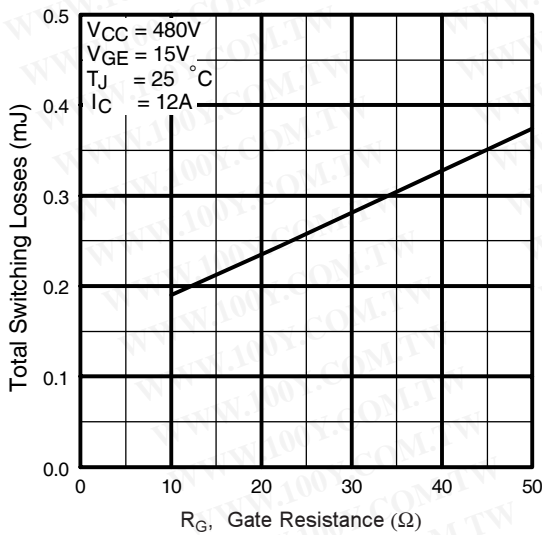


Fig. 9 - Typical Switching Losses vs. Gate Resistance

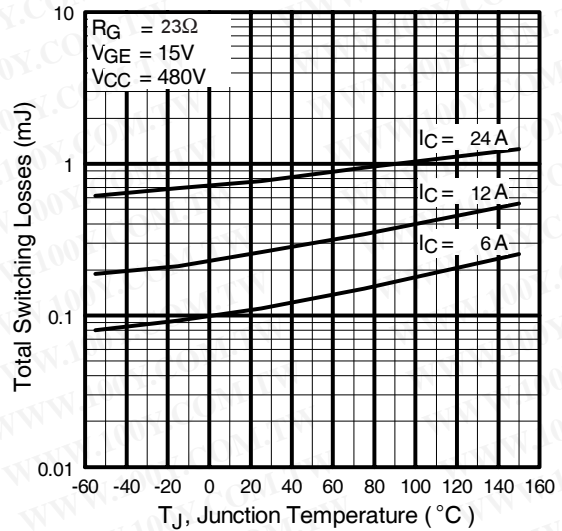


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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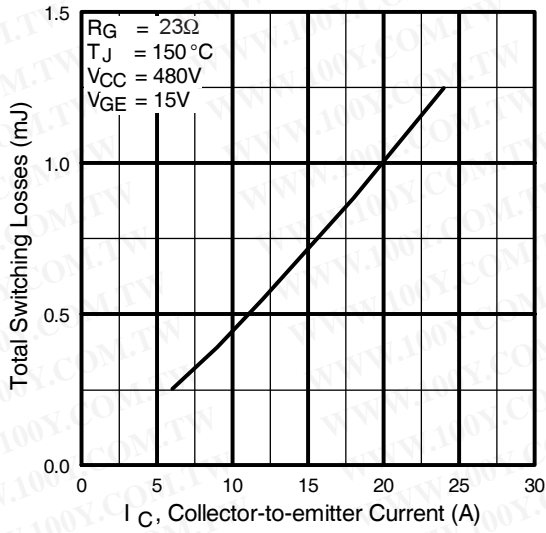


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

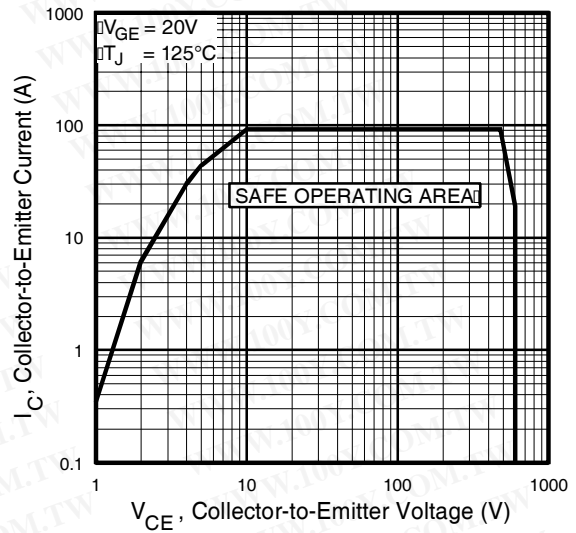
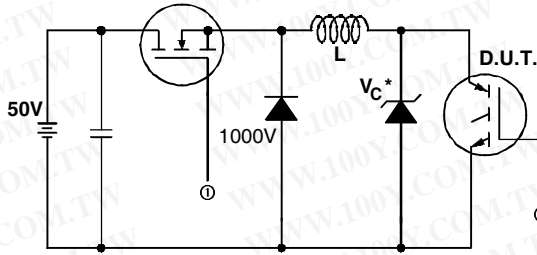


Fig. 12 - Turn-Off SOA



* Driver same type as D.U.T.; $V_c = 80\%$ of $V_{ce(max)}$
 * Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated I_d .

Fig. 13a - Clamped Inductive Load Test Circuit

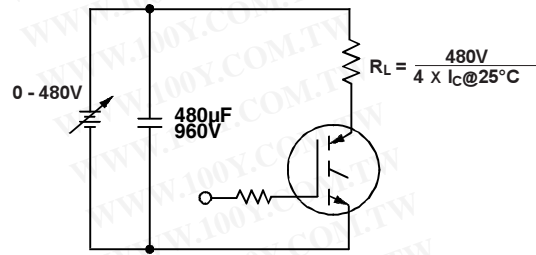


Fig. 13b - Pulsed Collector Current Test Circuit

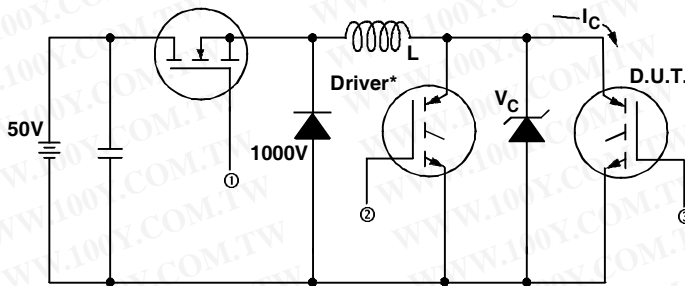


Fig. 14a - Switching Loss Test Circuit

* Driver same type as D.U.T., $V_c = 480V$

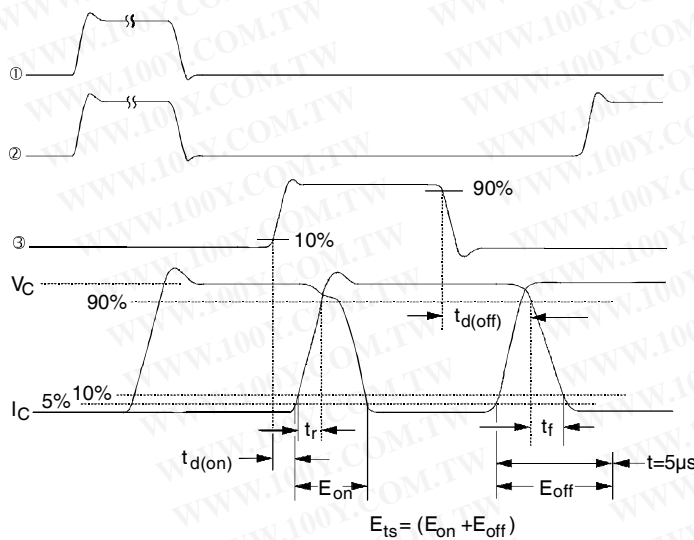


Fig. 14b - Switching Loss Waveforms

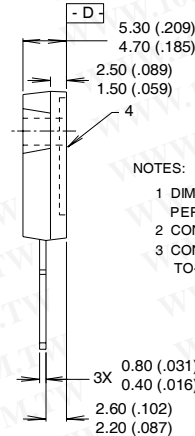
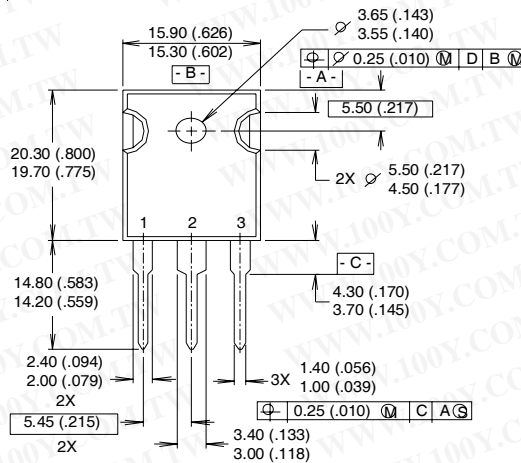
勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
 勝特力电子(深圳) 86-755-83298787
 Http://www.100y.com.tw

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TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

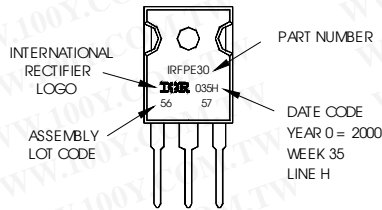
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

LEAD ASSIGNMENTS

Hexfet	IGBT
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
 WITH ASSEMBLY
 LOT CODE 5667
 ASSEMBLED ON WW 35, 2000
 IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line
 position indicates "Lead-Free"



Data and specifications subject to change without notice.

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