



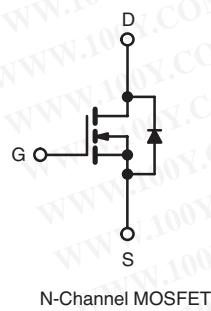
勝特力材料 886-3-5753170
 胜特力电子(上海) 86-21-54151736
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IRL510, SiHL510

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0$ V 0.54
Q_g (Max.) (nC)	6.1
Q_{gs} (nC)	2.6
Q_{gd} (nC)	3.3
Configuration	Single



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available



RoHS*

COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRL510PbF SiHL510-E3
SnPb	IRL510 SiHL510

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current	I_D	5.6	A
		4.0	
Pulsed Drain Current ^a	I_{DM}	18	
Linear Derating Factor		0.29	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	100	mJ
Repetitive Avalanche Current ^c	I_{AR}	5.6	A
Repetitive Avalanche Energy ^a	E_{AR}	4.3	mJ
Maximum Power Dissipation	P_D	43	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 4.8$ mH, $R_G = 25$ Ω, $I_{AS} = 5.6$ A (see fig. 12).
- $I_{SD} \leq 5.6$ A, $dI/dt \leq 75$ A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

SPECIFICATIONS $T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		100	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$, $I_D = 1 \text{ mA}$		-	0.12	-	$\text{V}/^{\circ}\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		1.0	-	2.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10 \text{ V}$		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA	
		$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 150 \text{ }^{\circ}\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0 \text{ V}$	$I_D = 3.4 \text{ A}^b$	-	-	0.54	Ω	
		$V_{GS} = 4.0 \text{ V}$	$I_D = 2.8 \text{ A}^b$	-	-	0.76		
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$, $I_D = 3.4 \text{ A}^b$		1.9	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	250	-	pF	
Output Capacitance	C_{oss}			-	80	-		
Reverse Transfer Capacitance	C_{rss}			-	15	-		
Total Gate Charge	Q_g	$V_{GS} = 5.0 \text{ V}$	$I_D = 5.6 \text{ A}$, $V_{DS} = 80 \text{ V}$ see fig. 6 and 13 ^b	-	-	6.1	nC	
Gate-Source Charge	Q_{gs}			-	-	2.6		
Gate-Drain Charge	Q_{gd}			-	-	3.3		
Turn-On Delay Time	$t_{d(on)}$			-	9.3	-		
Rise Time	t_r	$V_{DD} = 50 \text{ V}$, $I_D = 5.6 \text{ A}$ $R_G = 12 \Omega$, $R_D = 8.4 \Omega$ see fig. 10 ^b		-	47	-	ns	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-		
Fall Time	t_f			-	18	-		
Internal Drain Inductance	L_D			-	4.5	-		
Internal Source Inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5	-	nH	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.6	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	18		
Body Diode Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 5.6 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	2.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = 5.6 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	110	130	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.50	0.65	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

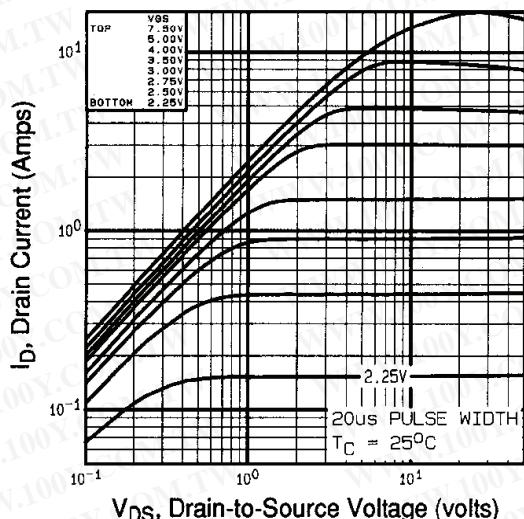


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

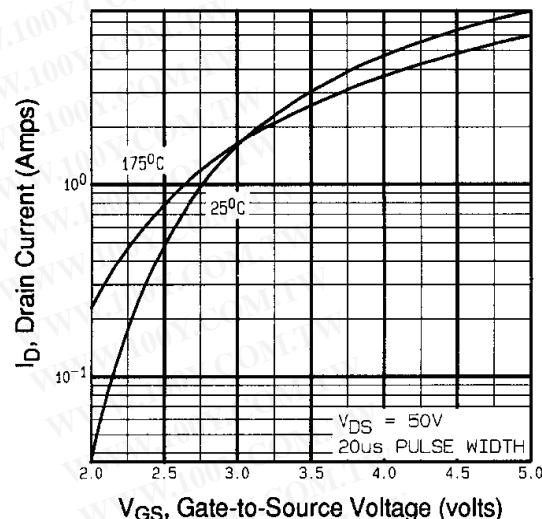


Fig. 3 - Typical Transfer Characteristics

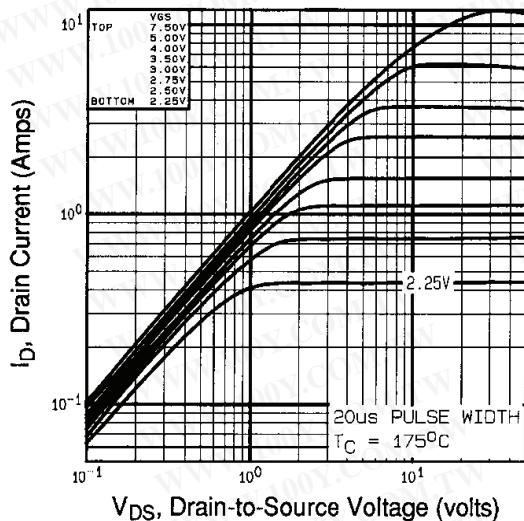


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

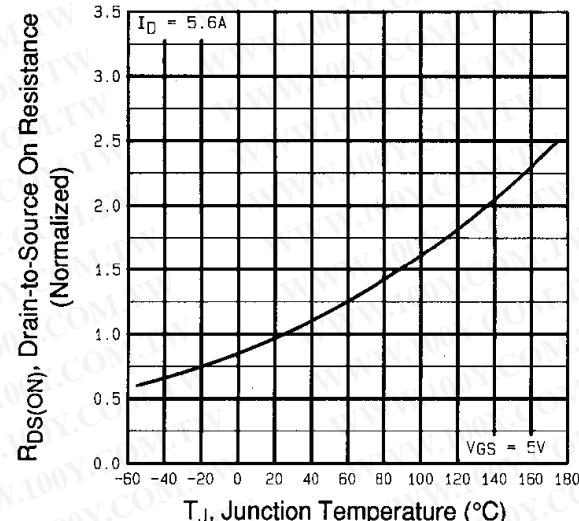


Fig. 4 - Normalized On-Resistance vs. Temperature

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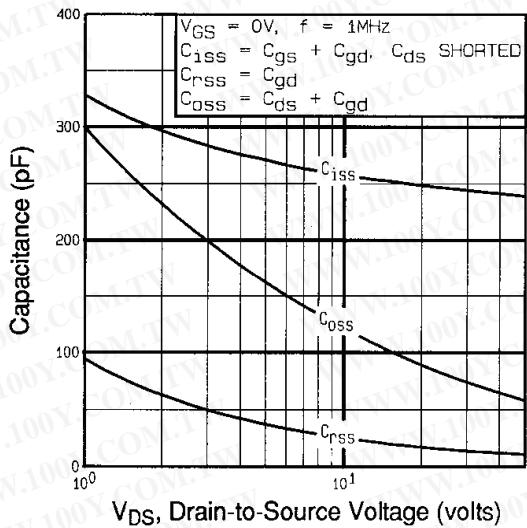


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

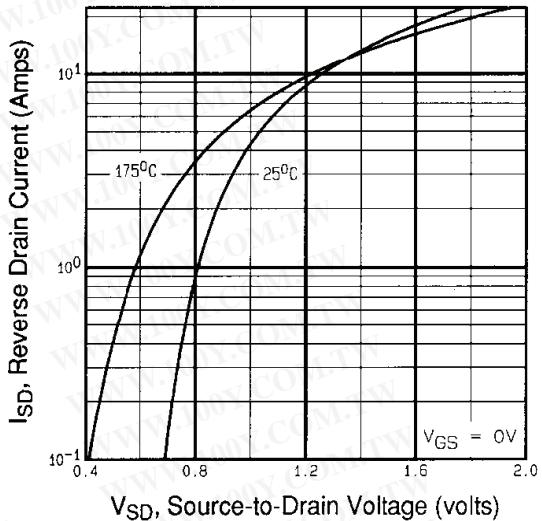


Fig. 7 - Typical Source-Drain Diode Forward Voltage

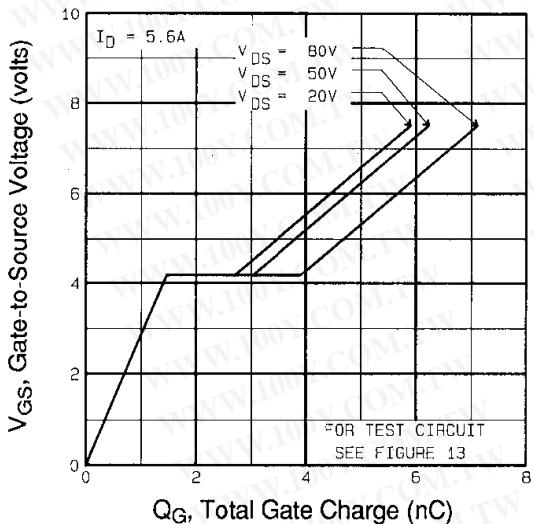


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

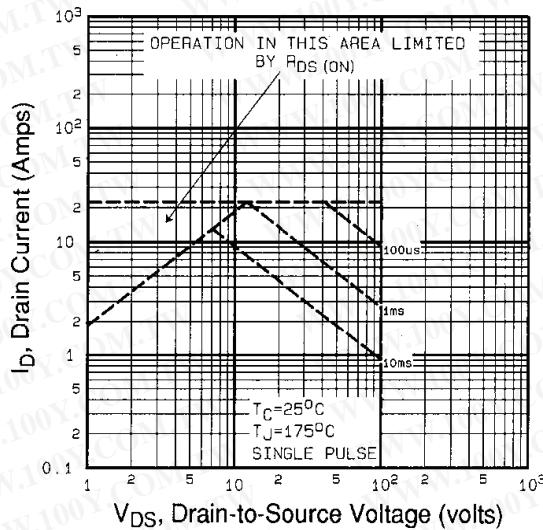


Fig. 8 - Maximum Safe Operating Area

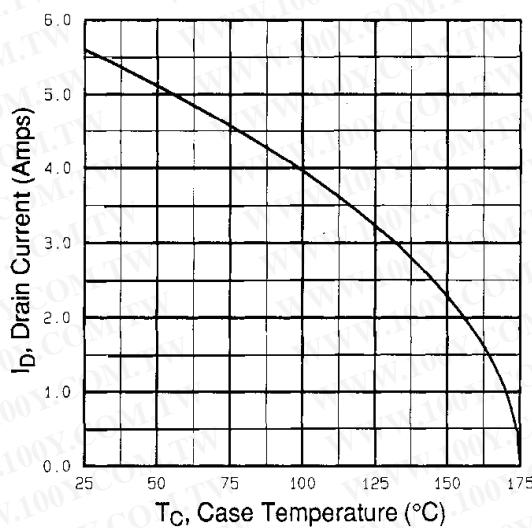


Fig. 9 - Maximum Drain Current vs. Case Temperature

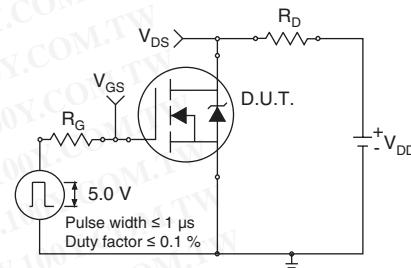


Fig. 10a - Switching Time Test Circuit

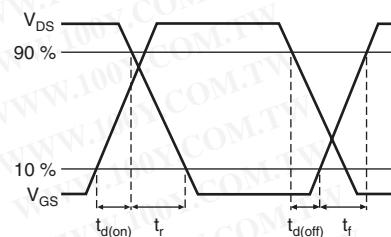


Fig. 10b - Switching Time Waveforms

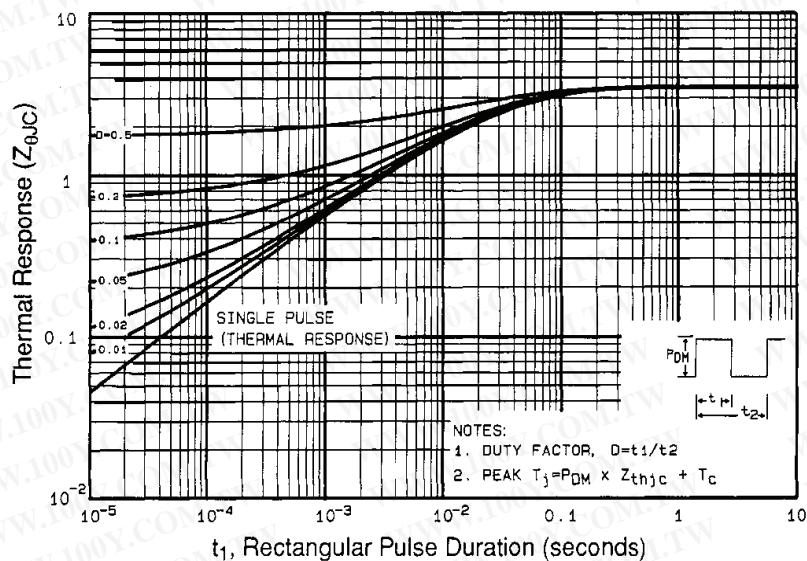


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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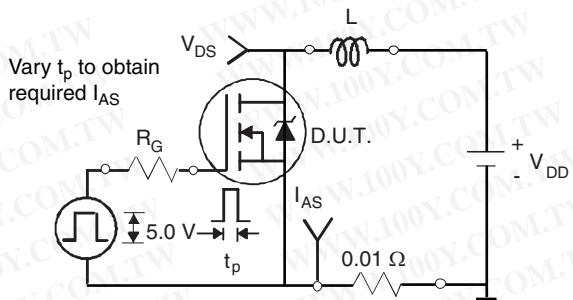


Fig. 12a - Unclamped Inductive Test Circuit

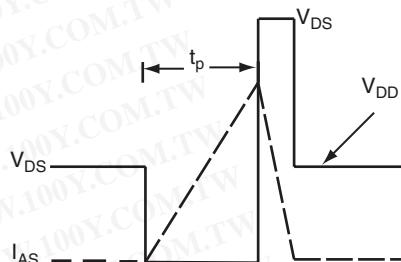


Fig. 12b - Unclamped Inductive Waveforms

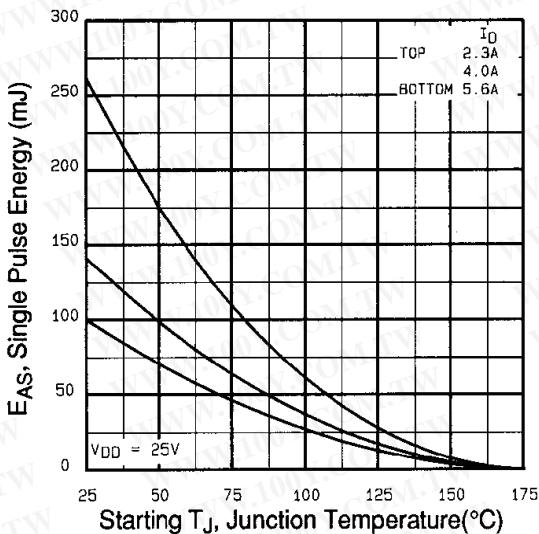


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

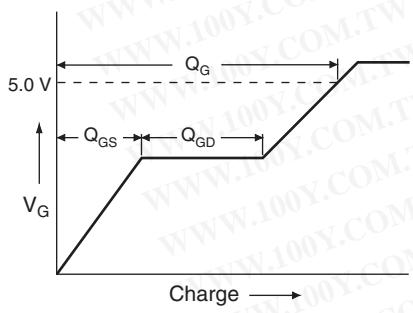


Fig. 13a - Basic Gate Charge Waveform

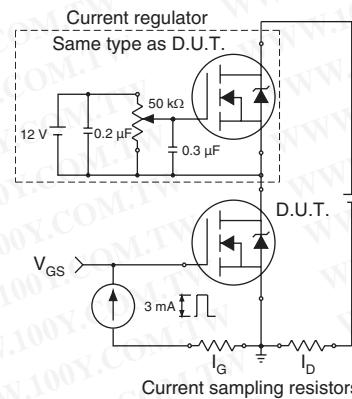


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

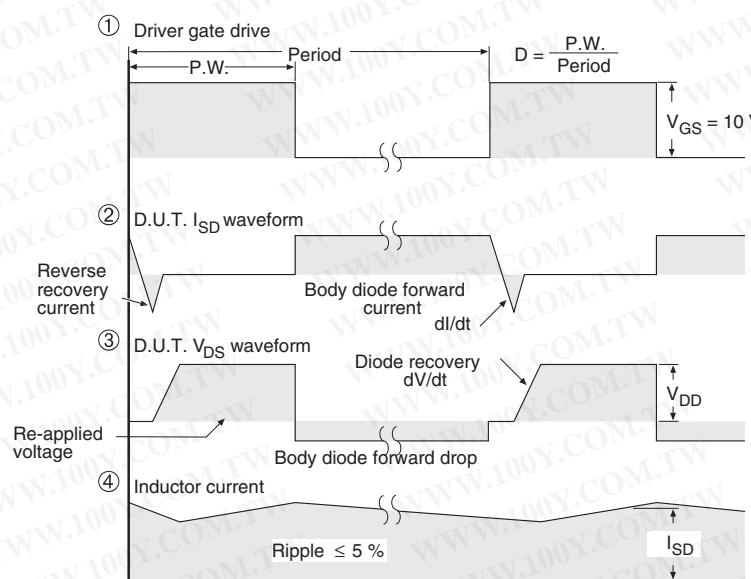
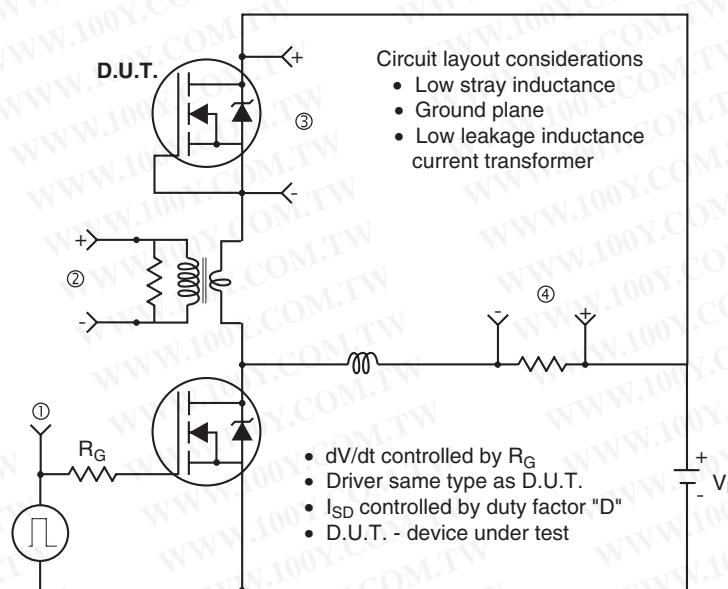


Fig. 14 - For N-Channel

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