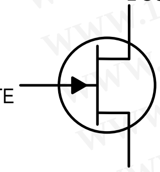
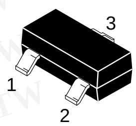
JFET Transistor
N–Channel

MMBF5484LT1

Motorola Preferred Device





CASE 318–08, STYLE 10
SOT–23 (TO–236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DG}	25	Vdc
Reverse Gate–Source Voltage	$V_{GS(r)}$	25	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Continuous Device Dissipation at or Below T_C = 25°C Linear Derating Factor	P_D	200 2.8	mW mW/°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board(1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

MMBF5484LT1 = 6B

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = –1.0 µAdc, V_{DS} = 0)	$V_{(BR)GSS}$	–25	—	Vdc
Gate Reverse Current (V_{GS} = –20 Vdc, V_{DS} = 0) (V_{GS} = –20 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	— —	–1.0 –0.2	nAdc µAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	$V_{GS(off)}$	–0.3	–3.0	Vdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	1.0	5.0	mAdc
SMALL–SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|Y_{fs}\|$	3000	6000	µmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	—	50	µmhos

1. FR–5 = 1.0 × 0.75 × 0.062 in.

Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
SMALL–SIGNAL CHARACTERISTICS (Continued)				
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 10 MHz)	C_{rss}	—	1.0	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	2.0	pF
FUNCTIONAL CHARACTERISTICS				
Noise Figure	NF			dB
(V_{DS} = 15 Vdc, I_D = 1.0 mAdc, YG′ = 1.0 mmhos) (R_G = 1.0 kΩ, f = 100 MHz)		—	3.0	
(V_{DS} = 15 Vdc, V_{GS} = 0, YG′ = 1.0 µmhos) (R_G = 1.0 MΩ, f = 1.0 kHz)		—	2.5	
Common Source Power Gain (V_{DS} = 15 Vdc, I_D = 1.0 mAdc, f = 100 MHz)	G_{ps}	16	25	dB

POWER GAIN

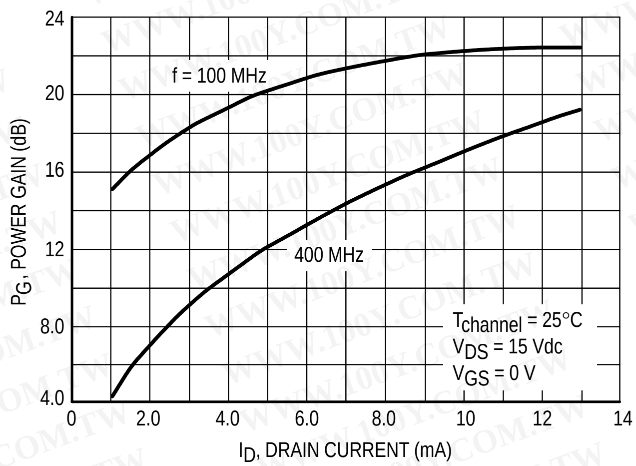
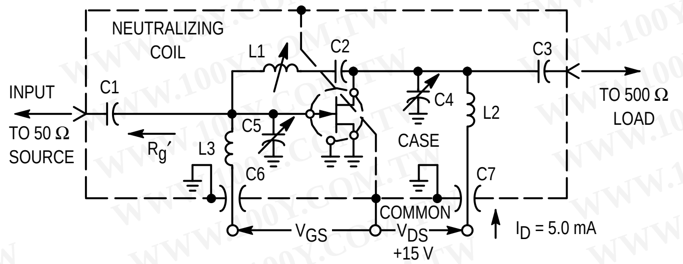


Figure 1. Effects of Drain Current



Reference Designation	VALUE	
	100 MHz	400 MHz
C1	7.0 pF	1.8 pF
C2	1000 pF	17 pF
C3	3.0 pF	1.0 pF
C4	1–12 pF	0.8–8.0 pF
C5	1–12 pF	0.8–8.0 pF
C6	0.0015 μF	0.001 μF
C7	0.0015 μF	0.001 μF
L1	3.0 μH*	0.2 μH**
L2	0.15 μH*	0.03 μH**
L3	0.14 μH*	0.022 μH**

Adjust V_{GS} for
I_D = 50 mA
V_{GS} < 0 Volts

NOTE: The noise source is a hot–cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

*L1 17 turns, (approx. — depends upon circuit layout) AWG #28 enameled copper wire, close wound on 9/32″ ceramic coil form. Tuning provided by a powdered iron slug.
L2 4–1/2 turns, AWG #18 enameled copper wire, 5/16″ long, 3/8″ I.D. (AIR CORE).
L3 3–1/2 turns, AWG #18 enameled copper wire, 1/4″ long, 3/8″ I.D. (AIR CORE).

**L1 6 turns, (approx. — depends upon circuit layout) AWG #24 enameled copper wire, close wound on 7/32″ ceramic coil form. Tuning provided by an aluminum slug.
L2 1 turn, AWG #16 enameled copper wire, 3/8″ I.D. (AIR CORE).
L3 1/2 turn, AWG #16 enameled copper wire, 1/4″ I.D. (AIR CORE).

Figure 2. 100 MHz and 400 MHz Neutralized Test Circuit

NOISE FIGURE

($T_{channel}$ = 25°C)

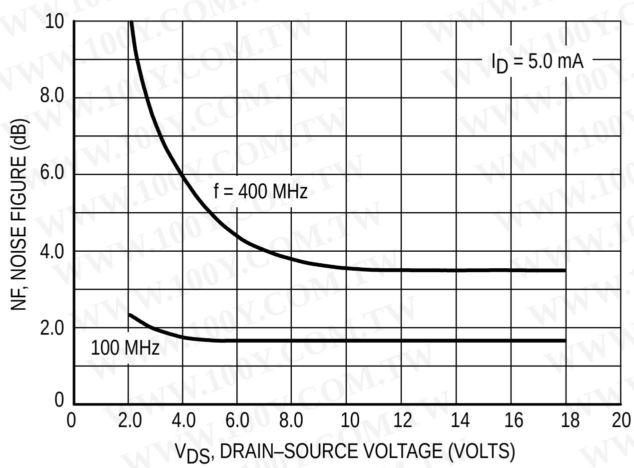


Figure 3. Effects of Drain–Source Voltage

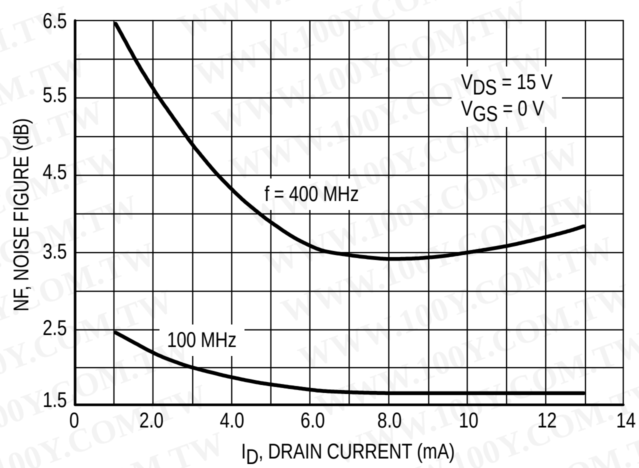


Figure 4. Effects of Drain Current

INTERMODULATION CHARACTERISTICS

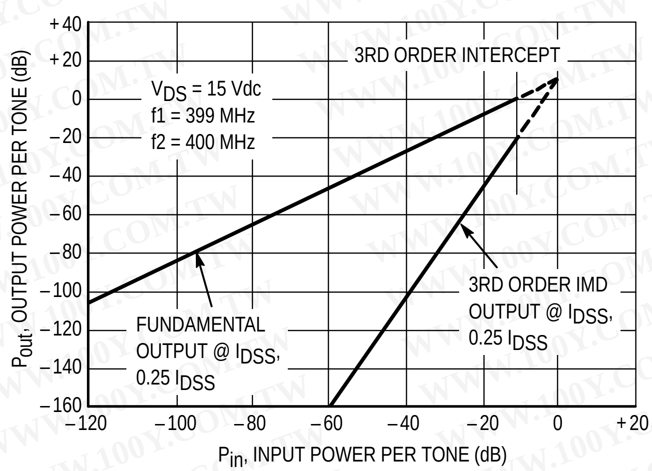


Figure 5. Third Order Intermodulation Distortion

COMMON SOURCE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C)

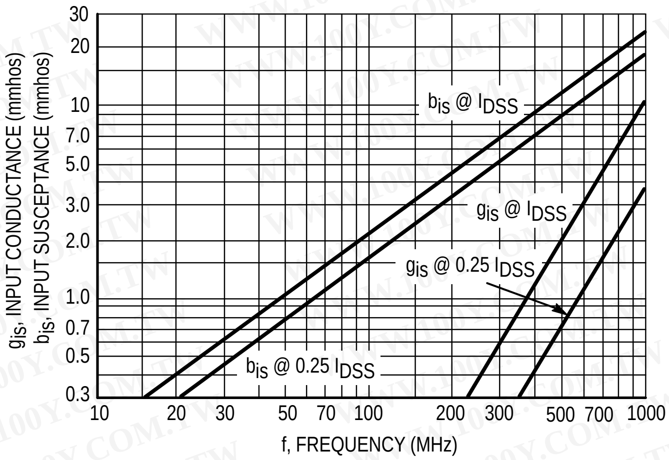


Figure 6. Input Admittance (y_{is})

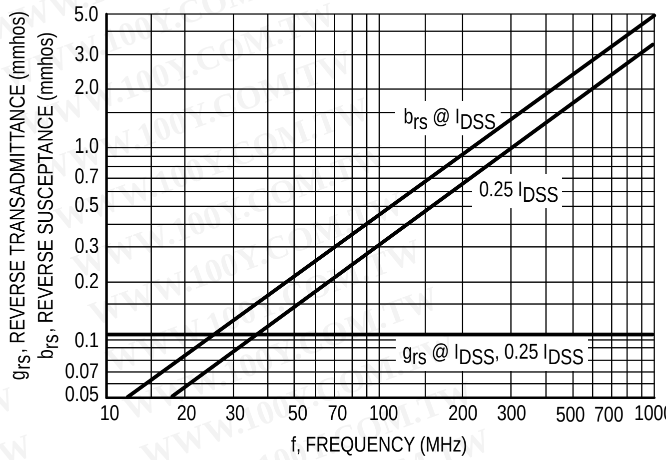


Figure 7. Reverse Transfer Admittance (y_{rs})

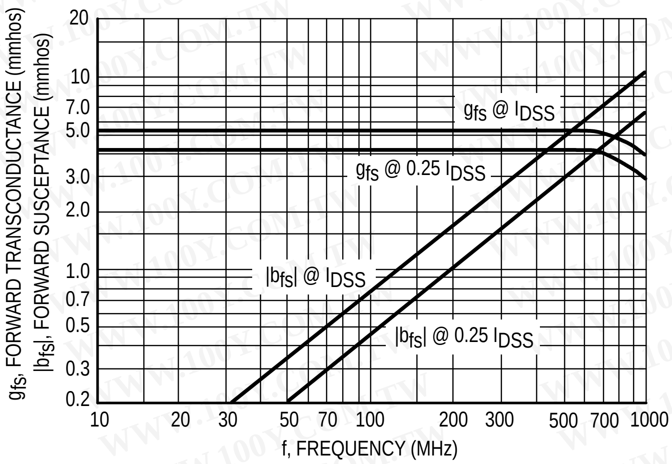


Figure 8. Forward Transadmittance (y_{fs})

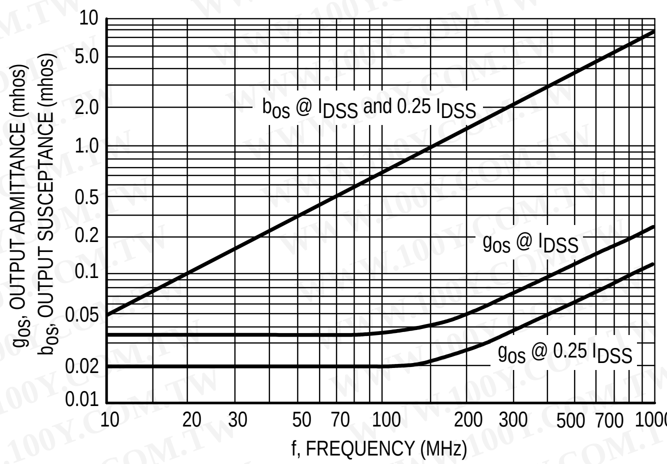


Figure 9. Output Admittance (y_{os})

COMMON SOURCE CHARACTERISTICS
S–PARAMETERS
(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

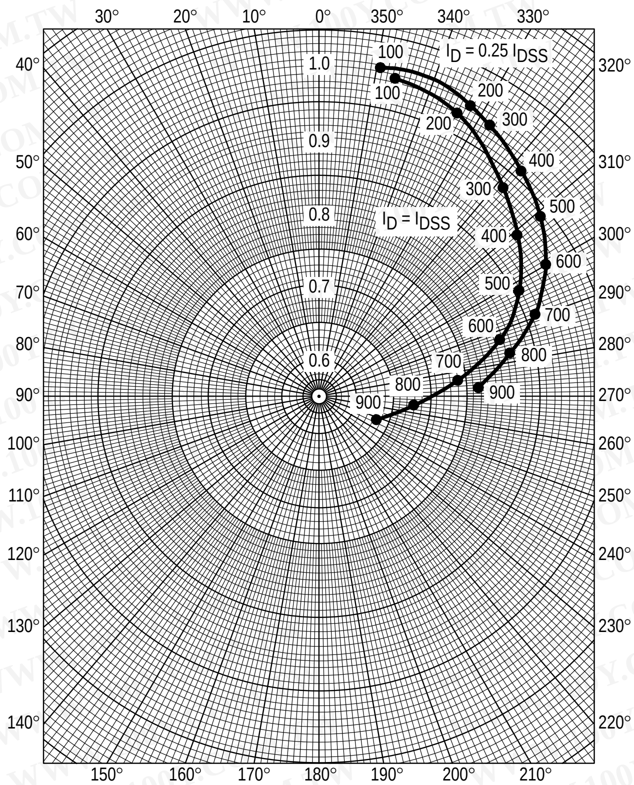


Figure 10. S_{11s}

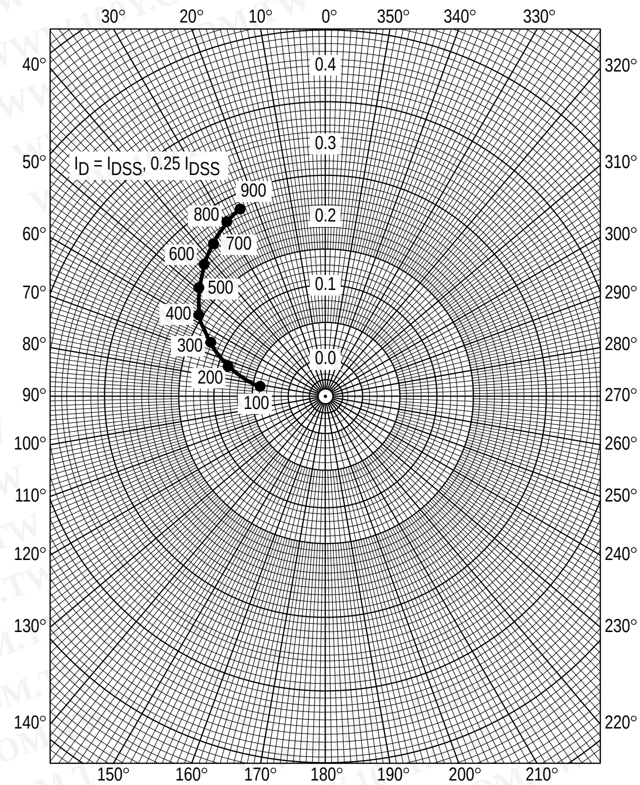


Figure 11. S_{12s}

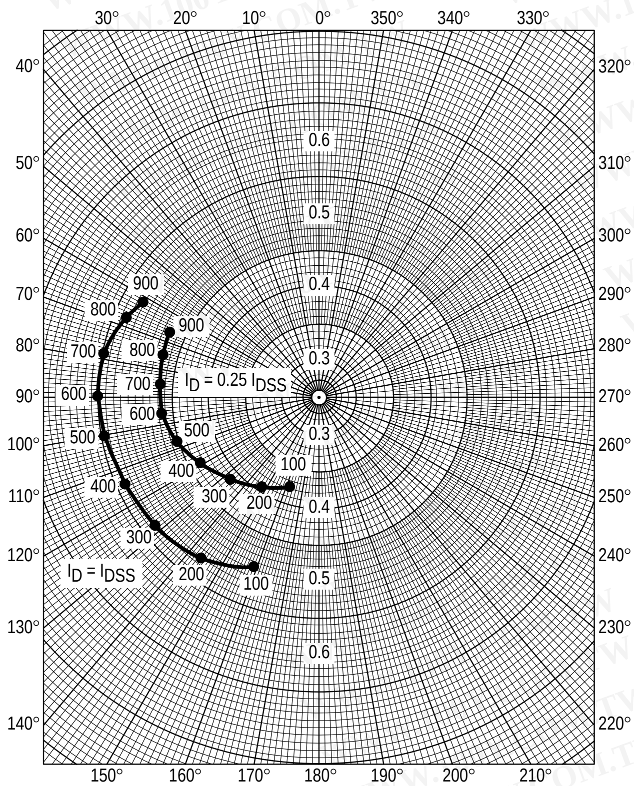


Figure 12. S_{21s}

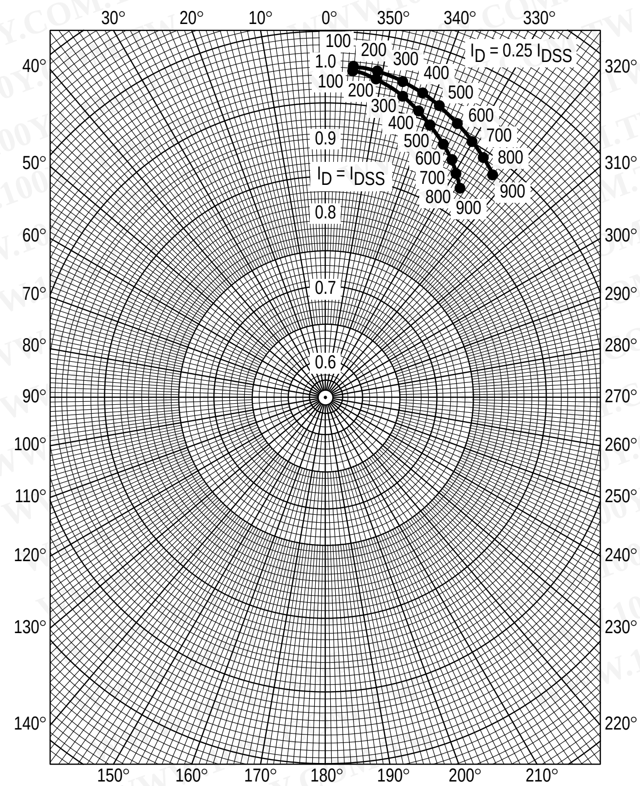


Figure 13. S_{22s}

COMMON GATE CHARACTERISTICS

ADMITTANCE PARAMETERS

(V_{DG} = 15 Vdc, $T_{channel}$ = 25°C)

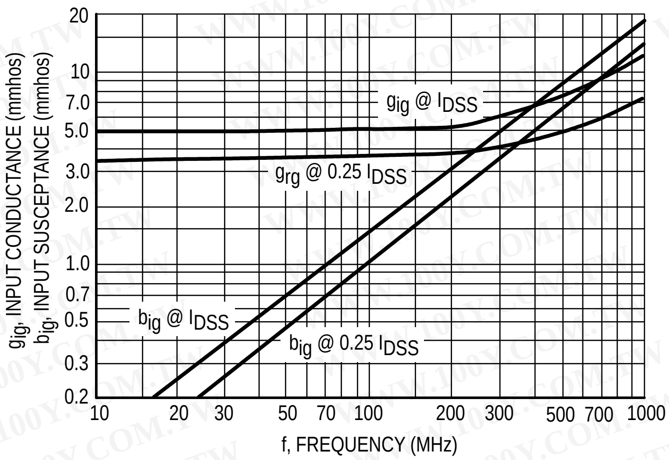


Figure 14. Input Admittance (y_{ig})

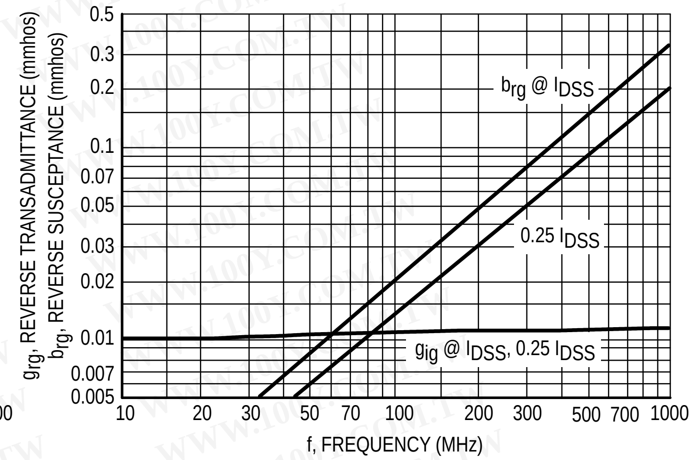


Figure 15. Reverse Transfer Admittance (y_{rg})

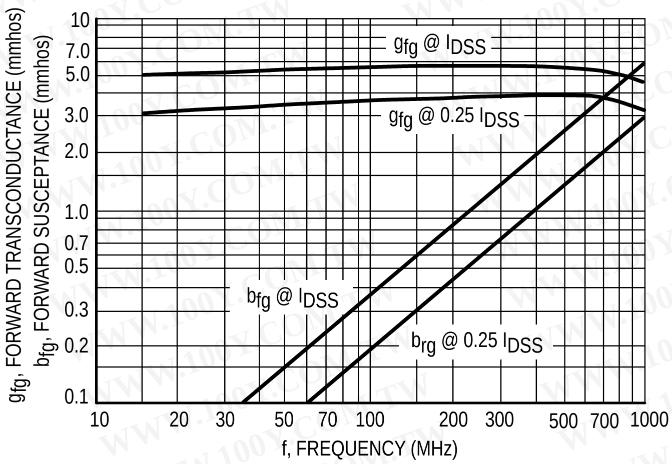


Figure 16. Forward Transfer Admittance (y_{fg})

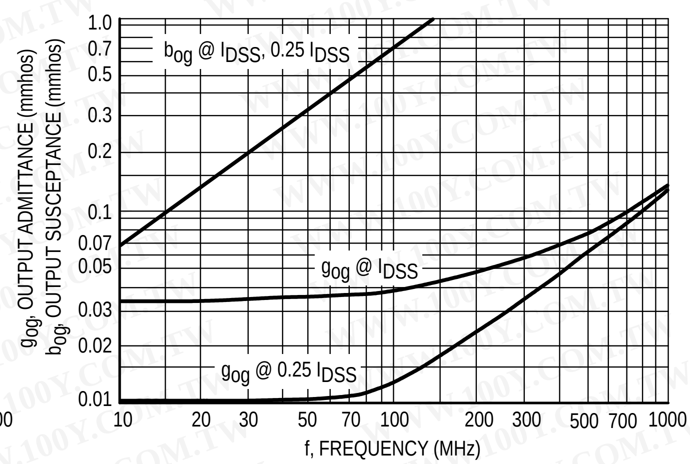


Figure 17. Output Admittance (y_{og})

COMMON GATE CHARACTERISTICS
S–PARAMETERS
(V_{DS} = 15 Vdc, $T_{channel}$ = 25°C, Data Points in MHz)

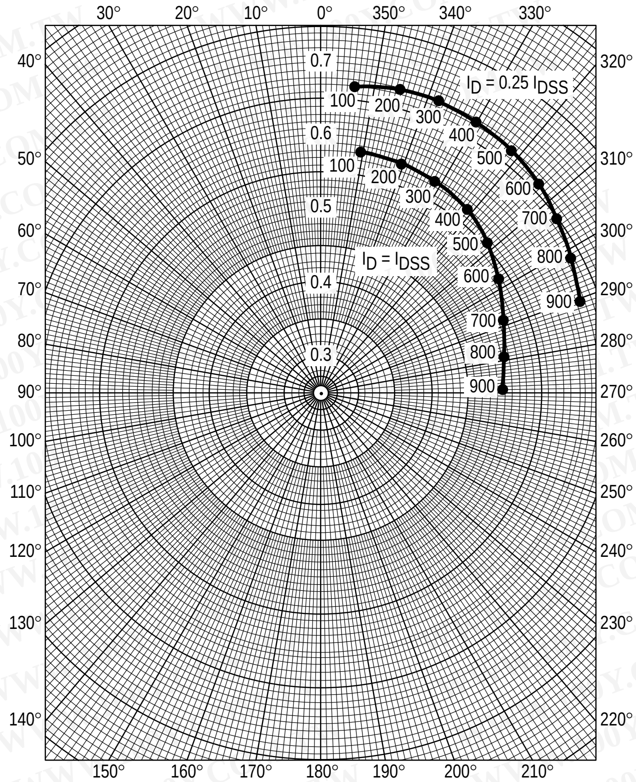


Figure 18. S_{11g}

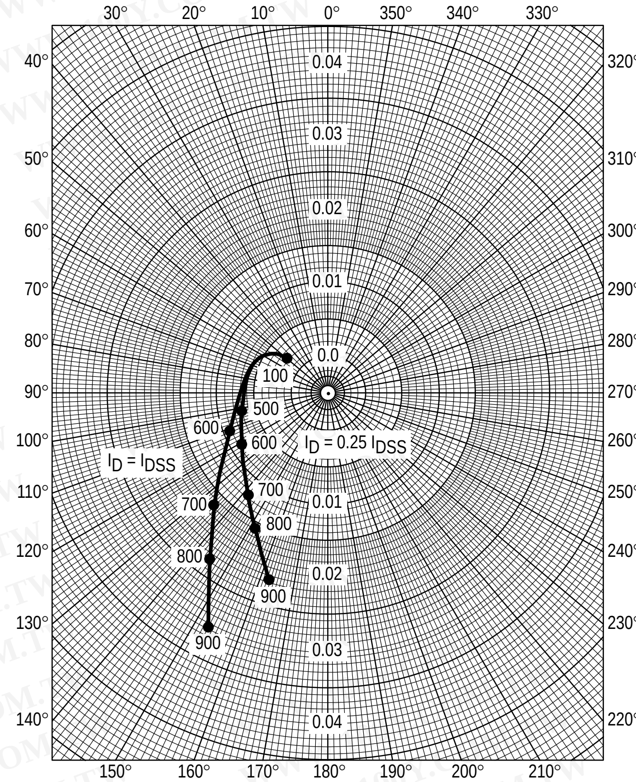


Figure 19. S_{12g}

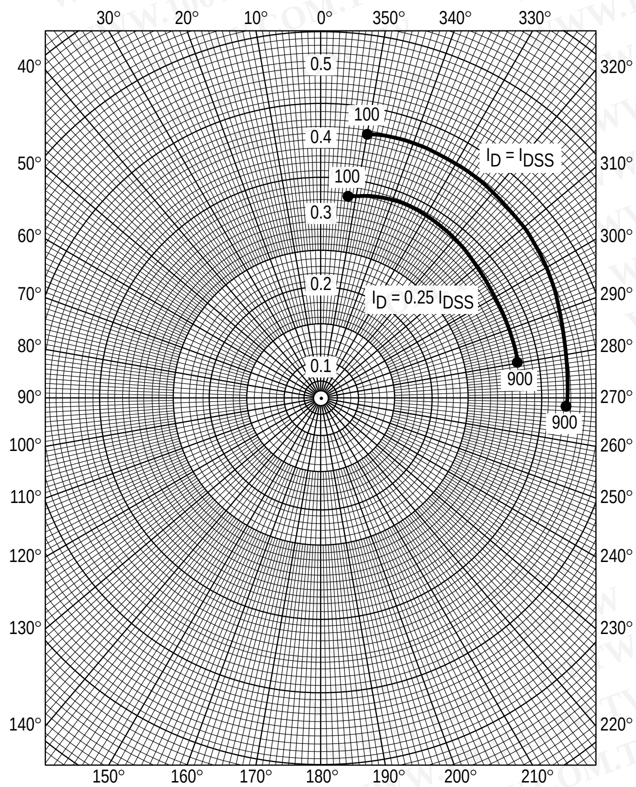


Figure 20. S_{21g}

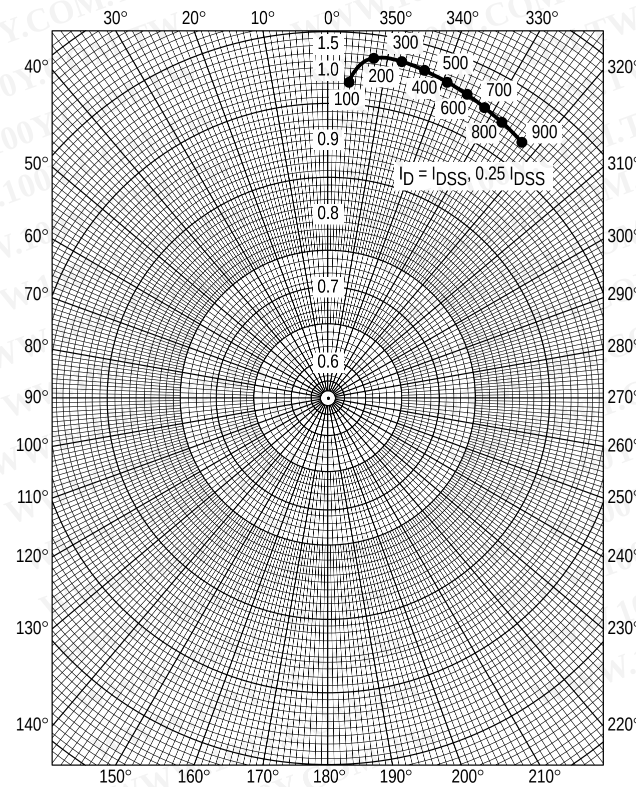
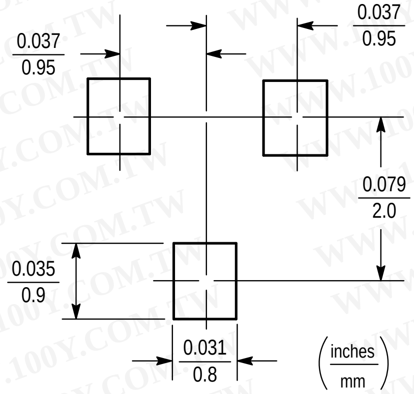


Figure 21. S_{22g}

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

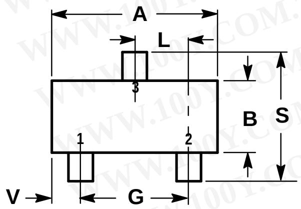
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

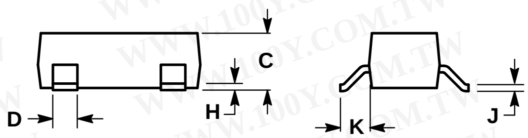
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

CASE 318–08
ISSUE AE
SOT–23 (TO–236AB)

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

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