

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3113 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristic, and designed for high voltage applications such as switching power supply, AC adapter.

FEATURES

- Low on-state resistance
 $R_{DS(on)} = 4.4 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 1.0 \text{ A)}$
- Low gate charge
 $Q_G = 9 \text{ nC TYP. (} V_{DD} = 450 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 2.0 \text{ A)}$
- Gate voltage rating $\pm 30 \text{ V}$
- Avalanche capability ratings

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	600	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 2.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 8.0	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	2.0	A
Single Avalanche Energy ^{Note3}	E_{AS}	2.7	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on glass epoxy board of 40 mm x 40 mm x 1.6 mm

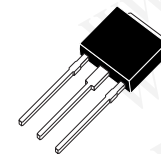
3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 150 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3113	TO-251 (MP-3)
2SK3113-Z	TO-252 (MP-3Z)

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

(TO-251)



(TO-252)



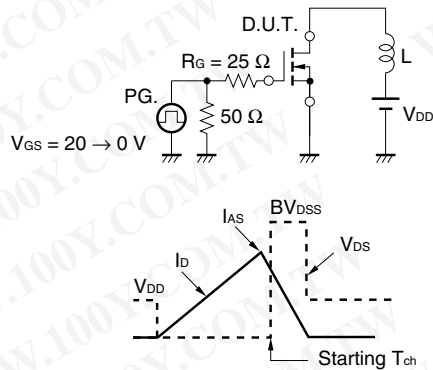
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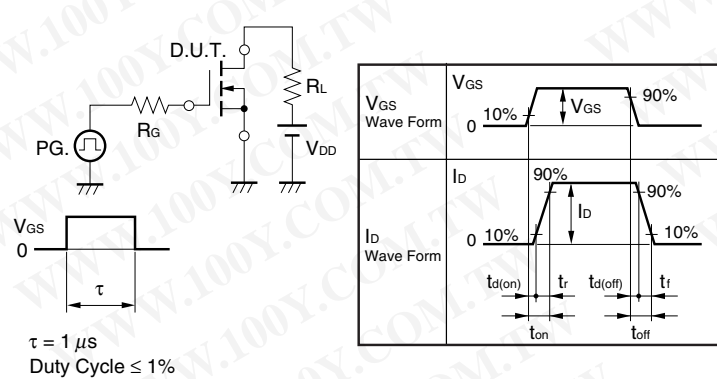
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$			100	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.5		3.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ A}$	0.5			S
Drain to Source On-state Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$		3.3	4.4	Ω
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$		290		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		60		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		5		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 150\text{ V}, I_D = 1.0\text{ A}$		7		ns
Rise Time	t_r	$V_{GS} = 10\text{ V}$		2		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega, R_L = 10\ \Omega$		22		ns
Fall Time	t_f			9		ns
Total Gate Charge	Q_G	$V_{DD} = 450\text{ V}$		9		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}$		2.4		nC
Gate to Drain Charge	Q_{GD}	$I_D = 2.0\text{ A}$		2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 2.0\text{ A}, V_{GS} = 0\text{ V}$		0.9		V
Reverse Recovery Time	t_{rr}	$I_F = 2.0\text{ A}, V_{GS} = 0\text{ V}$		0.9		μs
Reverse Recovery Charge	Q_{rr}	$di/dt = 50\text{ A}/\mu\text{s}$		2.0		μC

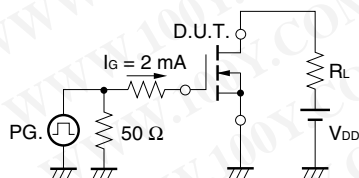
TEST CIRCUIT 1 AVALANCHE CAPABILITY



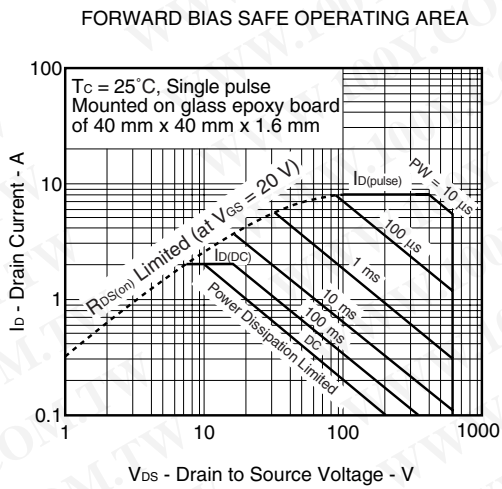
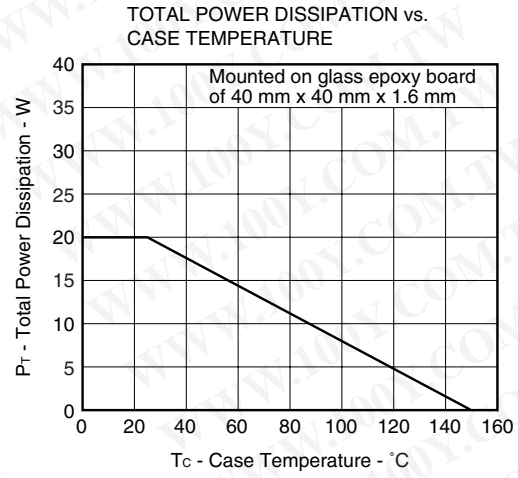
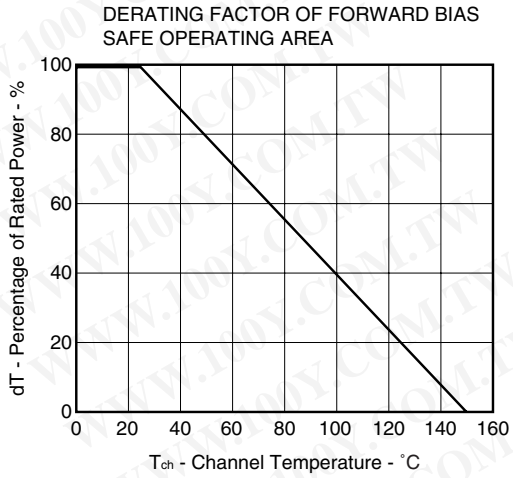
TEST CIRCUIT 2 SWITCHING TIME



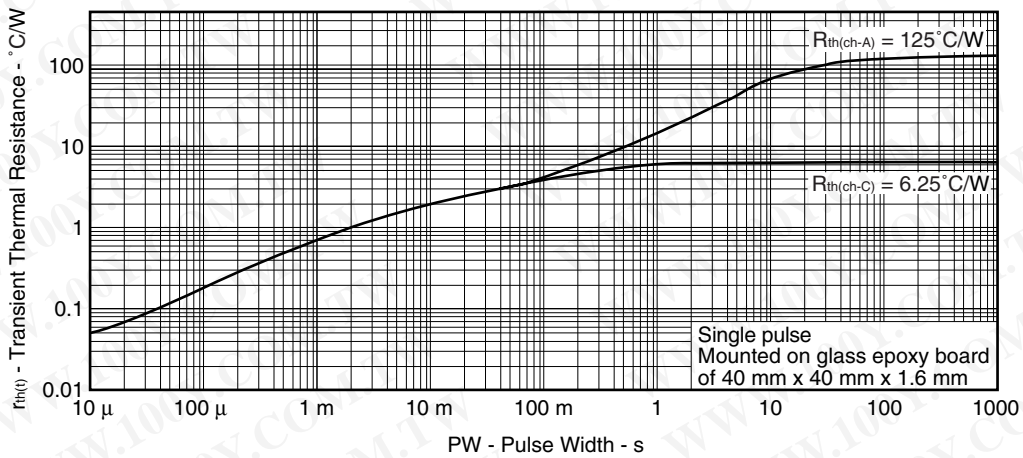
TEST CIRCUIT 3 GATE CHARGE



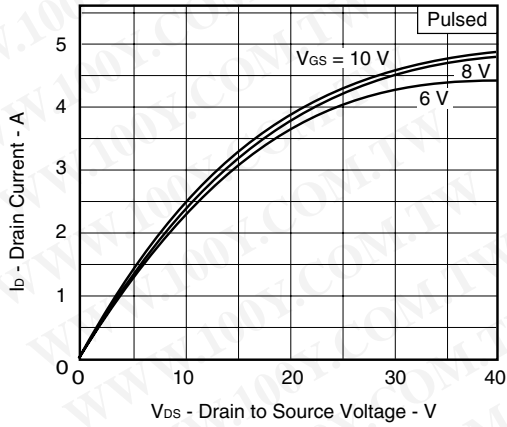
★ TYPICAL CHARACTERISTICS (T_A = 25°C)



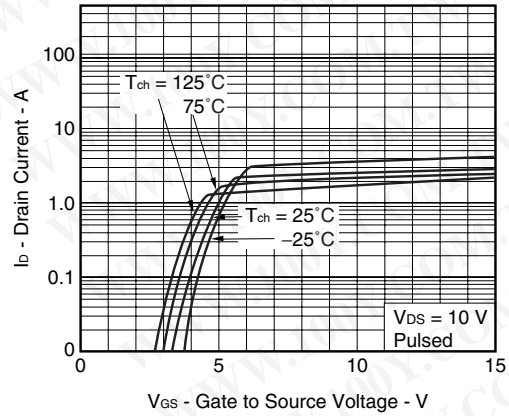
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



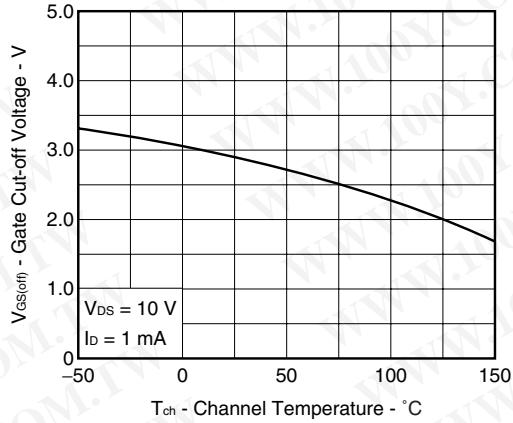
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



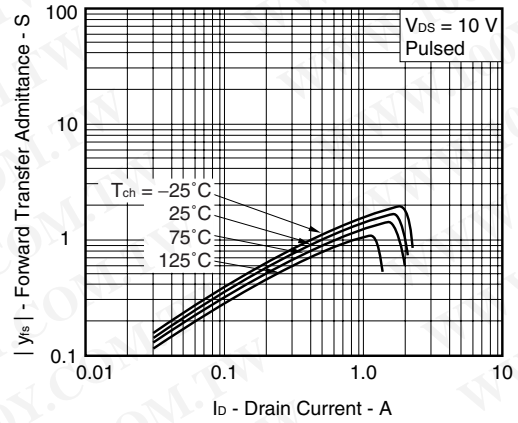
FORWARD TRANSFER CHARACTERISTICS



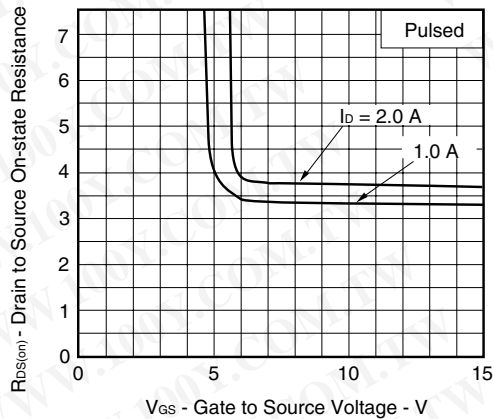
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



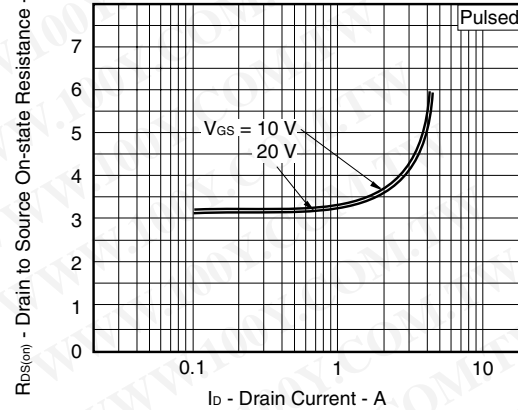
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

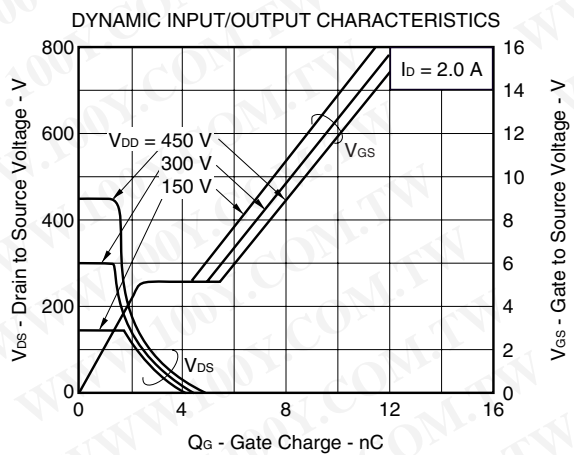
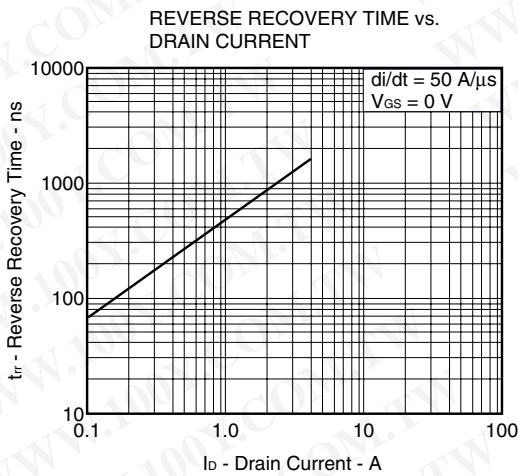
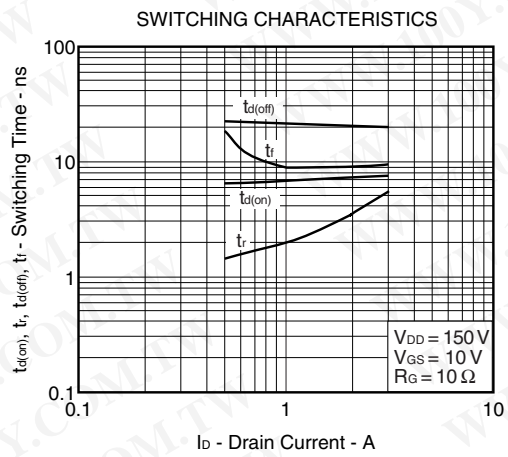
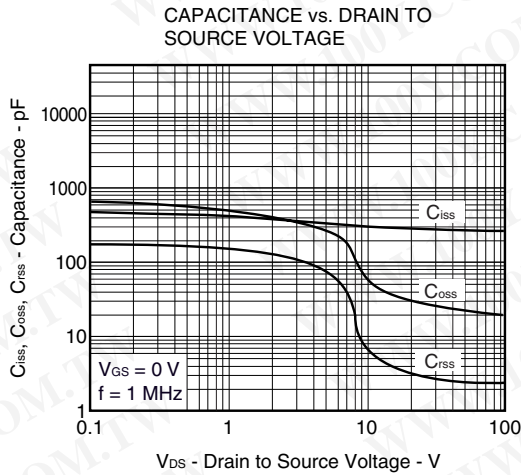
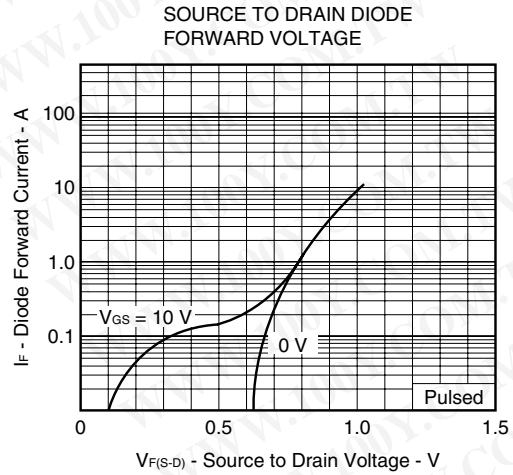
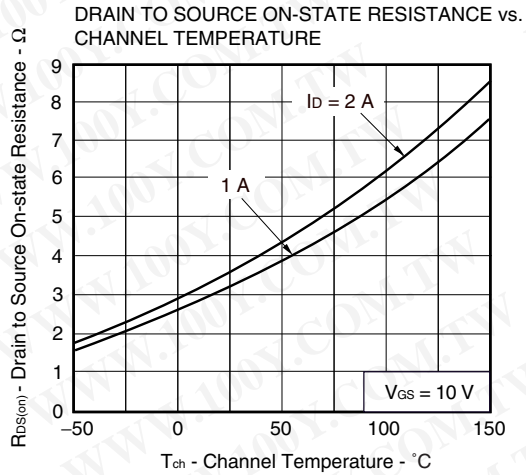


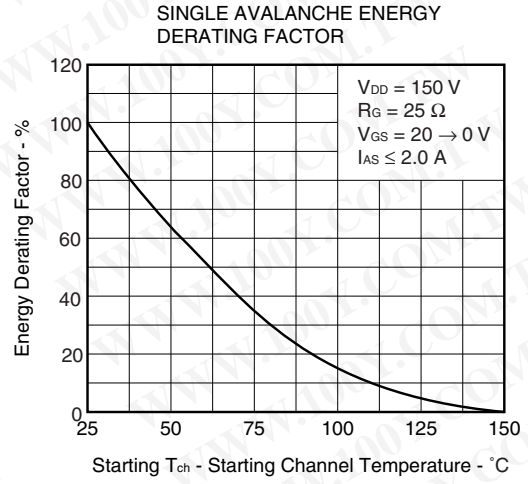
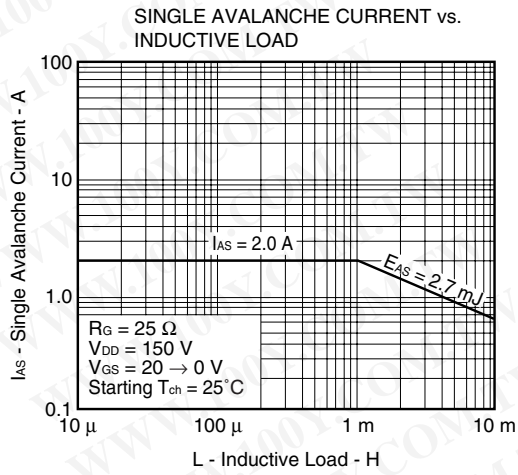
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

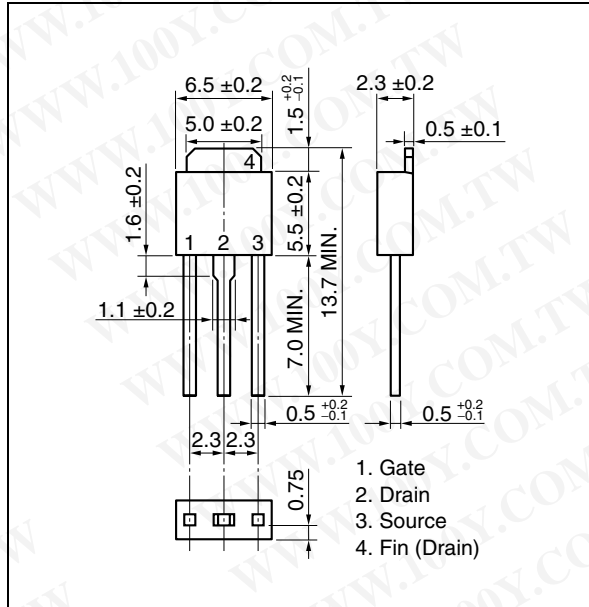




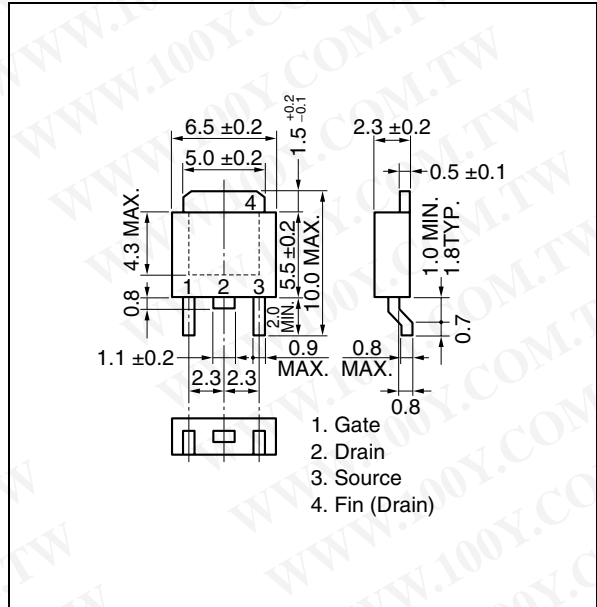


★ PACKAGE DRAWINGS (Unit: mm)

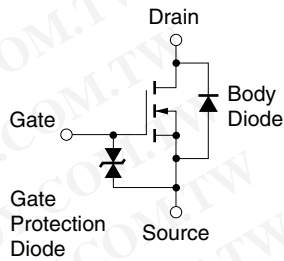
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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