

COMPOUND FIELD EFFECT POWER TRANSISTOR

μ PA1556A

N-CHANNEL POWER MOS FET ARRAY

SWITCHING TYPE

DESCRIPTION

The μ PA1556A is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
 $I_{D(pulse)} = \pm 20$ A
 $R_{DS(on)} = 0.20 \Omega$ TYP. ($V_{GS} = 10$ V)
 $R_{DS(on)} = 0.25 \Omega$ TYP. ($V_{GS} = 4$ V)
- Low Capacitance $C_{iss} = 700$ pF TYP.
- Gate Protector built in.
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

| Part Number | Package | Quality Grade |
|----------------|------------|---------------|
| μ PA1556AH | 10 Pin SIP | Standard |

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

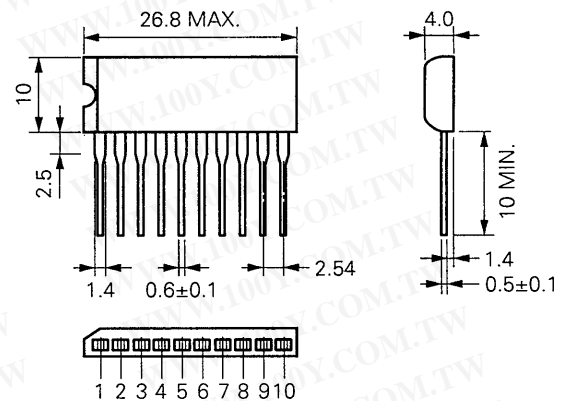
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

| | | | |
|--------------------------------------|------------------|-------------|------------------|
| Drain to Source Voltage | V_{DSS} | 100 | V |
| Gate to Source Voltage (AC) | V_{GSS} | ± 20 | V |
| Gate to Source Voltage (DC) | V_{GSS} | +20, -10 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 5.0 | A/unit |
| Drain Current (pulse) | $I_{D(pulse)}^*$ | ± 20 | A/unit |
| Total Power Dissipation (4 circuits) | | | |
| < $T_c = 25^\circ\text{C}$ > | P_{T1} | 28 | W |
| Total Power Dissipation (4 circuits) | | | |
| < $T_a = 25^\circ\text{C}$ > | P_{T2} | 3.5 | W |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Junction Temperature | T_j | 150 | $^\circ\text{C}$ |

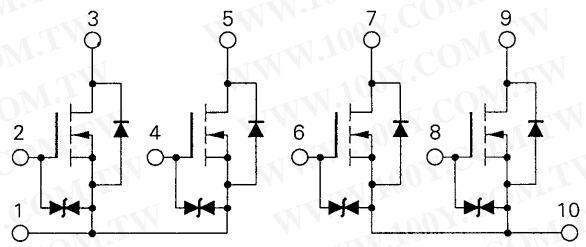
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSION

(in millimeters)

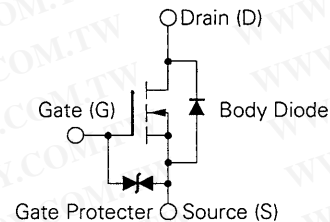


CONNECTION DIAGRAM



PIN No.

| | |
|------------|------------|
| 2, 4, 6, 8 | Gate (G) |
| 3, 5, 7, 9 | Drain (D) |
| 1, 10 | Source (S) |



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ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|------|----------|---------------|---|
| Drain Leakage Current | I_{DSS} | | | 10 | μA | $V_{\text{DS}} = 100\text{ V}$, $V_{\text{GS}} = 0$ |
| Gate to Source Leakage Current | I_{GSS} | | | ± 10 | μA | $V_{\text{GS}} = \pm 20\text{ V}$, $V_{\text{DS}} = 0$ |
| Gate to Source Cutoff Voltage | $V_{\text{GS(off)}}$ | 1.0 | | 2.5 | V | $V_{\text{DS}} = 10\text{ V}$, $I_{\text{D}} = 1\text{ mA}$ |
| Forward Transfer Admittance | $ y_{\text{fs}} $ | 4.0 | | | S | $V_{\text{DS}} = 10\text{ V}$, $I_{\text{D}} = 3\text{ A}$ |
| Drain to Source On-state Resistance | $R_{\text{DS(on)1}}$ | | 0.20 | 0.25 | Ω | $V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 3\text{ A}$ |
| Drain to Source On-state Resistance | $R_{\text{DS(on)2}}$ | | 0.25 | 0.33 | Ω | $V_{\text{GS}} = 4\text{ V}$, $I_{\text{D}} = 3\text{ A}$ |
| Input Capacitance | C_{iss} | | 700 | | pF | $V_{\text{DS}} = 10\text{ V}$ $V_{\text{GS}} = 0$ $f = 1.0\text{ MHz}$ |
| Output Capacitance | C_{oss} | | 200 | | pF | |
| Reverse Transfer Capacitance | C_{rss} | | 30 | | pF | |
| Turn-On Delay Time | $t_{\text{d(on)}}$ | | 35 | | ns | $I_{\text{D}} = 3\text{ A}$ $V_{\text{GS}} = 10\text{ V}$ $V_{\text{CC}} = 50\text{ V}$ $R_{\text{L}} = 17\ \Omega$, $R_{\text{in}} = 10\ \Omega$ See Fig. 1 |
| Rise Time | t_{r} | | 60 | | ns | |
| Turn-Off Delay Time | $t_{\text{d(off)}}$ | | 800 | | ns | |
| Fall Time | t_{f} | | 200 | | ns | |
| Total Gate Charge | Q_{G} | | 17 | | nC | $V_{\text{GS}} = 10\text{ V}$ $I_{\text{D}} = 5\text{ A}$ $V_{\text{DD}} = 80\text{ V}$ See Fig. 2 |
| Gate to Source Charge | Q_{GS} | | 2.5 | | nC | |
| Gate to Drain Charge | Q_{GD} | | 4 | | nC | |
| Diode Forward Voltage | $V_{\text{F(S-D)}}$ | | 1.0 | | V | $I_{\text{F}} = 5\text{ A}$, $V_{\text{GS}} = 0$ |
| Reverse Recovery Time | t_{rr} | | 120 | | ns | $I_{\text{F}} = 5\text{ A}$, $V_{\text{GS}} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$ |
| Reverse Recovery Charge | Q_{rr} | | 230 | | nC | |

Fig. 1 Switching Time Test Circuit

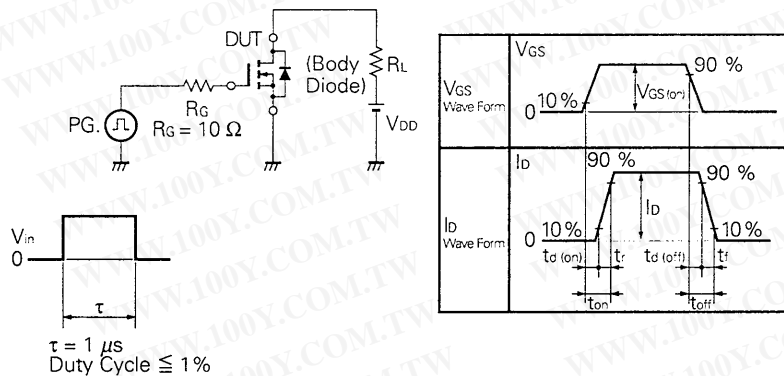
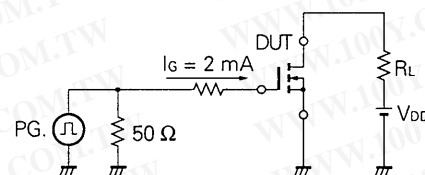


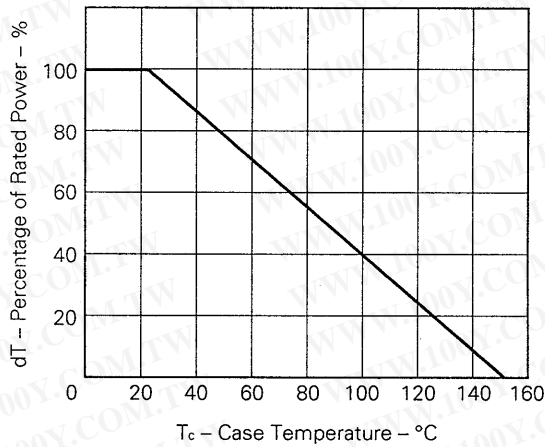
Fig. 2 Gate Charge Test Circuit



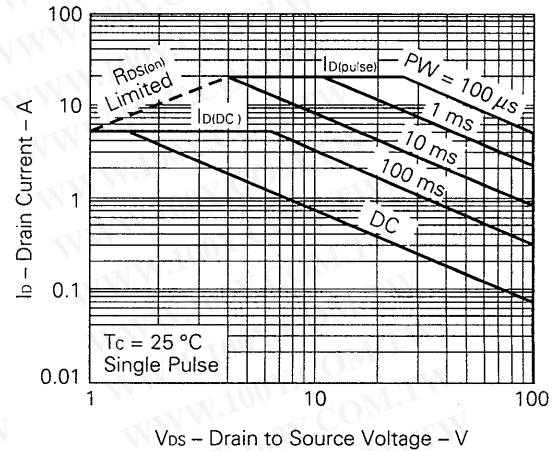
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TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

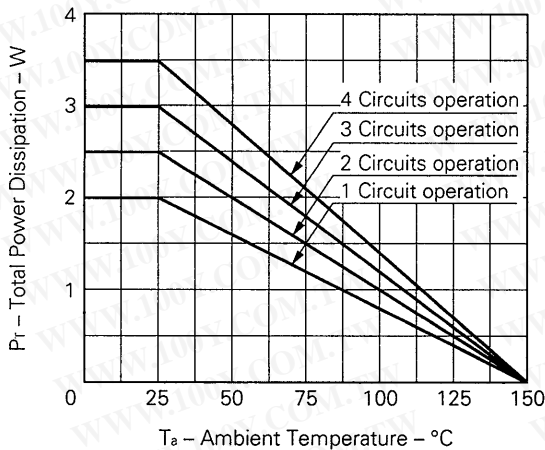
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



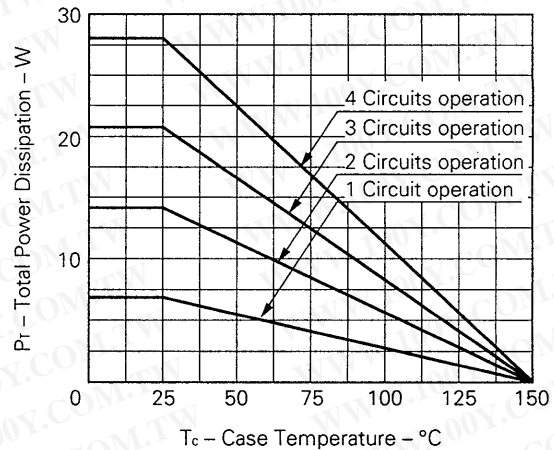
FORWARD BIAS SAFE OPERATING AREA



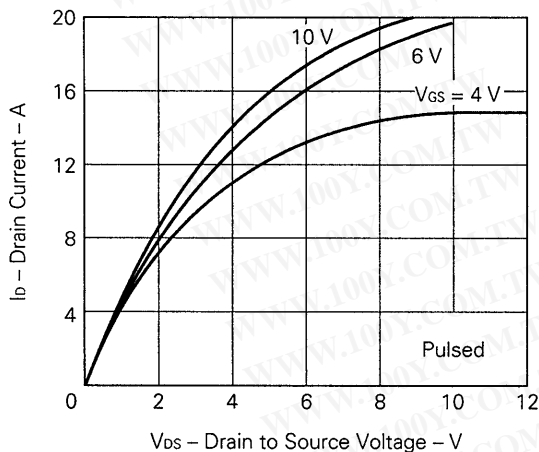
TOTAL POWER DISSIPATION vs.
AMBIENT TEMPERATURE



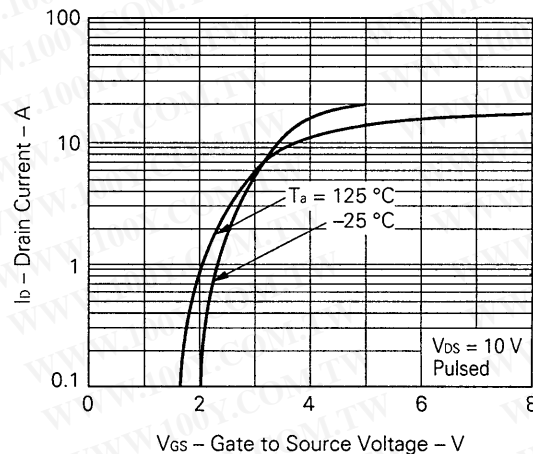
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

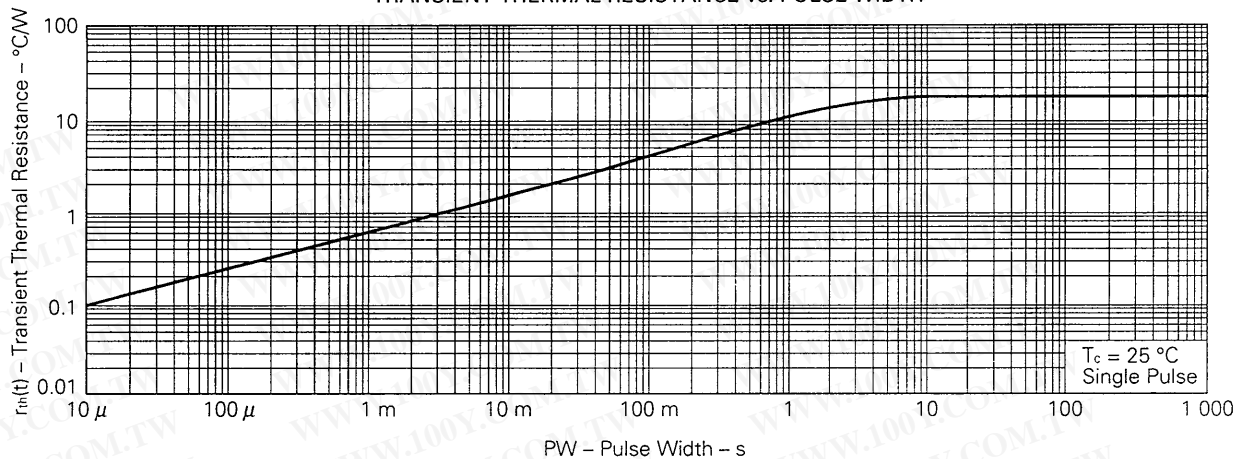


TRANSFER CHARACTERISTICS

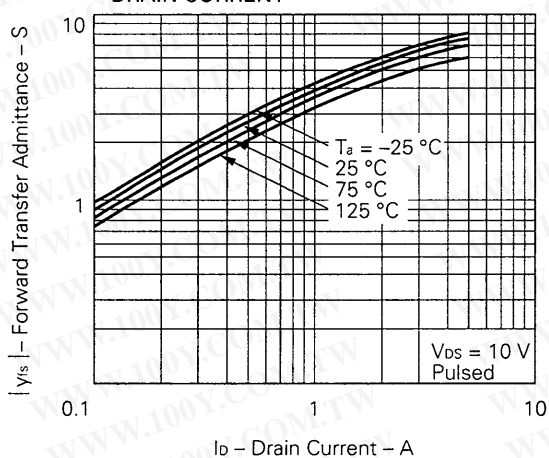


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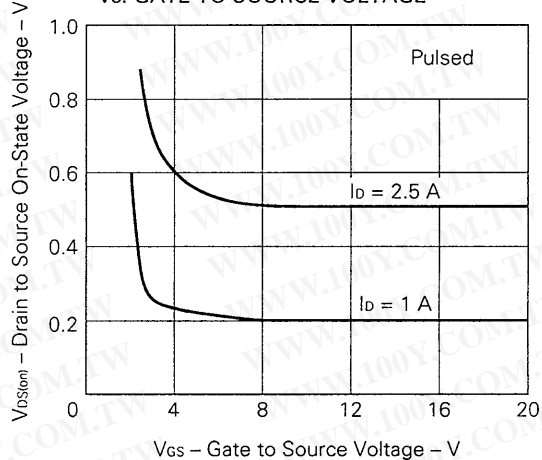
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



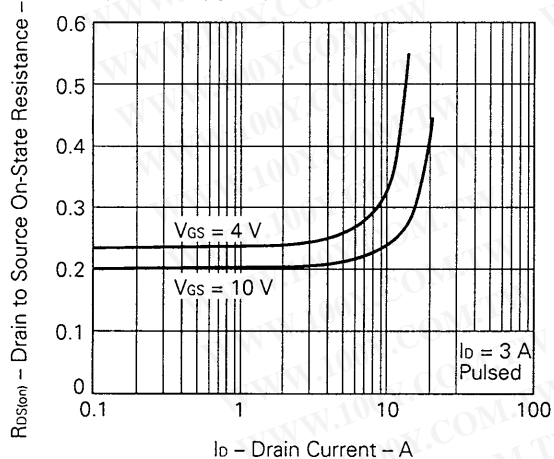
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



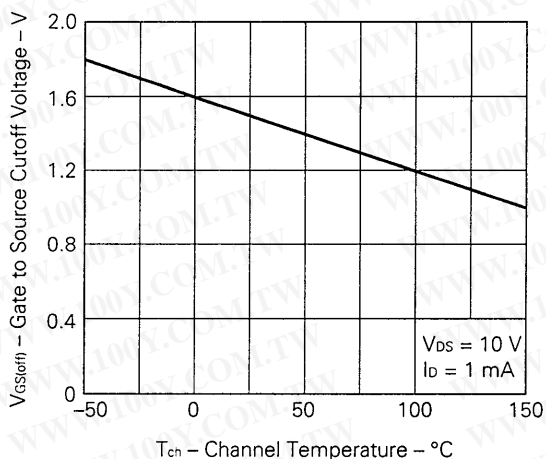
DRAIN TO SOURCE ON-STATE VOLTAGE vs. GATE TO SOURCE VOLTAGE



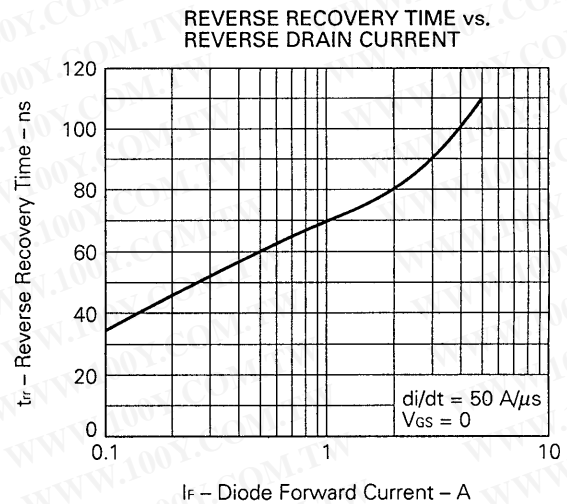
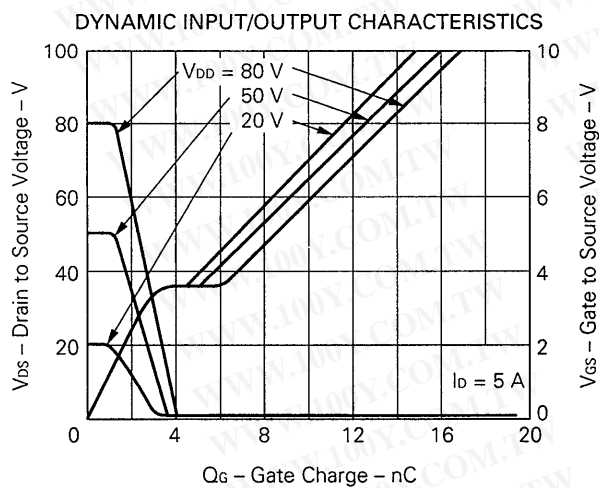
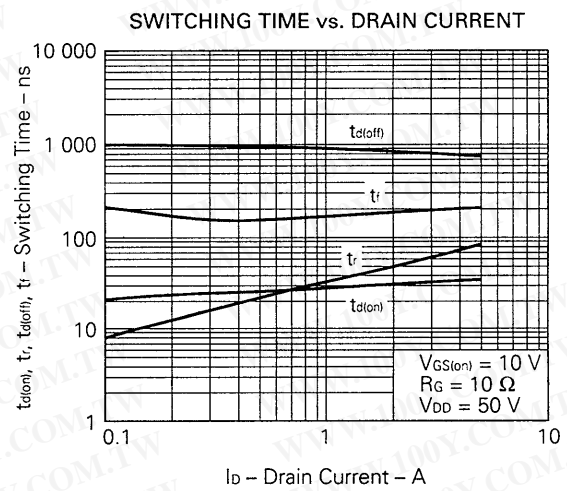
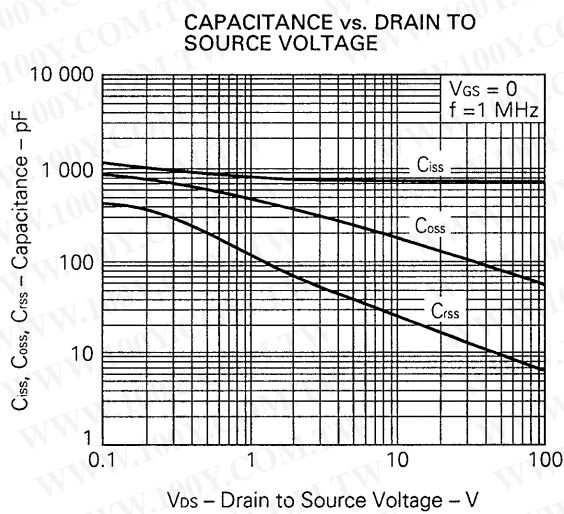
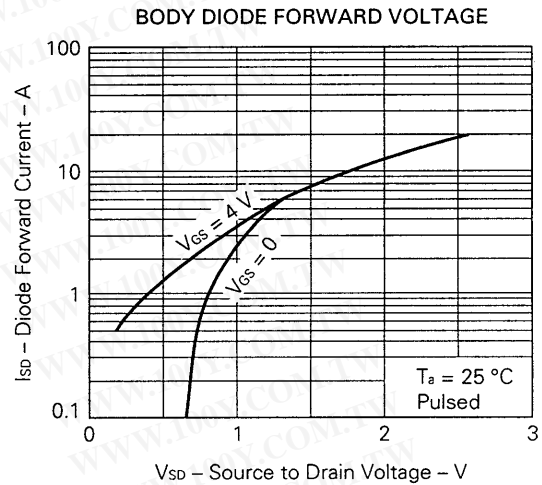
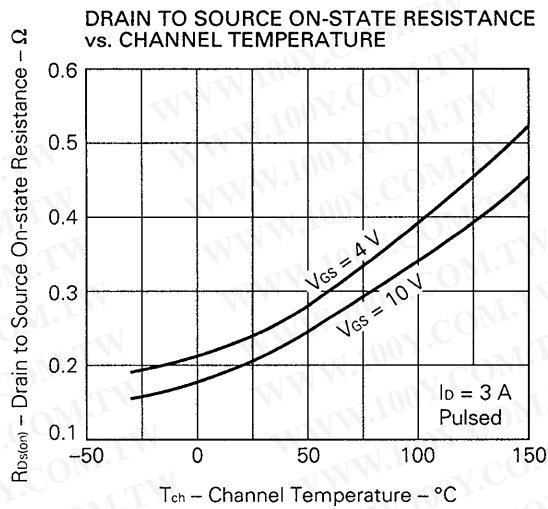
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



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Reference

| Document name | Document No. |
|--|--------------|
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |
| Safe operating area of Power MOS FET | TEA-1034 |
| Appication circuit using Power MOS FET | TEA-1035 |

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