# MMBTA05LT1, MMBTA06LT1

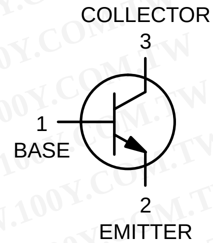
**MMBTA06LT1 is a Preferred Device**

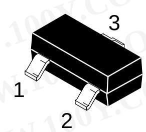
# Driver Transistors

## NPN Silicon

ON Semiconductor®

http://onsemi.com




**SOT–23**
**CASE 318**
**STYLE 6**

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage MMBTA05LT1 | $V_{CEO}$ | 60 | Vdc |
| MMBTA06LT1 | | 80 | |
| Collector–Base Voltage MMBTA05LT1 | $V_{CBO}$ | 60 | Vdc |
| MMBTA06LT1 | | 80 | |
| Emitter–Base Voltage | $V_{EBO}$ | 4.0 | Vdc |
| Collector Current – Continuous | $I_C$ | 500 | mAdc |

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR–5 Board (Note 1) $T_A = 25°C$ | $P_D$ | 225 | mW |
| Derate above 25°C | | 1.8 | mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25°C$ | $P_D$ | 300 | mW |
| Derate above 25°C | | 2.4 | mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 417 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. FR–5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.



**MARKING DIAGRAMS**


MMBTA05LT1 MMBTA06LT1

1H, 1GM = Specific Device Code
X = Date Code

**ORDERING INFORMATION**

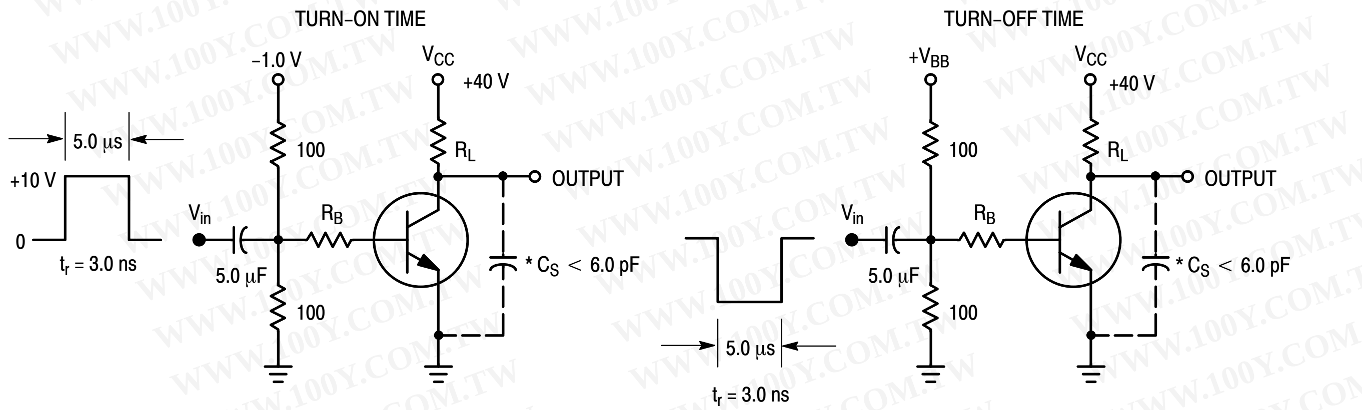
| Device | Package | Shipping |
|---|---|---|
| MMBTA05LT1 | SOT–23 | 3000/Tape & Reel |
| MMBTA06LT1 | SOT–23 | 3000/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector–Emitter Breakdown Voltage (Note 3) ($I_C$ = 1.0 mAdc, $I_B$ = 0) | MMBTA05<br>MMBTA06 | $V_{(BR)CEO}$ | 60<br>80 | –<br>– | Vdc |
| Emitter–Base Breakdown Voltage ($I_E$ = 100 μAdc, $I_C$ = 0) | | $V_{(BR)EBO}$ | 4.0 | – | Vdc |
| Collector Cutoff Current ($V_{CE}$ = 60 Vdc, $I_B$ = 0) | | $I_{CES}$ | – | 0.1 | μAdc |
| Collector Cutoff Current ($V_{CB}$ = 60 Vdc, $I_E$ = 0)<br>($V_{CB}$ = 80 Vdc, $I_E$ = 0) | MMBTA05<br>MMBTA06 | $I_{CBO}$ | –<br>– | 0.1<br>0.1 | μAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain ($I_C$ = 10 mAdc, $V_{CE}$ = 1.0 Vdc)<br>($I_C$ = 100 mAdc, $V_{CE}$ = 1.0 Vdc) | | $h_{FE}$ | 100<br>100 | –<br>– | – |
| Collector–Emitter Saturation Voltage ($I_C$ = 100 mAdc, $I_B$ = 10 mAdc) | | $V_{CE(sat)}$ | – | 0.25 | Vdc |
| Base–Emitter On Voltage ($I_C$ = 100 mAdc, $V_{CE}$ = 1.0 Vdc) | | $V_{BE(on)}$ | – | 1.2 | Vdc |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | |
| Current–Gain – Bandwidth Product (Note 4) ($I_C$ = 10 mA, $V_{CE}$ = 2.0 V, f = 100 MHz) | | $f_T$ | 100 | – | MHz |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. $f_T$ is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.




*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

**Figure 1. Switching Time Test Circuits**

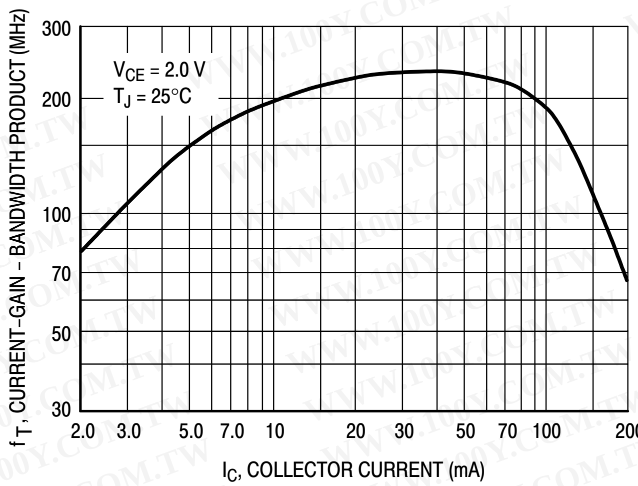



**Figure 2. Current–Gain — Bandwidth Product**

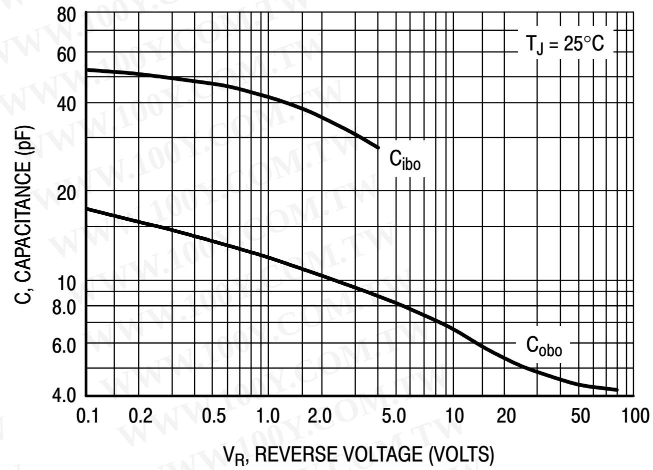



**Figure 3. Capacitance**

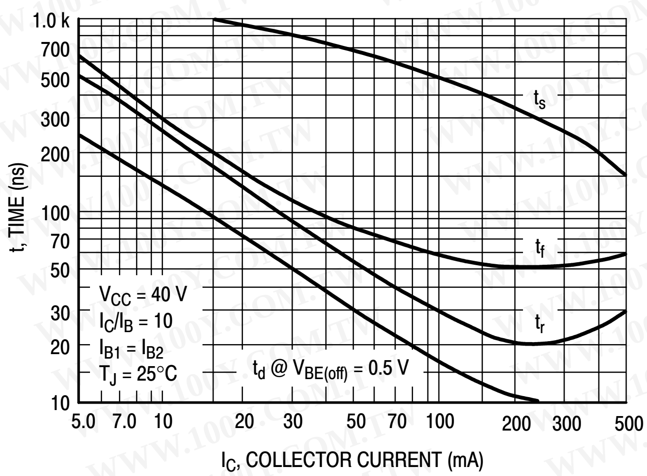



**Figure 4. Switching Time**

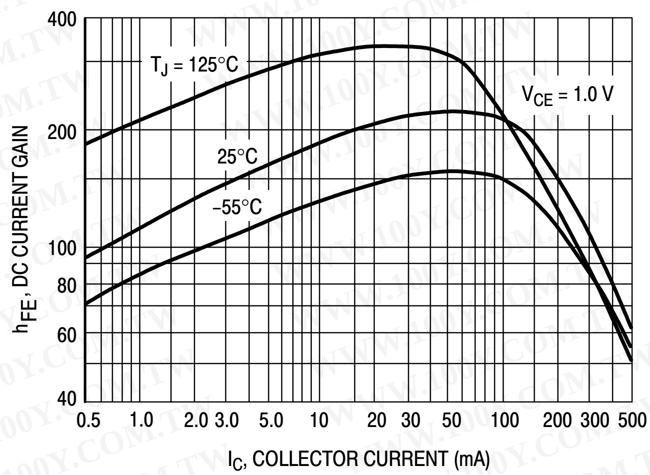



**Figure 5. DC Current Gain**

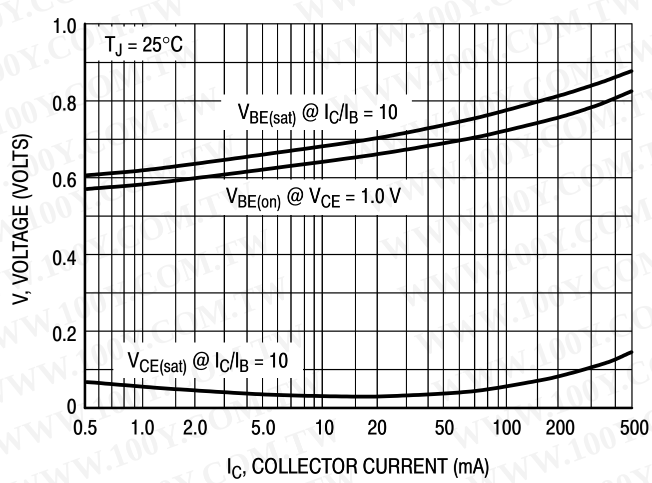



**Figure 6. "ON" Voltages**

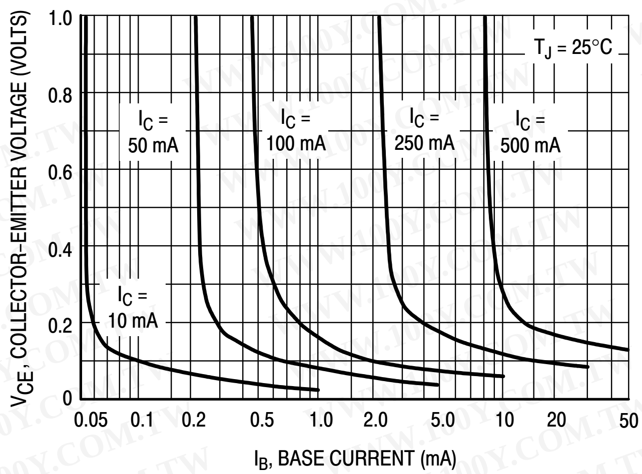



**Figure 7. Collector Saturation Region**

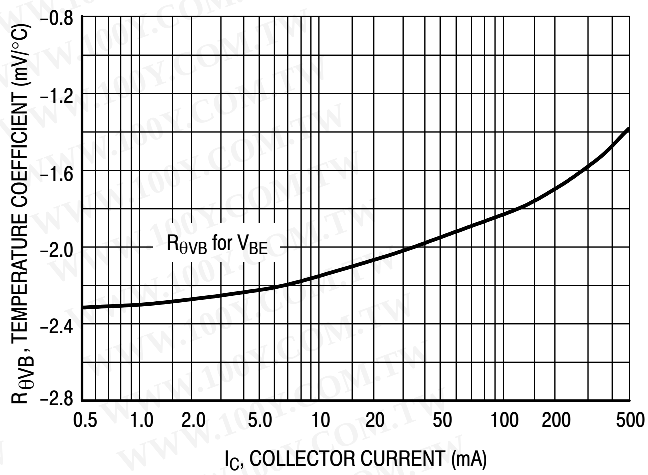
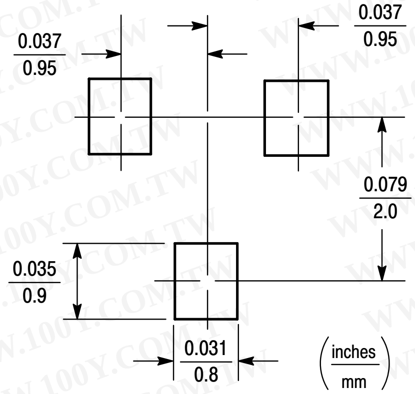



**Figure 8. Base−Emitter Temperature Coefficient**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.






SOT–23

## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

### SOLDERING PRECAUTIONS

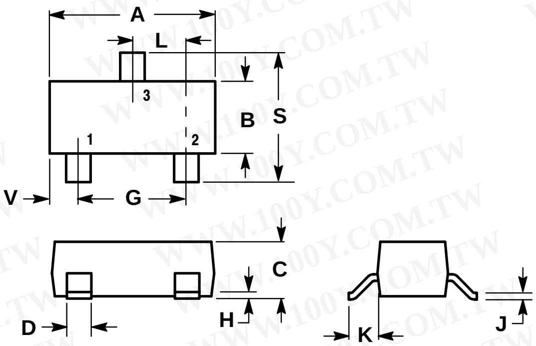
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## PACKAGE DIMENSIONS

### SOT–23 (TO–236)
### CASE 318–08
### ISSUE AH




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318–03 AND –07 OBSOLETE, NEW STANDARD 318–08.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.1102 | 0.1197 | 2.80 | 3.04 |
| B | 0.0472 | 0.0551 | 1.20 | 1.40 |
| C | 0.0350 | 0.0440 | 0.89 | 1.11 |
| D | 0.0150 | 0.0200 | 0.37 | 0.50 |
| G | 0.0701 | 0.0807 | 1.78 | 2.04 |
| H | 0.0005 | 0.0040 | 0.013 | 0.100 |
| J | 0.0034 | 0.0070 | 0.085 | 0.177 |
| K | 0.0140 | 0.0285 | 0.35 | 0.69 |
| L | 0.0350 | 0.0401 | 0.89 | 1.02 |
| S | 0.0830 | 0.1039 | 2.10 | 2.64 |
| V | 0.0177 | 0.0236 | 0.45 | 0.60 |

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

# Notes

Thermal Clad is a registered trademark of the Bergquist Company.



## PUBLICATION ORDERING INFORMATION

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