

Transistors

2.5V Drive Nch+Pch MOSFET

QS6M4

●Structure

Silicon P-channel MOSFET
 Silicon N-channel MOSFET

●Features

- 1) The QS6M4 combines Pch MOSFET with a Nch MOSFET in a single TSMT6 package.
- 2) Low on-state resistance with a fast switching.
- 3) Low voltage drive (2.5V).

●Applications

Load switch, inverter

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6M4		○

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Nchannel	Pchannel	
Drain-source voltage	V _{DSS}	30	-20	V
Gate-source voltage	V _{GSS}	±12	±12	V
Drain current	Continuous	I _D	±1.5	A
	Pulsed	I _{DP} *1	±6.0	A
Source current (Body diode)	Continuous	I _S	0.8	-0.75
	Pulsed	I _{SP} *1	6.0	-6.0
Total power dissipation	P _D *2		1.25	W / TOTAL
			0.9	W / ELEMENT
Channel temperature	T _{ch}		150	°C
Storage temperature	T _{stg}		-55 to +150	°C

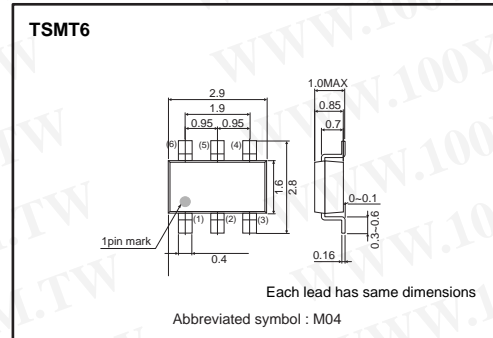
*1 Pw≤10μs, Duty cycles≤1%
 *2 Mounted on a ceramic board

●Thermal resistance

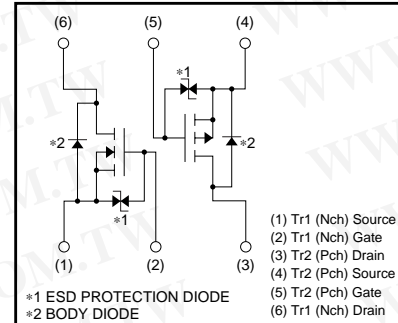
Parameter	Symbol	Limits	Unit
Channel to ambient	R _{th} (ch-a) *	100	°C / W / TOTAL
		139	°C / W / ELEMENT

* Mounted on a ceramic board

●Dimensions (Unit : mm)



●Equivalent circuit



Transistors

●Electrical characteristics (Ta=25°C)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	—	—	±10	μA	V _{GS} =±12V / V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	30	—	—	V	I _D =1mA / V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} =30V / V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	0.5	—	1.5	V	V _{DS} =10V / I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} *	—	170	230	mΩ	I _D =1.5A / V _{GS} =4.5V
		—	180	245		I _D =1.5A / V _{GS} =4.0V
		—	260	360		I _D =1.0A / V _{GS} =2.5V
Forward transfer admittance	Y _{fs} *	1.0	—	—	S	V _{DS} =10V / I _D =1.0A
Input capacitance	C _{iss}	—	80	—	pF	V _{DS} =10V
Output capacitance	C _{oss}	—	25	—	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	—	15	—	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	—	7	—	ns	I _D =1A, V _{DD} =15V
Rise time	t _r *	—	18	—	ns	V _{GS} =4.5V
Turn-off delay time	t _{d(off)} *	—	15	—	ns	R _L =15Ω / R _G =10Ω
Fall time	t _f *	—	15	—	ns	
Total gate charge	Q _g *	—	1.6	—	nC	V _{DD} =15V R _L =10Ω
Gate-source charge	Q _{gs} *	—	0.5	—	nC	V _{GS} =4.5V R _G =10Ω
Gate-drain charge	Q _{gd} *	—	0.9	—	nC	I _D =1.5A

*Pulsed

●Body diode characteristics (Source-Drain)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	—	—	1.2	V	I _S =3.2A / V _{GS} =0V

*Pulsed

Transistors

●Electrical characteristics (Ta=25°C)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{gss}	–	–	±10	μA	V _{GS} =±12V / V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	–20	–	–	V	I _D =–1mA / V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} =–20V / V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	–0.7	–	–2.0	V	V _{DS} =–10V / I _D =–1mA
Static drain-source on-state resistance	R _{DS(on)} *	–	155	215	mΩ	I _D =–1.5A / V _{GS} =–4.5V
		–	170	235		I _D =–1.5A / V _{GS} =–4.0V
		–	310	430		I _D =–0.75A / V _{GS} =–2.5V
Forward transfer admittance	Y _{fs} *	1.0	–	–	S	V _{DS} =–10V / I _D =–0.75A
Input capacitance	C _{iss}	–	270	–	pF	V _{DS} =–10V
Output capacitance	C _{oss}	–	40	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	35	–	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	–	10	–	ns	I _D =–0.75A, V _{DD} ≐–15V
Rise time	t _r *	–	12	–	ns	V _{GS} =–4.5V
Turn-off delay time	t _{d(off)} *	–	45	–	ns	R _L =20Ω / R _G =10Ω
Fall time	t _f *	–	20	–	ns	
Total gate charge	Q _g *	–	3.0	–	nC	V _{DD} ≐–15V R _L =10Ω
Gate-source charge	Q _{gs} *	–	0.8	–	nC	V _{GS} =–4.5V R _G =10Ω
Gate-drain charge	Q _{gd} *	–	0.85	–	nC	I _D =–1.5A

*Pulsed

●Body diode characteristics (Source-Drain)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD}	–	–	–1.2	V	I _S =–0.75A / V _{GS} =0V

Transistors

N-ch

●Electrical characteristic curves

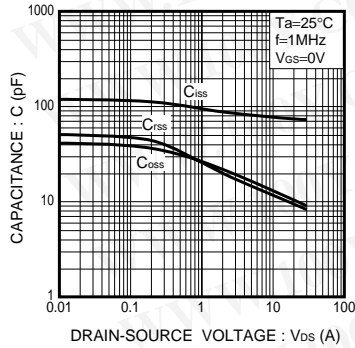


Fig.1 Typical Capacitance vs. Drain-Source Voltage

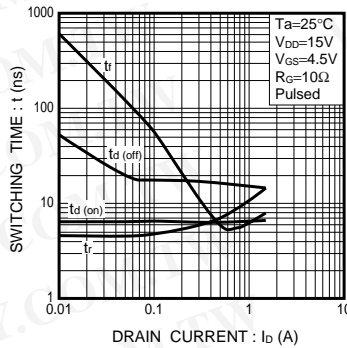


Fig.2 Switching Characteristics

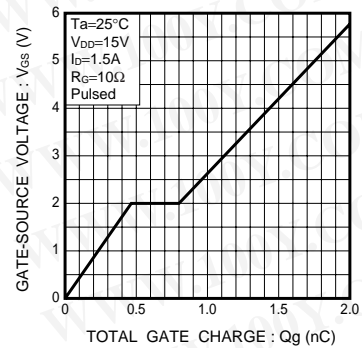


Fig.3 Dynamic Input Characteristics

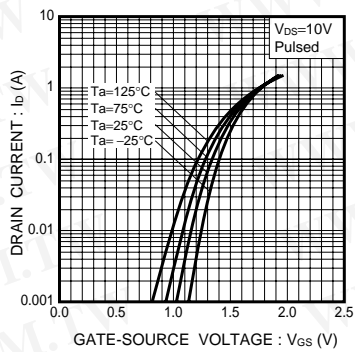


Fig.4 Typical Transfer Characteristics

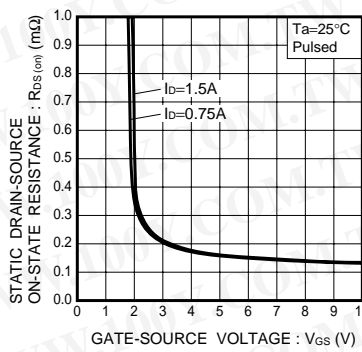


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

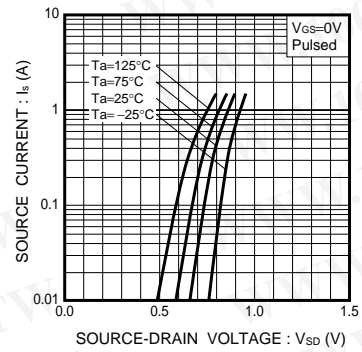


Fig.6 Source Current vs. Source-Drain Voltage

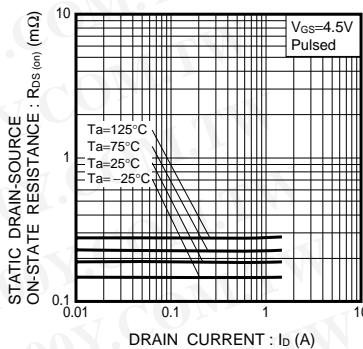


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

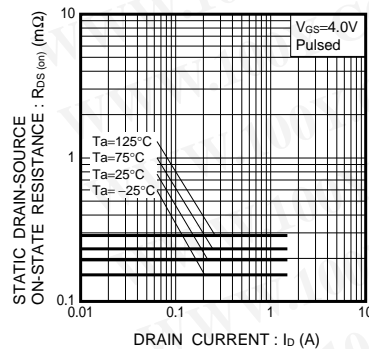


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

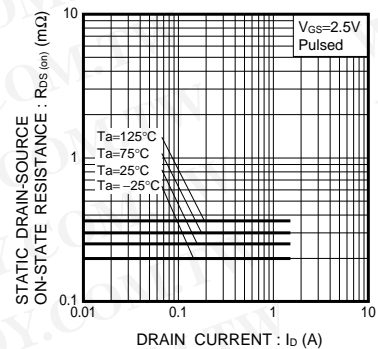


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

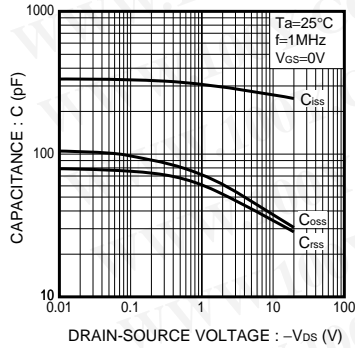


Fig.1 Typical Capacitance vs. Drain-Source Voltage

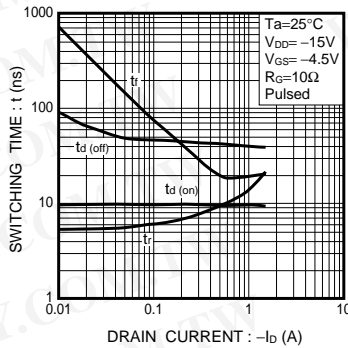


Fig.2 Switching Characteristics

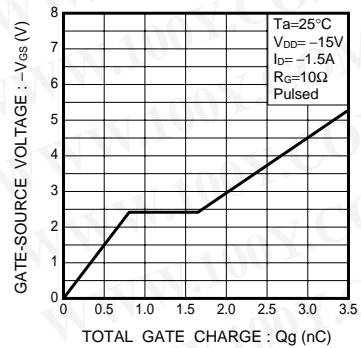


Fig.3 Dynamic Input Characteristics

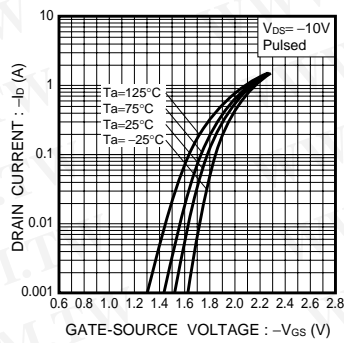


Fig.4 Typical Transfer Characteristics

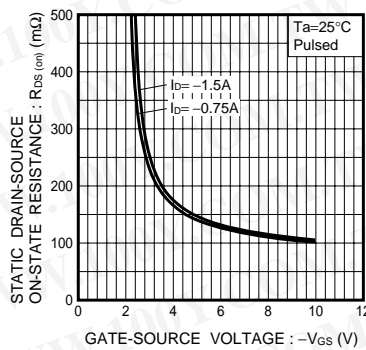


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

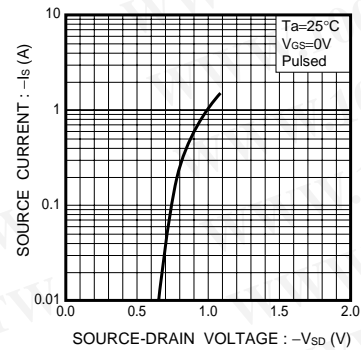


Fig.6 Source Current vs. Source-Drain Voltage

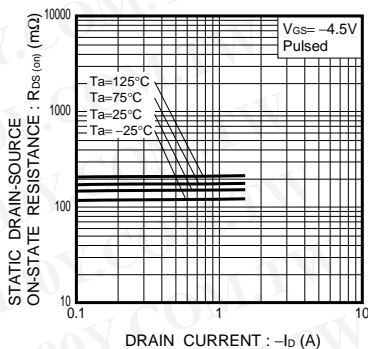


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

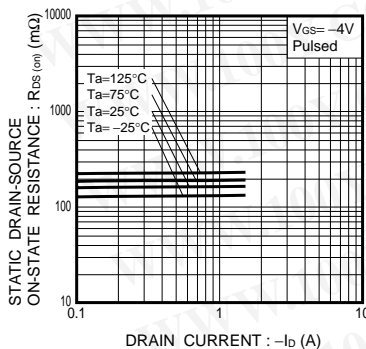


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

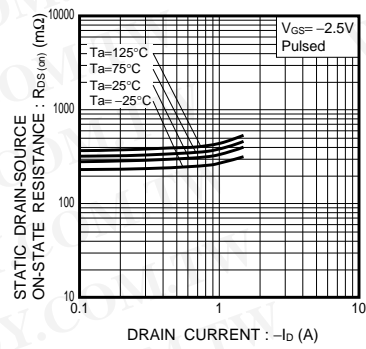


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Appendix

Notes

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