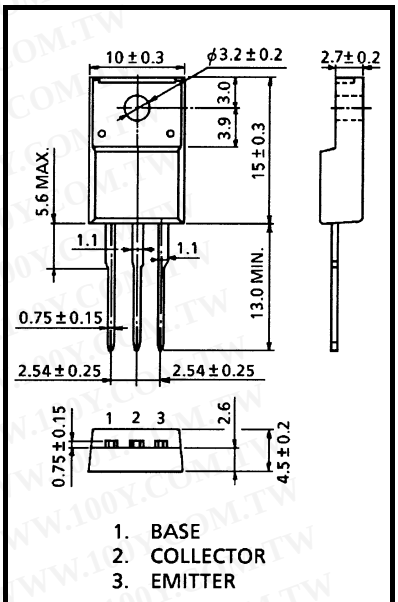
TOSHIBA Transistor Silicon PNP Triple Diffused Type

2SB1375

Audio Frequency Power Amplifier

- Low saturation voltage: $V_{CE\ (sat)}$ = −1.5 V (max) (I_C = −2 A, I_B = −0.2 A)
- High power dissipation: P_C = 25 W (Tc = 25°C)
- Collector metal (fin) is covered with mold resin
- Complementary to 2SD2012

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-10R1A

Weight: 1.7 g (typ.)

Absolute Maximum Ratings (Tc = 25°C)

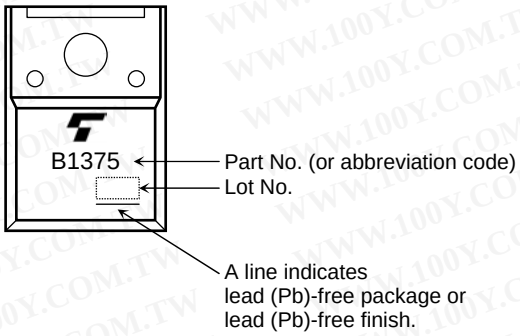
Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	−60	V
Collector-emitter voltage		V_{CEO}	−60	V
Emitter-base voltage		V_{EBO}	−7	V
Collector current		I_C	−3	A
Base current		I_B	−0.5	A
Collector power dissipation	Ta = 25°C	P_C	2.0	W
	Tc = 25°C		25	
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

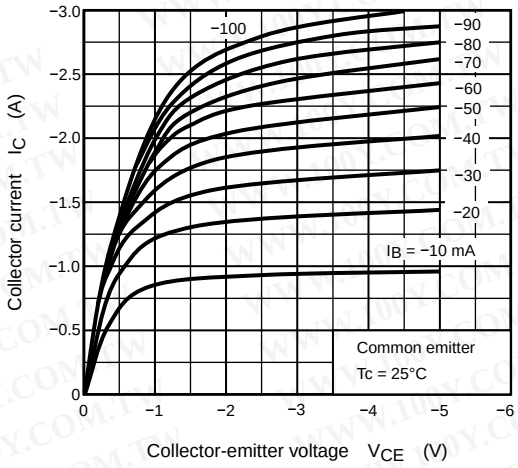
Electrical Characteristics (Tc = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I_{CBO}	V_{CB} = −60 V, I_E = 0	—	—	−10	μA
Emitter cut-off current	I_{EBO}	V_{EB} = −7 V, I_C = 0	—	—	−10	μA
Collector-emitter breakdown voltage	$V_{(BR)\ CEO}$	I_C = −50 mA, I_B = 0	−60	—	—	V
DC current gain	$h_{FE\ (1)}$	V_{CE} = −5 V, I_C = −0.5 A	100	—	320	
	$h_{FE\ (2)}$	V_{CE} = −5 V, I_C = −2 A	15	—	—	
Collector-emitter saturation voltage	$V_{CE\ (sat)}$	I_C = −2 A, I_B = −0.2 A	—	−1.0	−1.5	V
Base-emitter voltage	V_{BE}	V_{CE} = −5 V, I_C = −0.5 A	—	−0.75	−1.0	V
Transition frequency	f_T	V_{CE} = −5 V, I_C = −0.5 A	—	9	—	MHz
Collector output capacitance	C_{ob}	V_{CB} = −10 V, I_E = 0, f = 1 MHz	—	50	—	pF

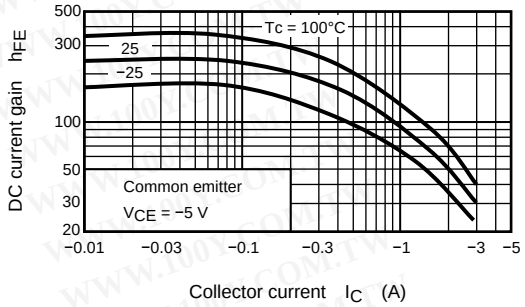
Marking



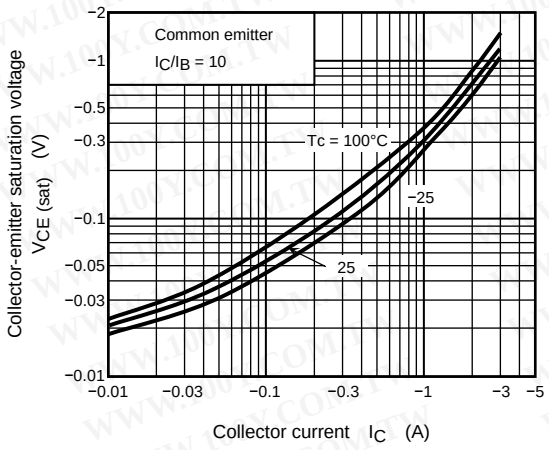
$I_C - V_{CE}$



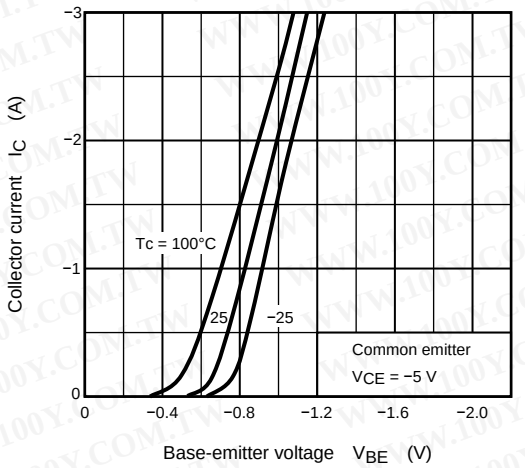
$h_{FE} - I_C$



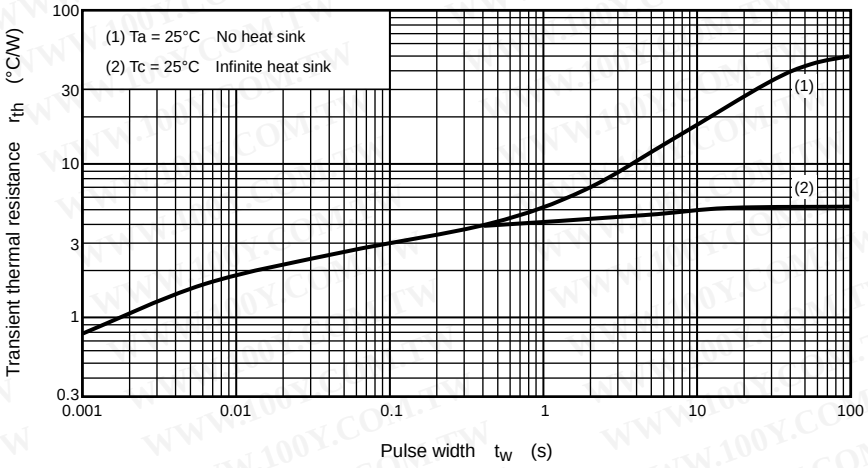
$V_{CE\ (sat)} - I_C$



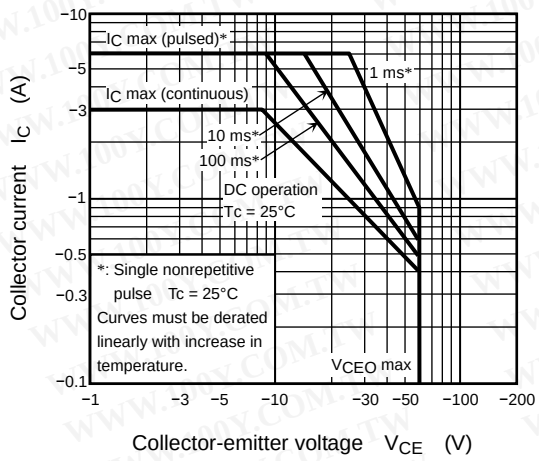
$I_C - V_{BE}$



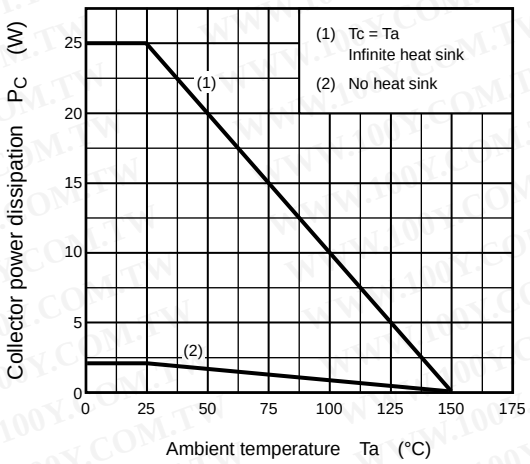
$r_{th} - t_w$



Safe Operating Area



$P_C - Ta$



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