

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS III)

TPCF8102

Notebook PC Applications

Portable Equipment Applications

- Low drain-source ON resistance: $R_{DS(ON)} = 24 \text{ m}\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 14 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = -10 \text{ }\mu\text{A}$ (max) ($V_{DS} = -20 \text{ V}$)
- Enhancement mode: $V_{th} = -0.5 \text{ to } -1.2 \text{ V}$
($V_{DS} = -10 \text{ V}$, $I_D = -200 \text{ }\mu\text{A}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	-20	V
Gate-source voltage		V_{GSS}	± 8	V
Drain current	DC (Note 1)	I_D	-6	A
	Pulsed (Note 1)	I_{DP}	-24	
Drain power dissipation ($t = 5 \text{ s}$) (Note 2a)		P_D	2.5	W
Drain power dissipation ($t = 5 \text{ s}$) (Note 2b)		P_D	0.7	W
Single pulse avalanche energy (Note 3)		E_{AS}	5.9	mJ
Avalanche current		I_{AR}	-3	A
Repetitive avalanche energy (Note 4)		E_{AR}	0.25	mJ
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

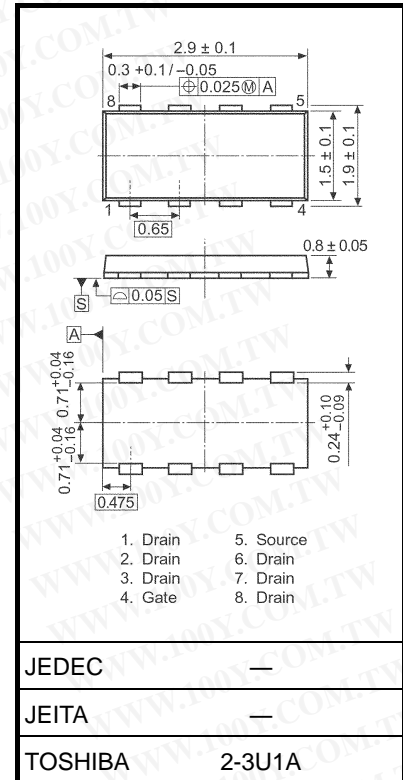
Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient ($t = 5 \text{ s}$) (Note 2a)	$R_{th(ch-a)}$	50.0	$^\circ\text{C/W}$
Thermal resistance, channel to ambient ($t = 5 \text{ s}$) (Note 2b)	$R_{th(ch-a)}$	178.6	$^\circ\text{C/W}$

Note: (Note 1), (Note 2), (Note 3), (Note 4) and (Note 5): See the next page.

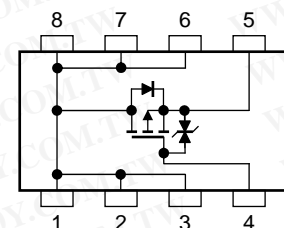
This transistor is an electrostatic-sensitive device. Please handle with caution.

Unit: mm

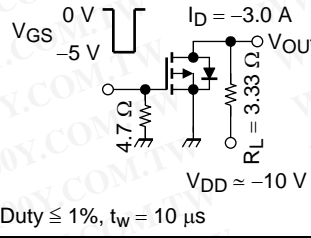


Weight: 0.011 g (typ.)

Circuit Configuration



Electrical Characteristics (Ta = 25°C)

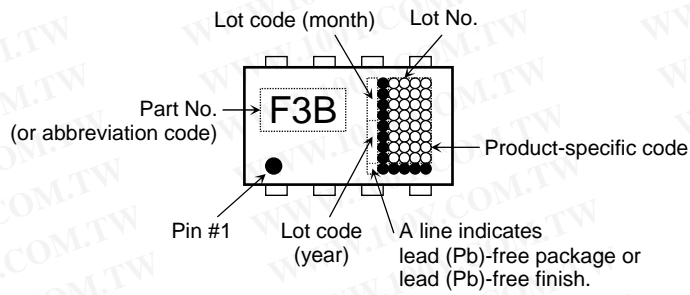
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-10	μA
Drain-source breakdown voltage	$V_{(BR) DSS}$		$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR) DSX}$		$I_D = -10 \text{ mA}, V_{GS} = 8 \text{ V}$	-12	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = -10 \text{ V}, I_D = -200 \mu\text{A}$	-0.5	—	-1.2	V
Drain-source ON resistance	$R_{DS(ON)}$		$V_{GS} = -1.8 \text{ V}, I_D = -1.5 \text{ A}$	—	67	90	m Ω
	$R_{DS(ON)}$		$V_{GS} = -2.5 \text{ V}, I_D = -3.0 \text{ A}$	—	36	41	
	$R_{DS(ON)}$		$V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$	—	24	30	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10 \text{ V}, I_D = -3.0 \text{ A}$	7	14	—	S
Input capacitance		C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	1550	—	pF
Reverse transfer capacitance		C_{rss}		—	215	—	
Output capacitance		C_{oss}		—	265	—	
Switching time	Rise time	t_r	 $V_{GS} = 0 \text{ V} \rightarrow -5 \text{ V}$ $I_D = -3.0 \text{ A}$ $V_{DD} \approx -10 \text{ V}$ $R_L = 3.33 \Omega$ $Duty \leq 1\%, t_w = 10 \mu\text{s}$	—	7	—	ns
	Turn-on time	t_{on}		—	13	—	
	Fall time	t_f		—	21	—	
	Turn-off time	t_{off}		—	68	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx -16 \text{ V}, V_{GS} = -5 \text{ V}, I_D = -6.0 \text{ A}$	—	19	—	nC
Gate-source charge		Q_{gs}		—	14	—	
Gate-drain ("miller") charge		Q_{gd}		—	5	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	-24	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = -6.0 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	1.2	V

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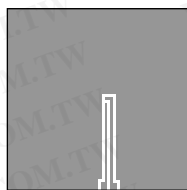
Marking (Note 5)



Note 1: Ensure that the channel temperature does not exceed 150°C.

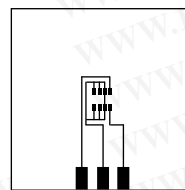
Note 2: (a) Device mounted on a glass-epoxy board (a)

(b) Device mounted on a glass-epoxy board (b)



(a)

FR-4
25.4 × 25.4 × 0.8
Unit: (mm)



(b)

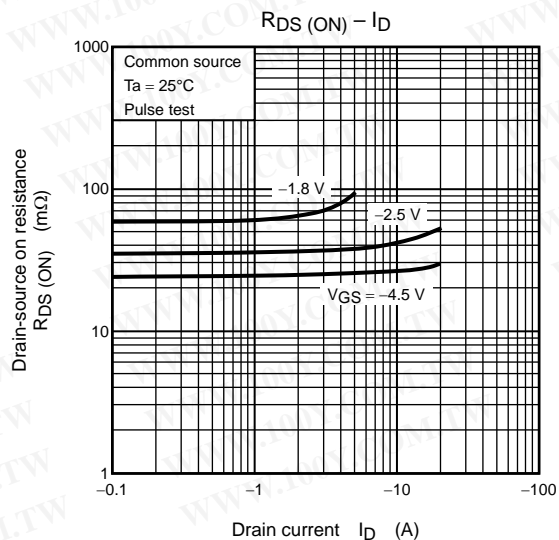
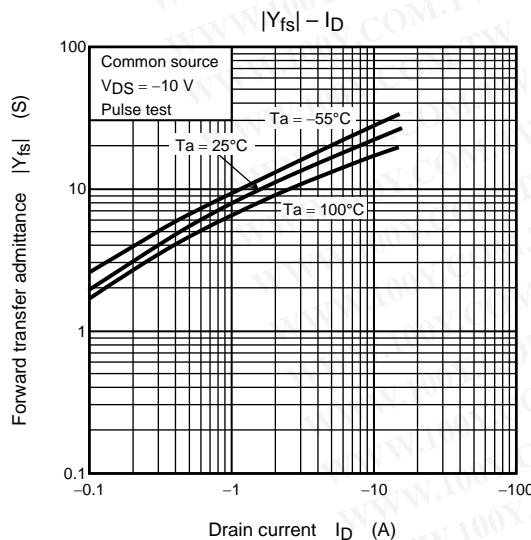
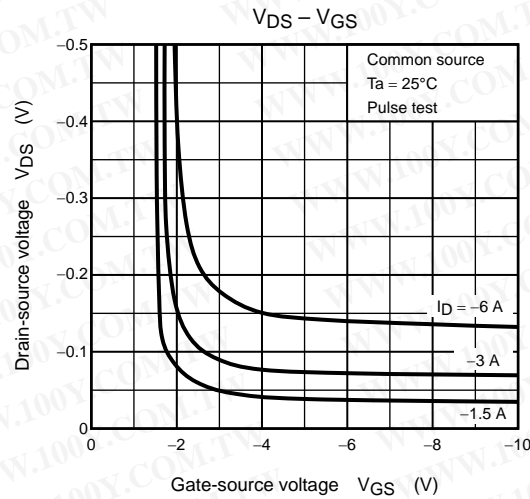
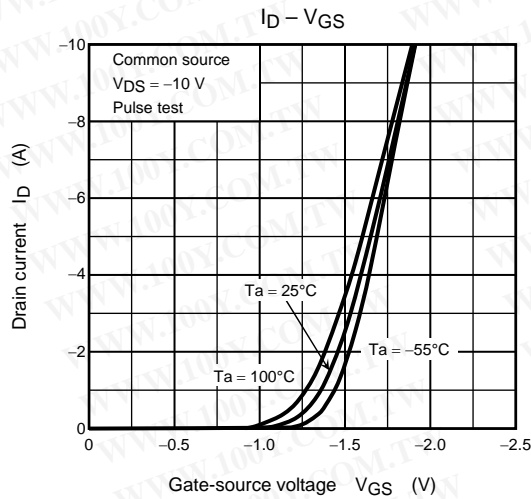
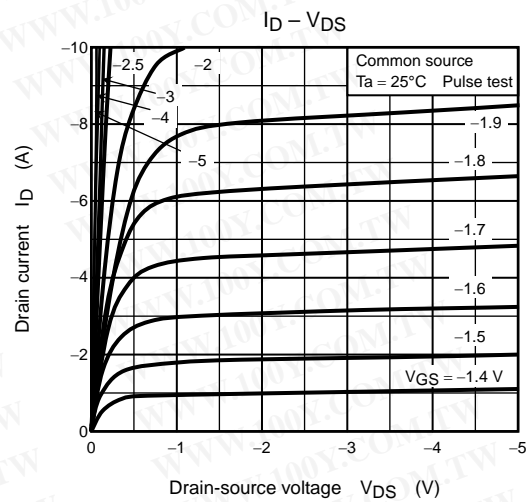
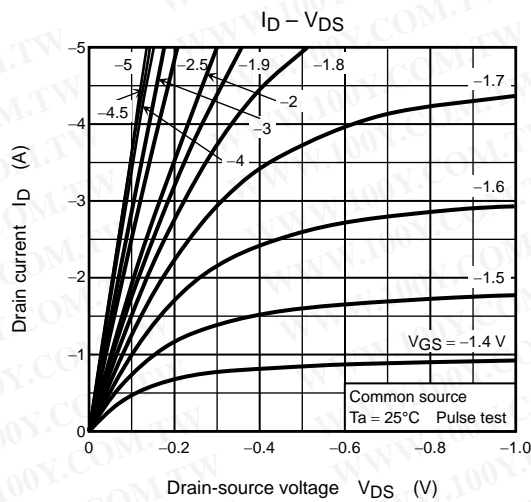
FR-4
25.4 × 25.4 × 0.8
Unit: (mm)

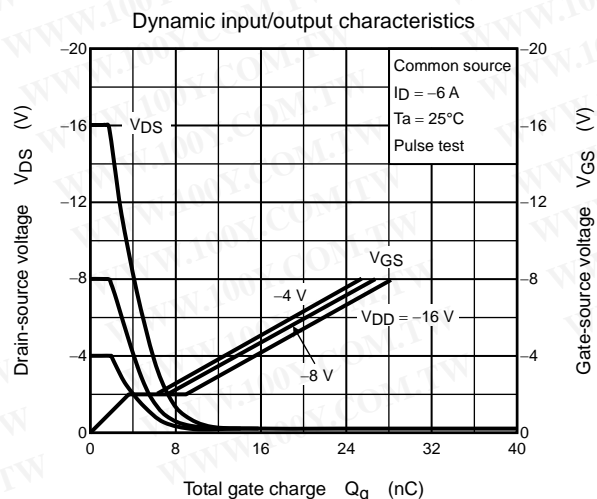
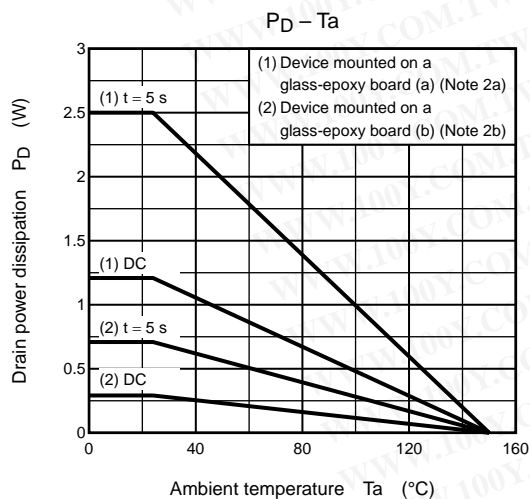
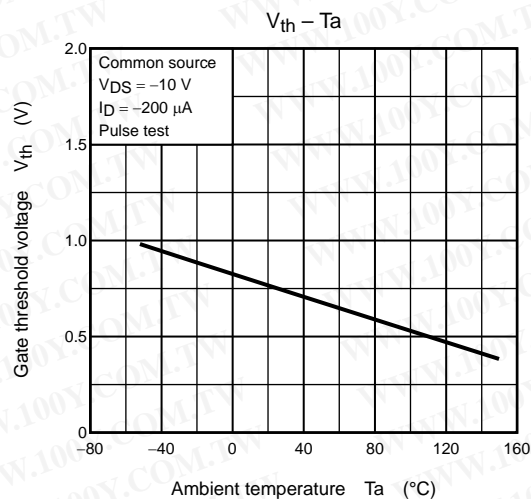
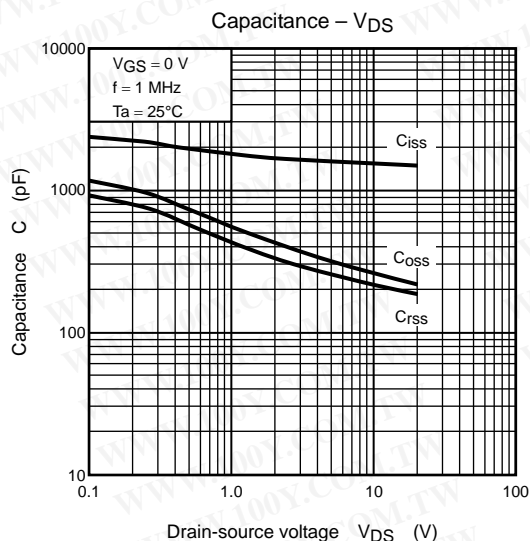
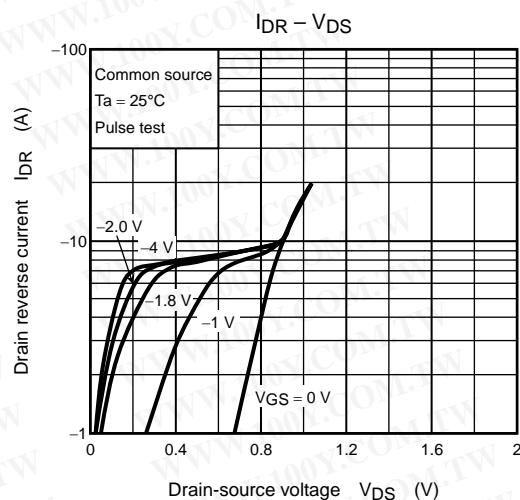
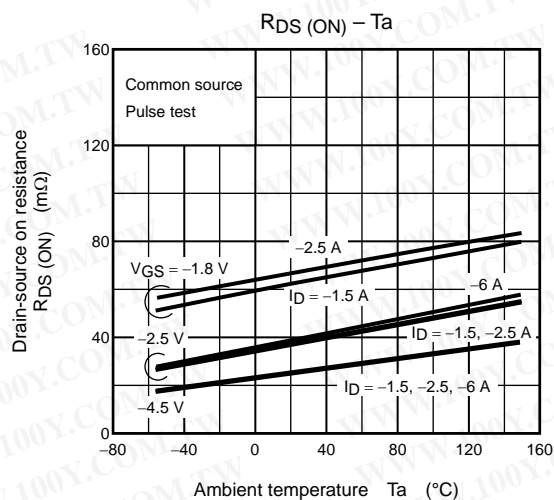
Note 3: $V_{DD} = -16\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 0.5\text{ mH}$, $R_G = 25\ \Omega$, $I_{AR} = -3.0\text{ A}$

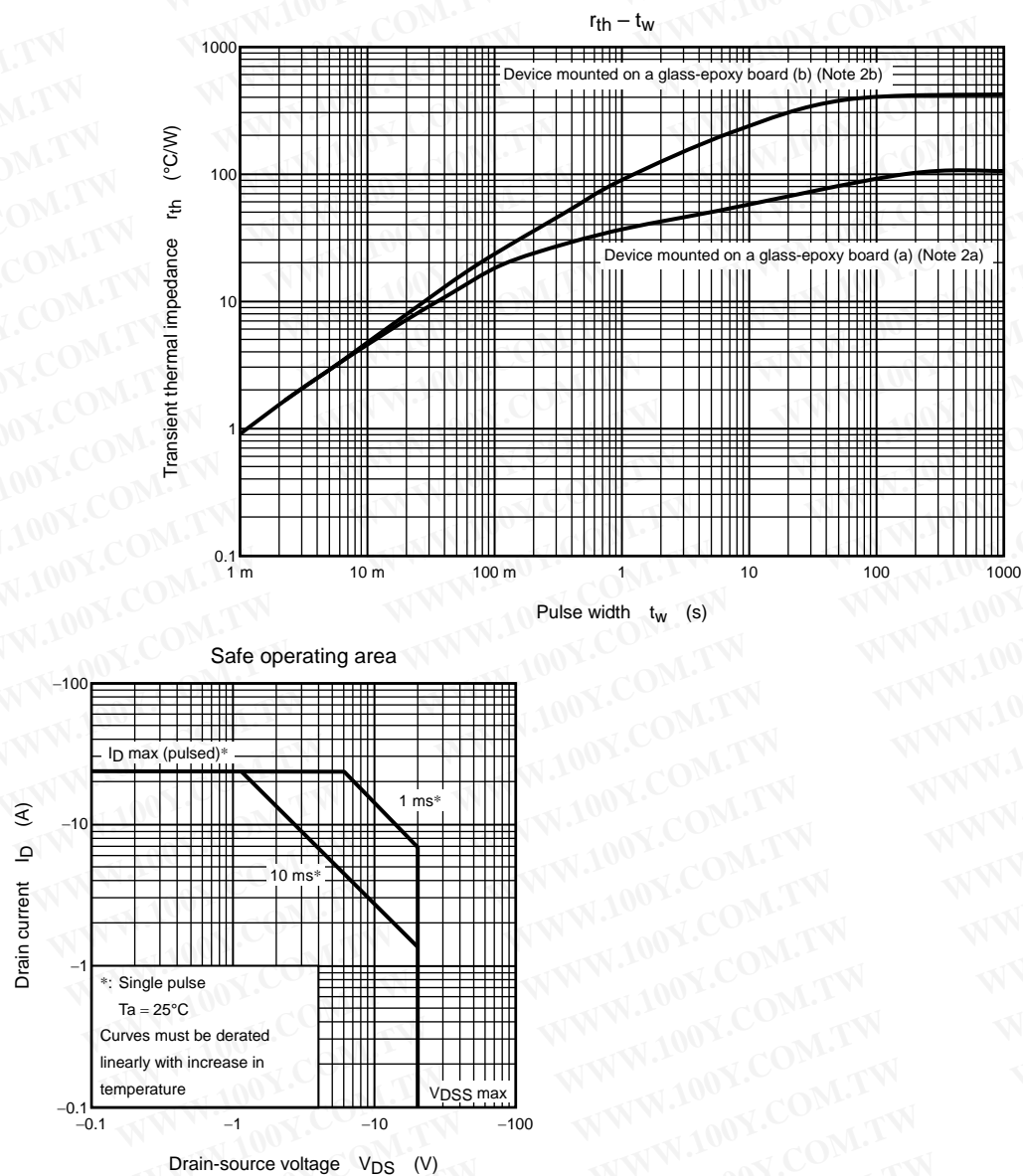
Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: A dot on the lower left of the marking indicates Pin 1.

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