

INTERNATIONAL RECTIFIER

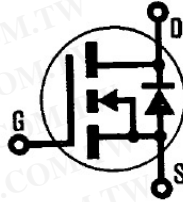
INTERNATIONAL RECTIFIER 

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
 Http://www.100y.com.tw

**HEXFET® TRANSISTORS**  
**N-CHANNEL**  
**HEXDIP™**

**IRFD020**  
**IRFD022**

1-WATT RATED POWER MOSFETs  
 IN A 4-PIN, DUAL-IN-LINE PACKAGE



4-PIN DIP

**50 Volt, 0.10 Ohm, 1-Watt HEXDIP**

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. Efficient geometry and unique processing of the HEXFET design achieve a very low on-state resistance combined with high transconductance and great device ruggedness. HEXFETs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

The HEXDIP 4-pin, Dual-In-Line Package brings the advantages of HEXFETs to high volume applications where automatic PC Board insertion is desirable, such as circuit boards for computers, printers, telecommunications equipment and consumer products. Their compatibility with automatic insertion equipment, low-profile and end-stackable features represent the state-of-the-art in power device packaging

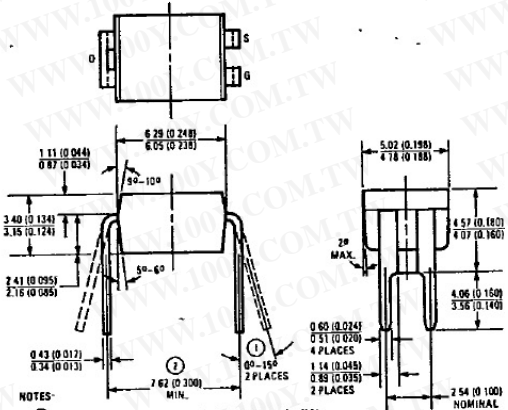
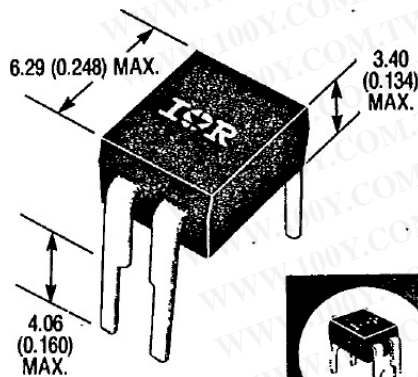
**FEATURES:**

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Excellent Temperature Stability

**Product Summary**

Part Number	V <sub>DS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
IRFD020	50V	0.10Ω	2.4A
IRFD022	-50V	0.12Ω	2.2A

**CASE STYLE AND DIMENSIONS**



NOTES:  
 ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION  
 ② APPLIES TO INSTALLED LEAD CENTERS.

Case Style HD-1 (Similar to JEDEC Outline MO-001)  
 Dimensions in Millimeters and (Inches)

IRFD020, IRFD022 Devices

INTERNATIONAL RECTIFIER

T-35-25

Absolute Maximum Ratings

Parameter	IRFD020	IRFD022	Units
V <sub>DS</sub> Drain - Source Voltage ①	50	50	V
V <sub>DGR</sub> Drain - Gate Voltage (R <sub>GS</sub> = 20 K $\Omega$ ) ①	50	50	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C Continuous Drain Current	2.4	2.2	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C Continuous Drain Current	1.5	1.4	A
I <sub>DM</sub> Pulsed Drain Current ②	19	18	A
V <sub>GS</sub> Gate - Source Voltage	±20		V
P <sub>D</sub> @ T <sub>C</sub> = 25°C Max. Power Dissipation	1.0		W
Linear Derating Factor	0.0080		W/K ③
I <sub>LM</sub> Inductive Current, Clamped	(See Fig. 14) L = 100 $\mu$ H		A
I <sub>L</sub> Unclamped Inductive Current (Avalanche Current) ④	(See Fig. 15) 2.2		A
T <sub>J</sub> Operating Junction and Storage Temperature Range	-55 to 150		°C
T <sub>stg</sub> Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T<sub>C</sub> = 25°C (Unless Otherwise Specified)


Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub> Drain - Source Breakdown Voltage	IRFD020	50	—	—	V	V <sub>GS</sub> = 0V I <sub>D</sub> = 250 $\mu$ A
	IRFD022	—	—	—	—	—
V <sub>GS(th)</sub> Gate Threshold Voltage	ALL	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu$ A
I <sub>GSS</sub> Gate-Source Leakage Forward	ALL	—	—	500	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub> Gate-Source Leakage Reverse	ALL	—	—	-500	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	ALL	—	—	250	$\mu$ A	V <sub>DS</sub> = Max. Rating, V <sub>GS</sub> = 0V
		—	—	1000	$\mu$ A	V <sub>DS</sub> = Max. Rating $\times$ 0.8, V <sub>GS</sub> = 0V, T <sub>C</sub> = 125°C
I <sub>D(on)</sub> On-State Drain Current ⑤	IRFD020	2.4	—	—	A	V <sub>DS</sub> > I <sub>D(on)</sub> $\times$ R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10V
	IRFD022	2.2	—	—	A	
R <sub>DS(on)</sub> Static Drain-Source On-State Resistance ⑥	IRFD020	—	0.080	0.10	$\Omega$	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.4A
	IRFD022	—	0.11	0.12	$\Omega$	
g <sub>fs</sub> Forward Transconductance ⑦	ALL	4.9	7.3	—	S/(V)	V <sub>DS</sub> = 2 $\times$ V <sub>GS</sub> , I <sub>DS</sub> = 7.5A
C <sub>iss</sub> Input Capacitance	ALL	—	400	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0 MHz
C <sub>oss</sub> Output Capacitance	ALL	—	260	—	pF	See Fig. 10
C <sub>rss</sub> Reverse Transfer Capacitance	ALL	—	44	—	pF	—
t <sub>d(on)</sub> Turn-On Delay Time	ALL	—	8.7	13	ns	V <sub>DD</sub> = 25V, I <sub>D</sub> $\approx$ 15A, R <sub>G</sub> = 18 $\Omega$ , R <sub>D</sub> = 1.7 $\Omega$
t <sub>r</sub> Rise Time	ALL	—	55	83	ns	See Fig. 16
t <sub>d(off)</sub> Turn-Off Delay Time	ALL	—	16	24	ns	(MOSFET switching times are essentially independent of operating temperature.)
t <sub>f</sub> Fall Time	ALL	—	26	39	ns	—
Q <sub>g</sub> Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	16	24	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 15A, V <sub>DS</sub> = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q <sub>gs</sub> Gate-Source Charge	ALL	—	4.7	7.1	nC	—
Q <sub>gd</sub> Gate-Drain ("Miller") Charge	ALL	—	4.7	7.1	nC	—
L <sub>D</sub> Internal Drain Inductance	ALL	—	4.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L <sub>S</sub> Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.



Thermal Resistance

R <sub>thJA</sub> Junction-to-Ambient	ALL	—	—	120	K/W ⑧	Typical socket mount
---------------------------------------	-----	---	---	-----	-------	----------------------

Source-Drain Diode Ratings and Characteristics

$I_S$	Continuous Source Current (Body Diode)	IRFD020	—	—	2.4	A	Modified MOSFET symbol showing the integral reverse PN junction rectifier.
		IRFD022	—	—	2.2	A	
$I_{SM}$	Pulse Source Current (Body Diode) ③	IRFD020	—	—	19	A	
		IRFD022	—	—	18	A	
$V_{SD}$	Diode Forward Voltage ④	ALL	—	—	1.4	V	$T_C = 25^\circ\text{C}, I_S = 2.4\text{A}, V_{GS} = 0\text{V}$
$t_{rr}$	Reverse Recovery Time	ALL	57	130	310	ns	$T_J = 25^\circ\text{C}, I_F = 15\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
$Q_{RR}$	Reverse Recovered Charge	ALL	0.17	0.34	0.85	$\mu\text{C}$	$T_J = 25^\circ\text{C}, I_F = 15\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
$t_{on}$	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$ .				

①  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$     ② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).  
 ③ @  $V_{dd} = 25\text{V}, T_J = 25^\circ\text{C}$     ④ Pulse Test: Pulse width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$   
 ⑤  $KW = ^\circ\text{C}/\text{W}$      $L = 100 \mu\text{H}, R_G = 25\Omega$

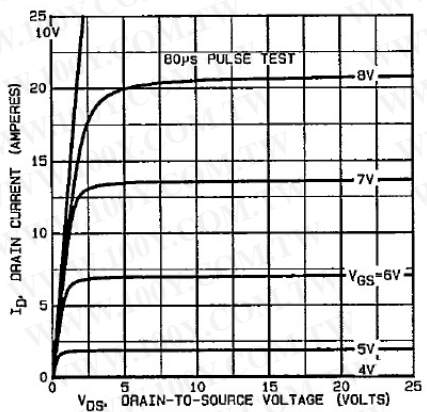


Fig. 1 — Typical Output Characteristics

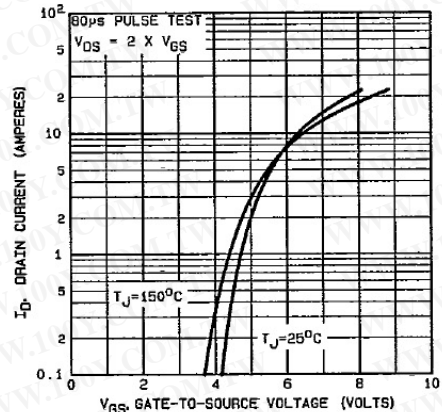


Fig. 2 — Typical Transfer Characteristics

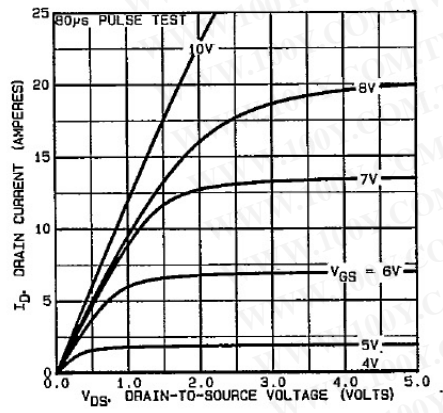


Fig. 3 — Typical Saturation Characteristics

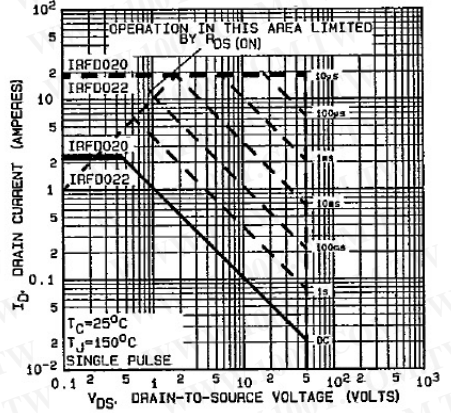


Fig. 4 — Maximum Safe Operating Area

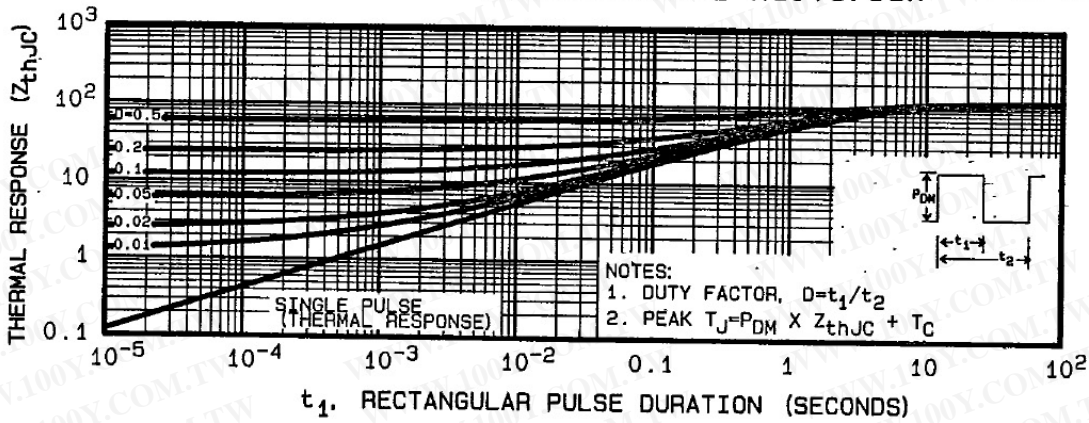


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

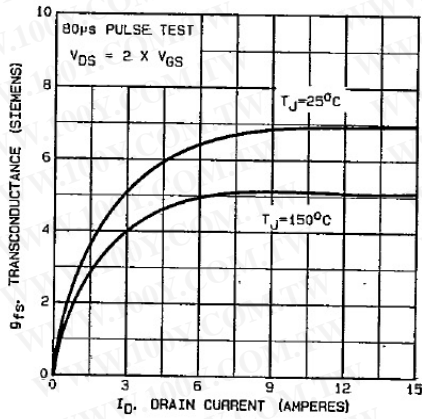


Fig. 6 — Typical Transconductance Vs. Drain Current

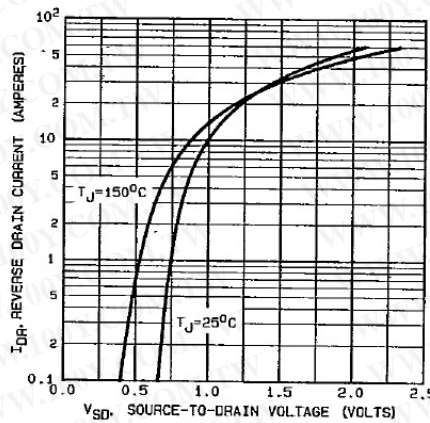


Fig. 7 — Typical Source-Drain Diode Forward Voltage

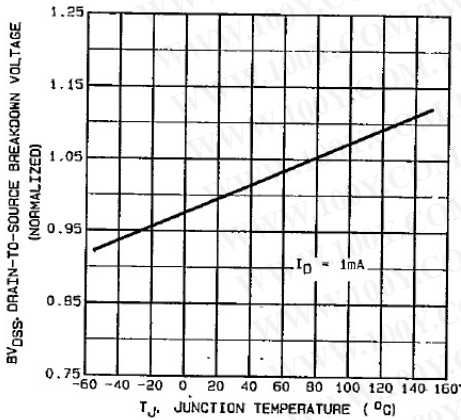


Fig. 8 — Breakdown Voltage Vs. Temperature

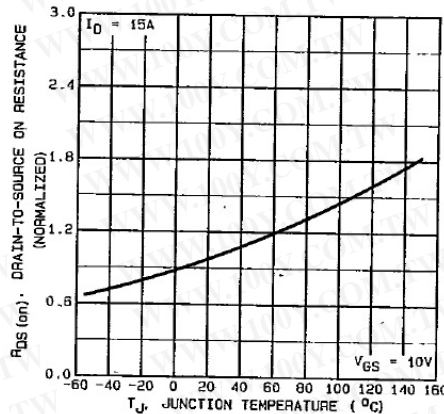


Fig. 9 — Normalized On-Resistance Vs. Temperature

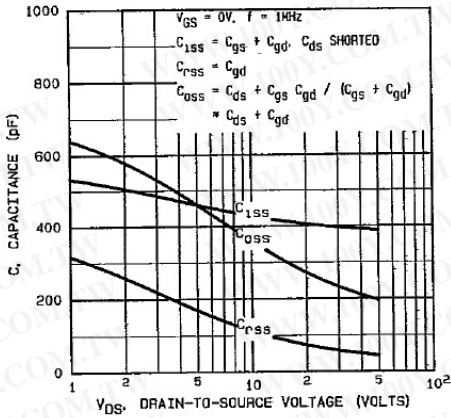


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

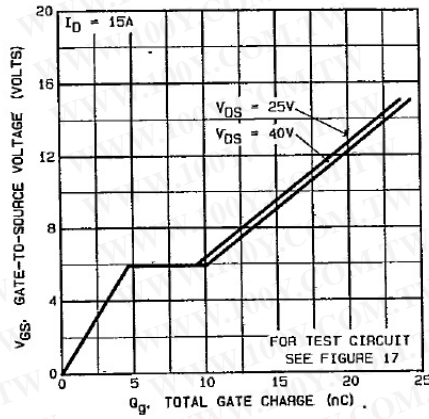


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

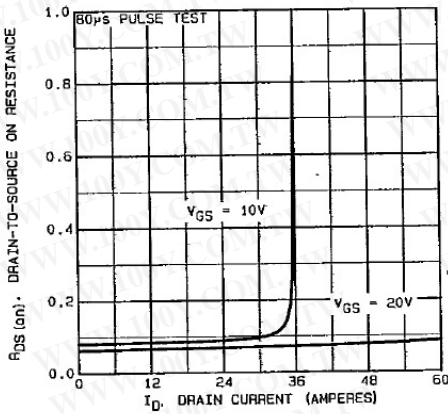


Fig. 12 — Typical On-Resistance Vs. Drain Current

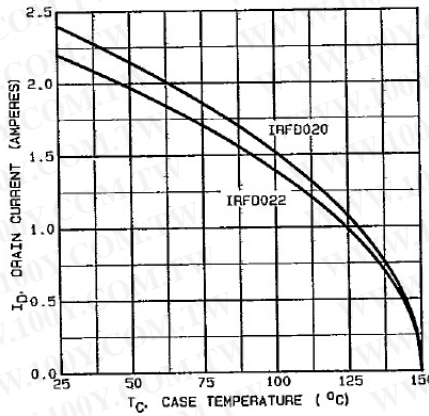


Fig. 13 — Maximum Drain Current Vs. Case Temperature

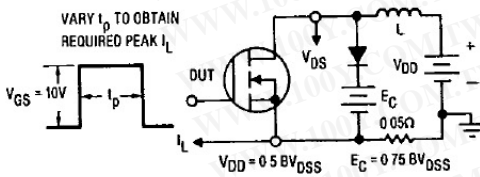


Fig. 14a — Clamped Inductive Test Circuit

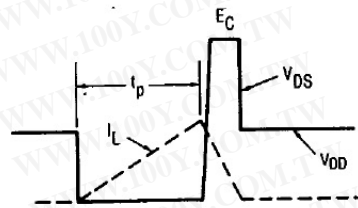


Fig. 14b — Clamped Inductive Waveforms



IRFD020, IRFD022 Devices

INTERNATIONAL RECTIFIER

T-35-25

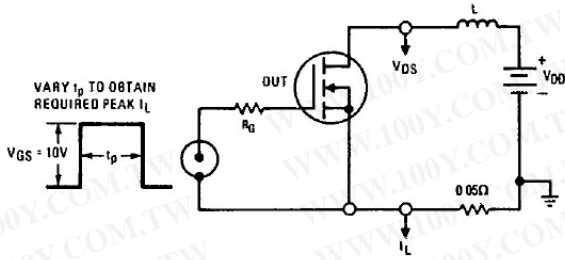


Fig. 15a — Unclamped Inductive Test Circuit

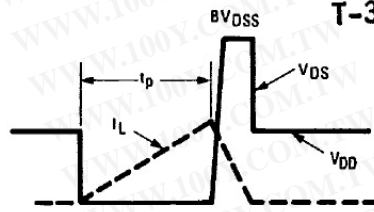


Fig. 15b — Unclamped Inductive Load Test Waveforms

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

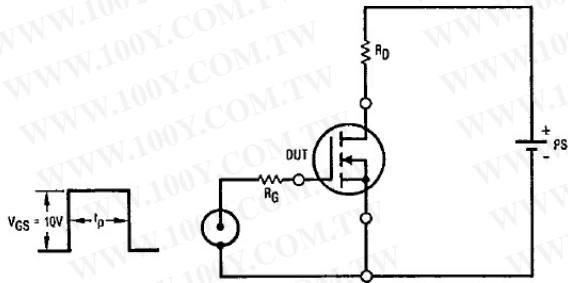


Fig. 16 — Switching Time Test Circuit

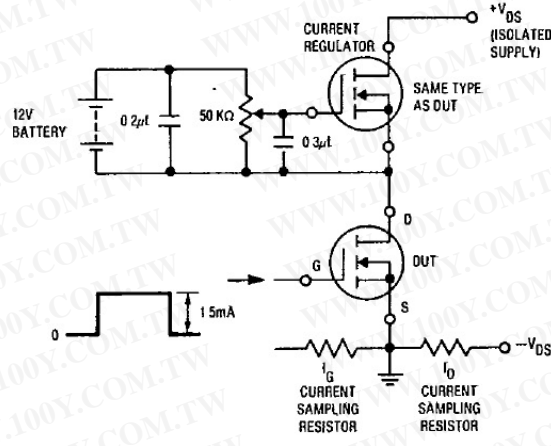
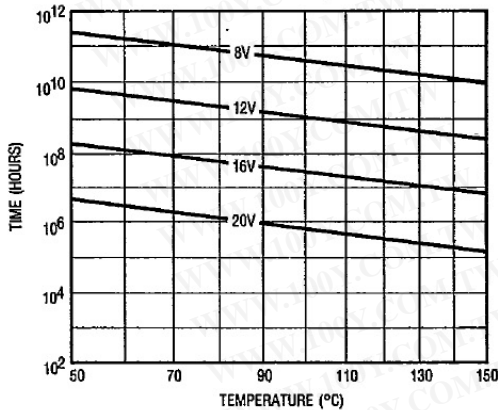
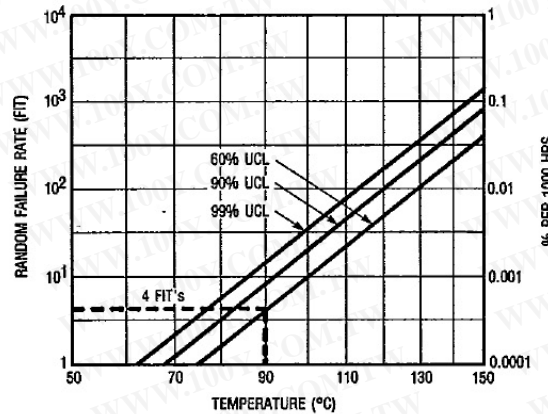


Fig. 17 — Gate Charge Test Circuit



\*Fig. 18 — Typical Time to Accumulated 1% Gate Failure



\*Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

\*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.