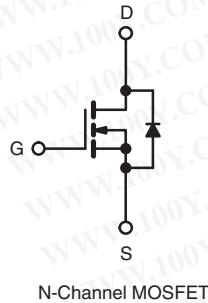
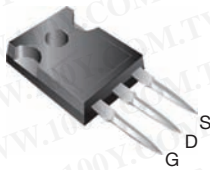


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Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	800	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	3.0
Q_g (Max.) (nC)	78	
Q_{gs} (nC)	9.6	
Q_{gd} (nC)	45	
Configuration	Single	

TO-247AC


FEATURES

- Dynamic dV/dt Rated
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



RoHS*
 COMPLIANT

DESCRIPTION

Third Generation Power MOSFETs from Vishay provide the designer with best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFPE30PbF
	SiHFPE30-E3
SnPb	IRFPE30
	SiHFPE30

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	800	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C	4.1
		$T_C = 100$ °C	2.6
Pulsed Drain Current ^a	I_{DM}	16	A
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	170	mJ
Repetitive Avalanche Current ^a	I_{AR}	4.1	A
Repetitive Avalanche Energy ^a	E_{AR}	13	mJ
Maximum Power Dissipation	P_D	125	W
		$T_C = 25$ °C	
Peak Diode Recovery dV/dt ^c	dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 18$ mH, $R_g = 25$ Ω , $I_{AS} = 4.1$ A (see fig. 12).
- $I_{SD} \leq 4.1$ A, $dI/dt \leq 100$ A/ μ s, $V_{DD} \leq 600$, $T_J \leq 150$ °C.
- 1.6 mm from case.



* Pb containing terminations are not RoHS compliant, exemptions may apply

IRFPE30, SiHFPE30

Vishay Siliconix



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		800	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.90	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$		-	-	100	μA
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 2.5\text{ A}^b$	-	-	3.0	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 2.5\text{ A}^b$		2.4	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	1300	-	pF
Output Capacitance	C_{oss}			-	310	-	
Reverse Transfer Capacitance	C_{rss}			-	190	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 4.1\text{ A}, V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	78	nC
Gate-Source Charge	Q_{gs}			-	-	9.6	
Gate-Drain Charge	Q_{gd}			-	-	45	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}, I_D = 4.1\text{ A}, R_g = 12\text{ }\Omega, R_D = 95\text{ }\Omega$, see fig. 10 ^b		-	12	-	ns
Rise Time	t_r			-	33	-	
Turn-Off Delay Time	$t_{d(off)}$			-	82	-	
Fall Time	t_f			-	30	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	5.0	-	nH
Internal Source Inductance	L_S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	4.1	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	16	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 4.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 4.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	480	720	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.8	2.7	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

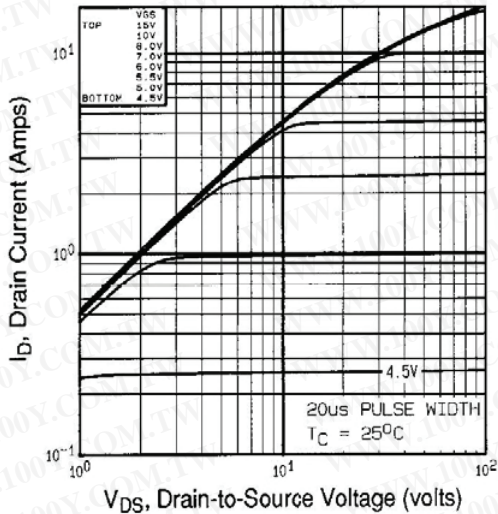


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

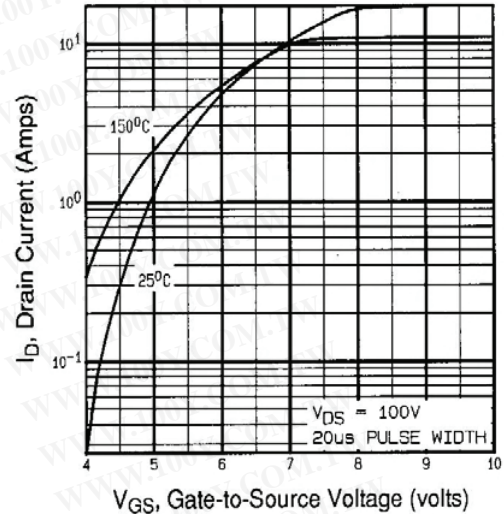


Fig. 3 - Typical Transfer Characteristics

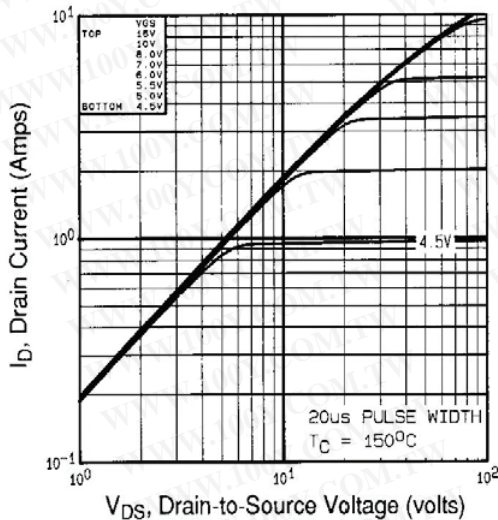


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

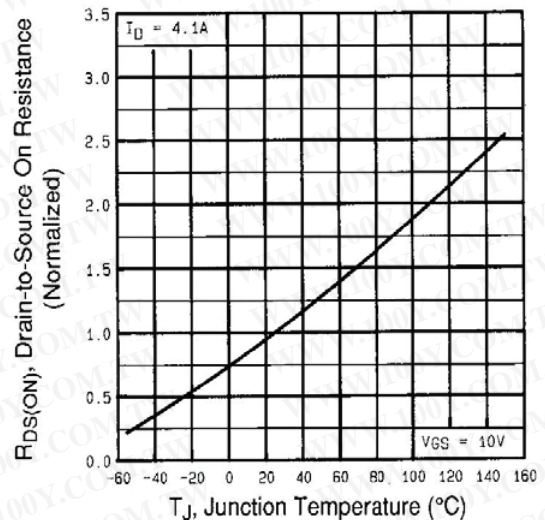


Fig. 4 - Normalized On-Resistance vs. Temperature

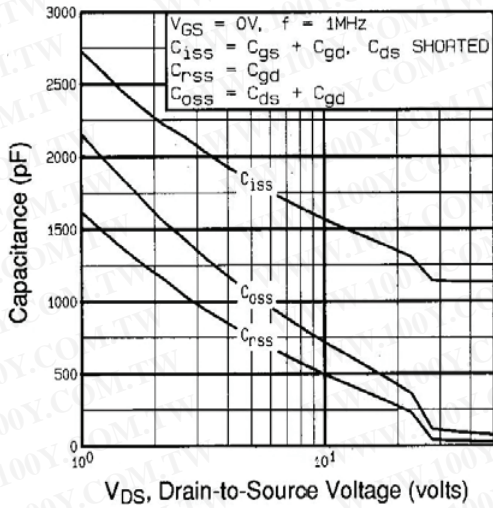


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

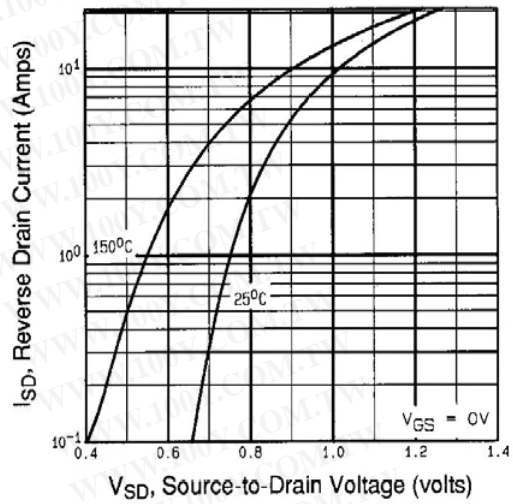


Fig. 7 - Typical Source-Drain Diode Forward Voltage

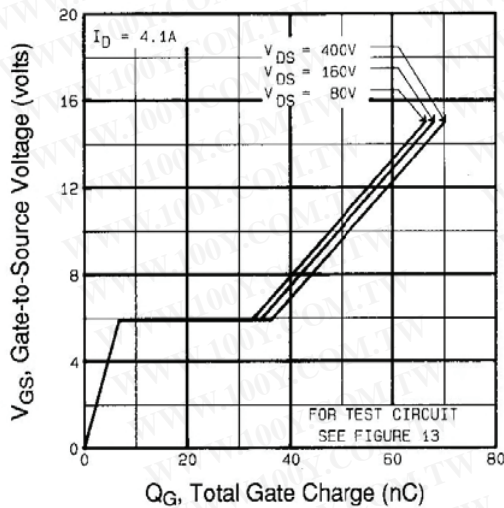


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

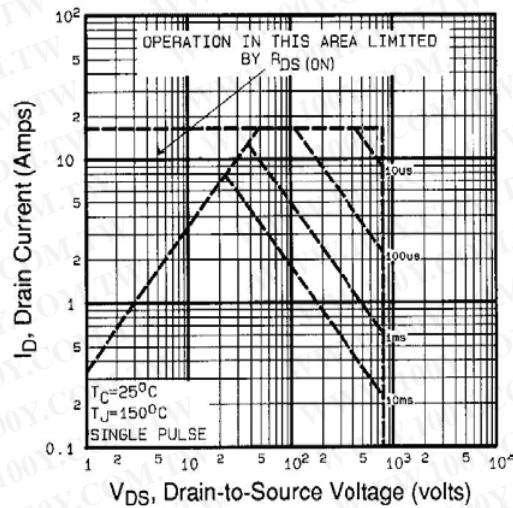


Fig. 8 - Maximum Safe Operating Area

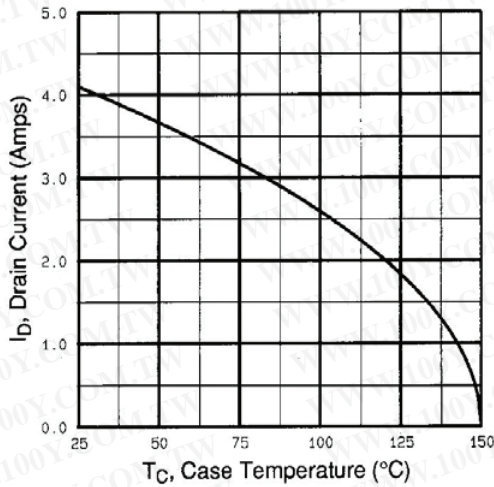


Fig. 9 - Maximum Drain Current vs. Case Temperature

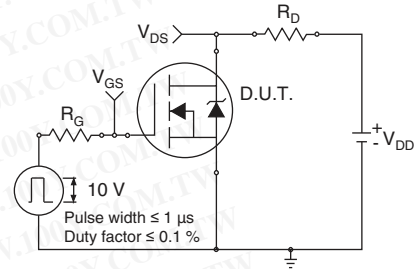


Fig. 10a - Switching Time Test Circuit

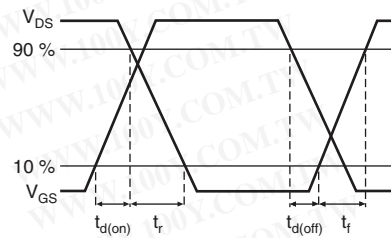


Fig. 10b - Switching Time Waveforms

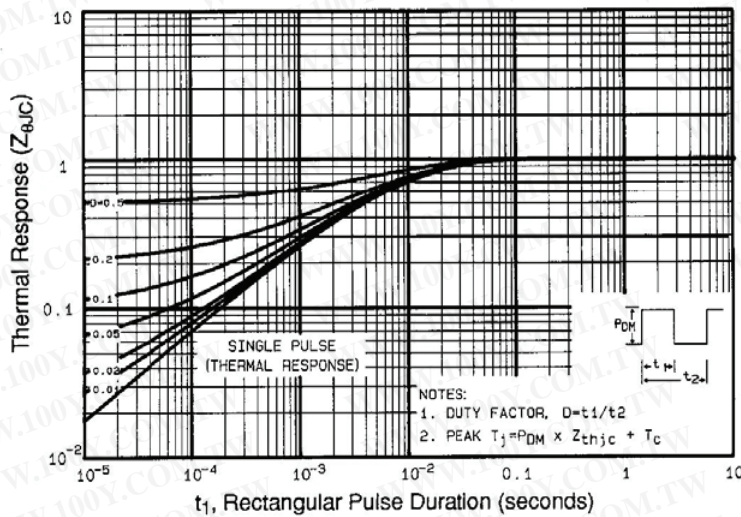


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

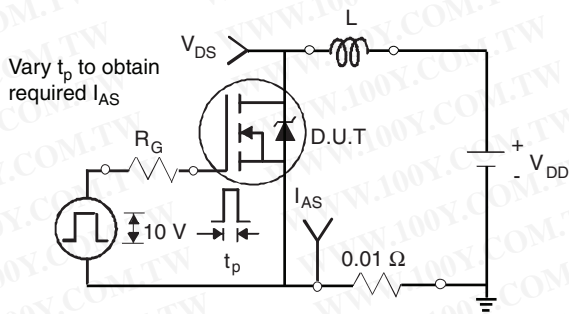


Fig. 12a - Unclamped Inductive Test Circuit

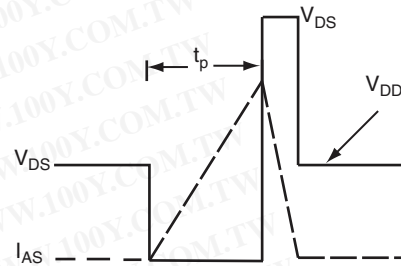


Fig. 12b - Unclamped Inductive Waveforms

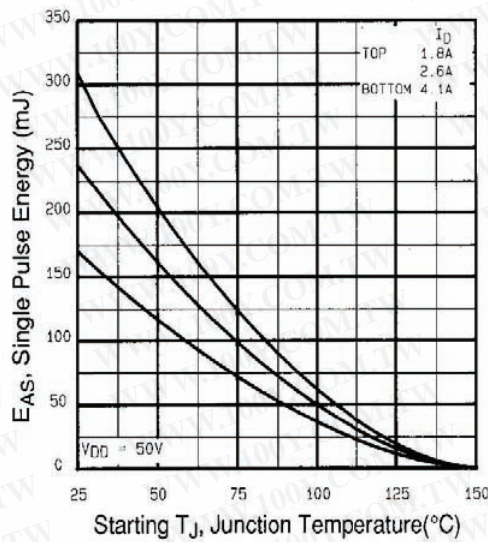


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

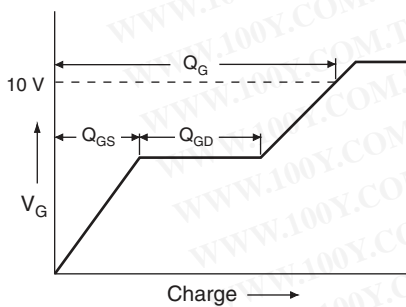


Fig. 13a - Basic Gate Charge Waveform

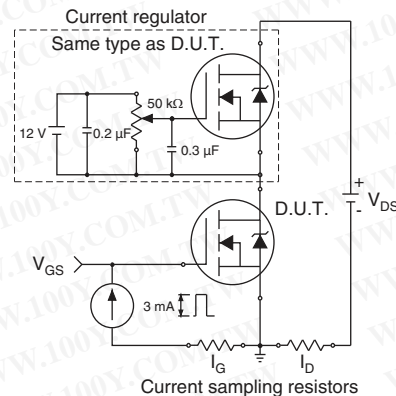
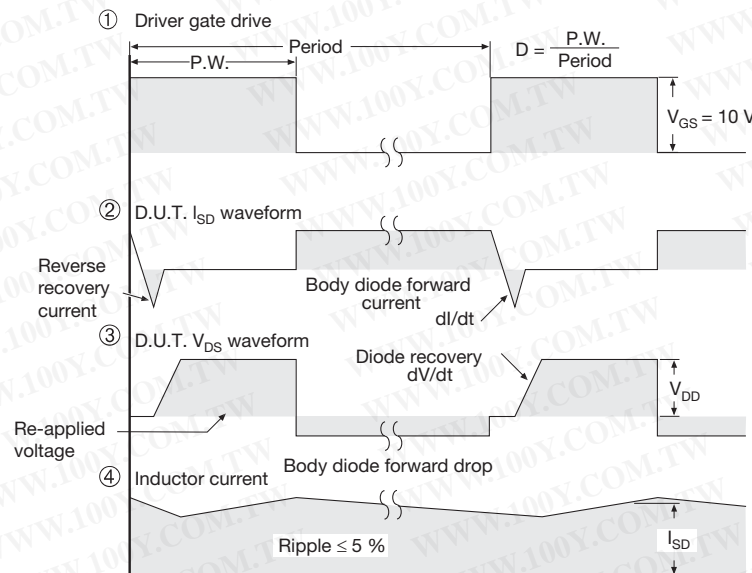
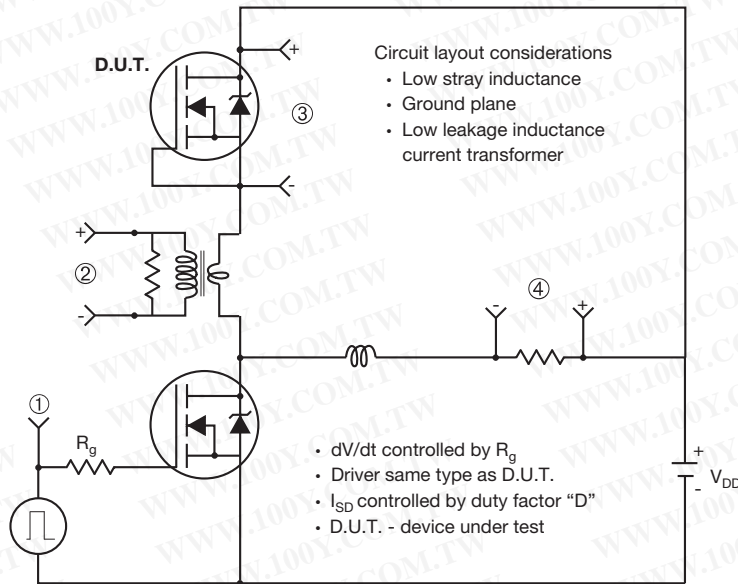


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

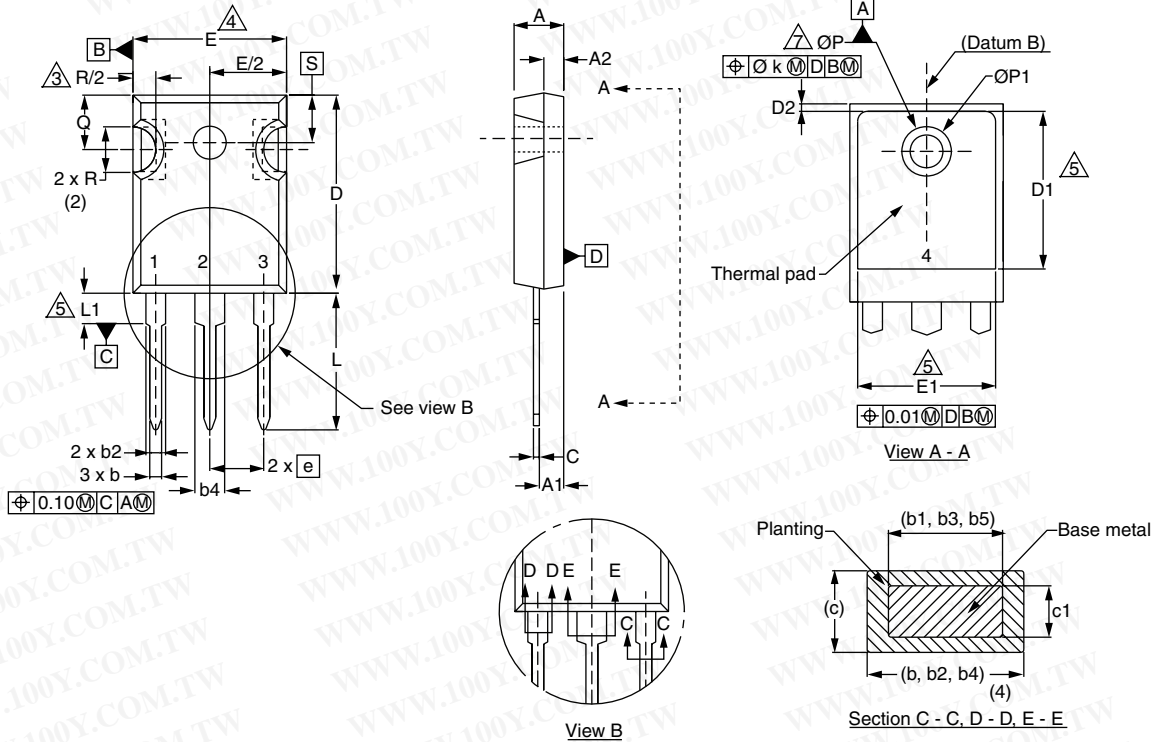
a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-247AC (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.65	5.31	0.183	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.65	2.39	0.065	0.094
b3	1.65	2.37	0.065	0.093
b4	2.59	3.43	0.102	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.70	0.776	0.815
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
ϕk	0.254		0.010	
L	14.20	16.10	0.559	0.634
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ϕP	3.56	3.66	0.140	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: S-81920-Rev. A, 15-Sep-08
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. ϕP to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.



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