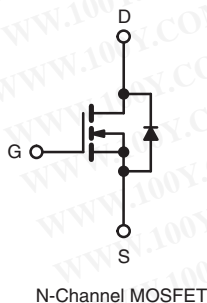
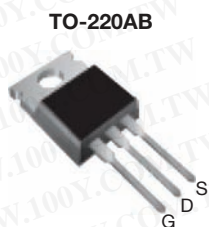


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	200 V	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5$ V	0.40
Q_g (Max.) (nC)	40	
Q_{gs} (nC)	5.5	
Q_{gd} (nC)	24	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4$ V and 5 V
- 150 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRL630PbF SiHL630-E3
SnPb	IRL630 SiHL630

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current ^a	I_{DM}	36	
Linear Derating Factor		0.59	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	250	mJ
Repetitive Avalanche Current ^a	I_{AR}	9.0	A
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ
Maximum Power Dissipation	P_D	74	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 4.6$ mH, $R_g = 25$ Ω , $I_{AS} = 9.0$ A (see fig. 12).
- $I_{SD} \leq 9.0$ A, $dV/dt \leq 120$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

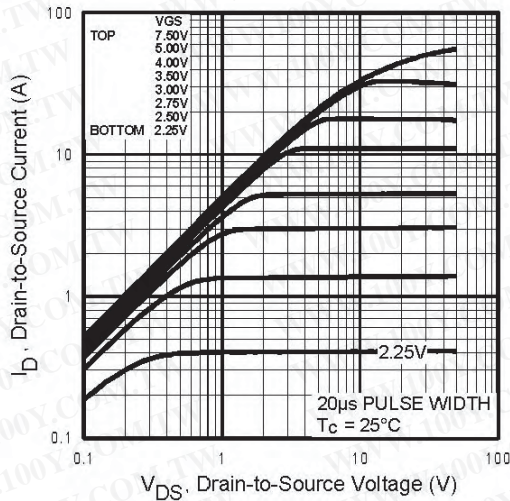
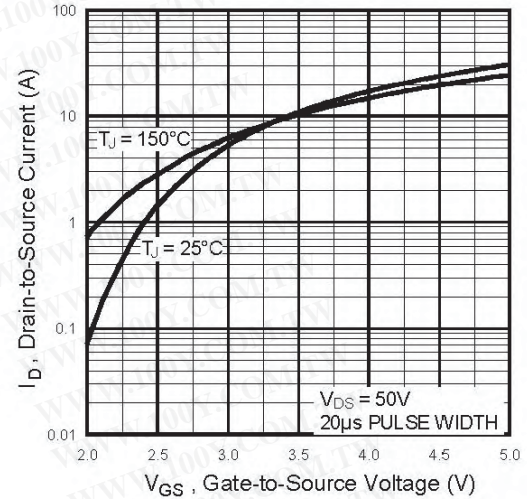
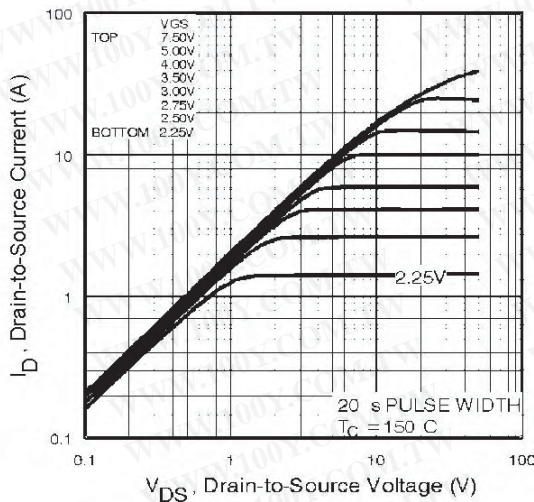
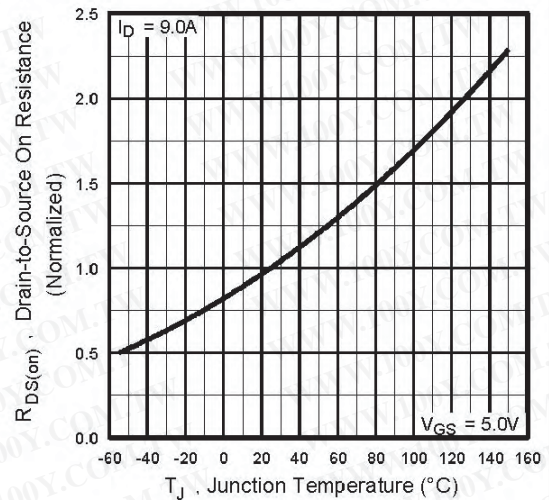
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$		-	0.27	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 160\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 5.4\text{ A}^b$	-	-	0.40	Ω
		$V_{GS} = 4.0\text{ V}$	$I_D = 4.5\text{ A}^b$	-	-	0.50	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 5.4\text{ A}^b$		4.8	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5		-	1100	-	pF
Output Capacitance	C_{oss}			-	220	-	
Reverse Transfer Capacitance	C_{rss}			-	70	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 9.0\text{ A}$, $V_{DS} = 160\text{ V}$, see fig. 6 and 13 ^b	-	-	40	nC
Gate-Source Charge	Q_{gs}			-	-	5.5	
Gate-Drain Charge	Q_{gd}			-	-	24	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$, $I_D = 9.0\text{ A}$ $R_g = 6.0\text{ }\Omega$, $R_D = 11\text{ }\Omega$, see fig. 10 ^b		-	8.0	-	ns
Rise Time	t_r			-	57	-	
Turn-Off Delay Time	$t_{d(off)}$			-	38	-	
Fall Time	t_f			-	33	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.0	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	36	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 9.0\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 9.0\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	230	350	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.7	2.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

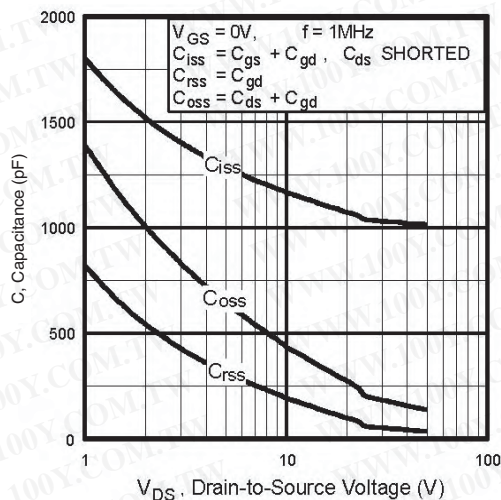


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

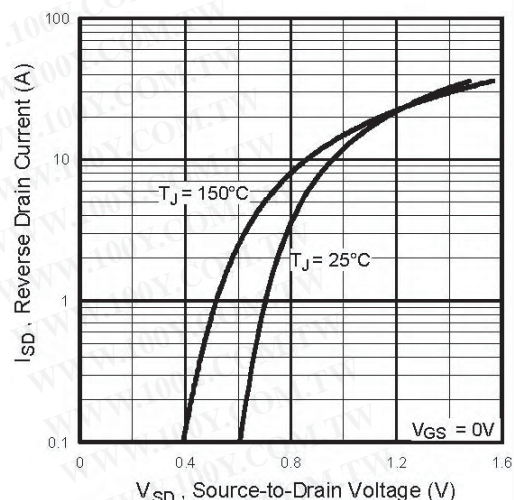


Fig. 7 - Typical Source-Drain Diode Forward Voltage

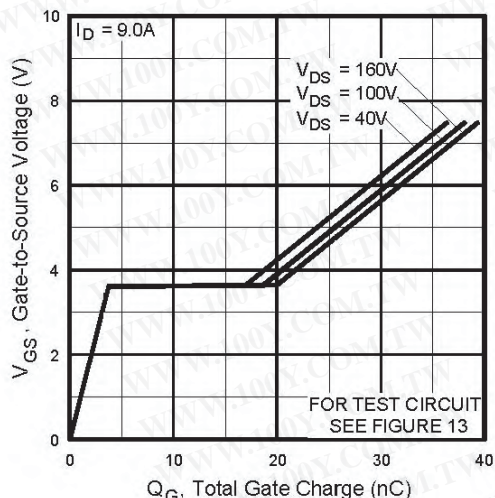


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

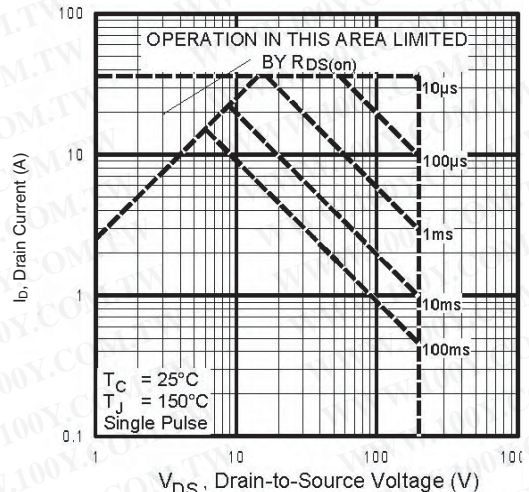
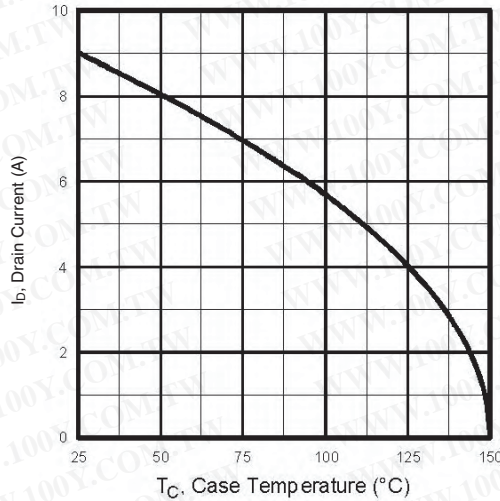
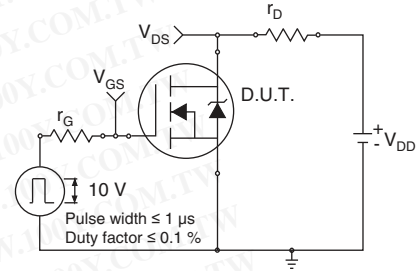
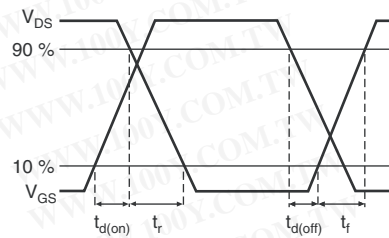
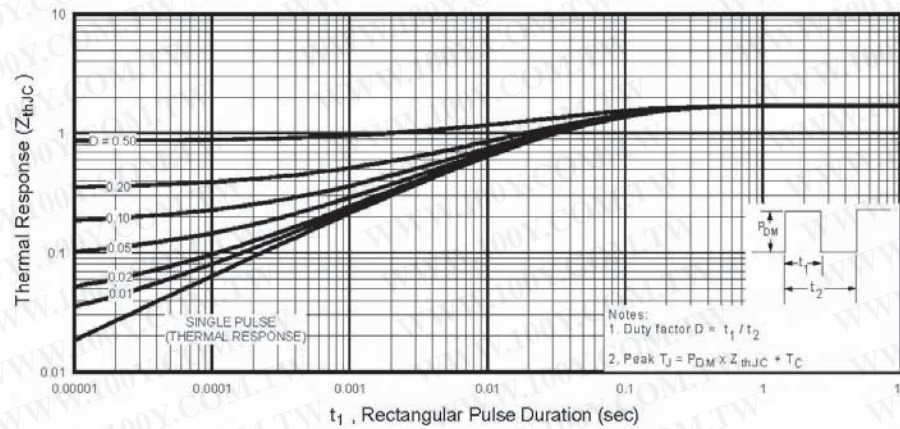


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

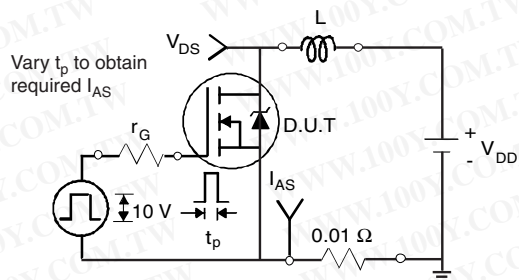


Fig. 12a - Unclamped Inductive Test Circuit

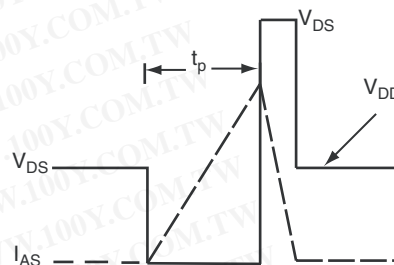


Fig. 12b - Unclamped Inductive Waveforms

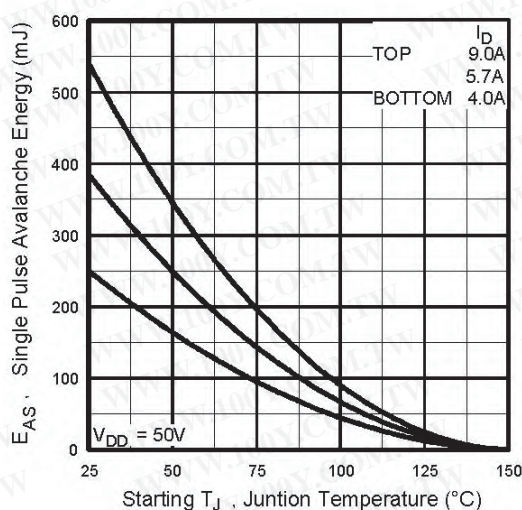


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

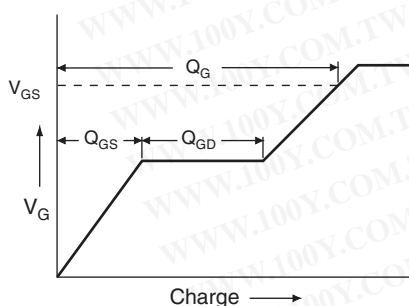


Fig. 13a - Basic Gate Charge Waveform

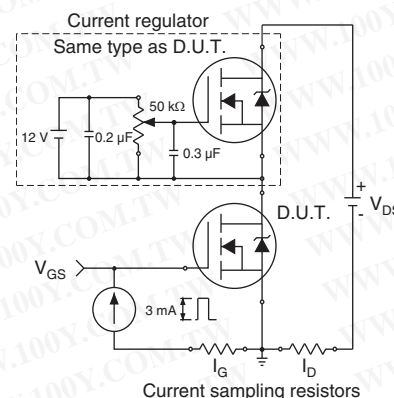
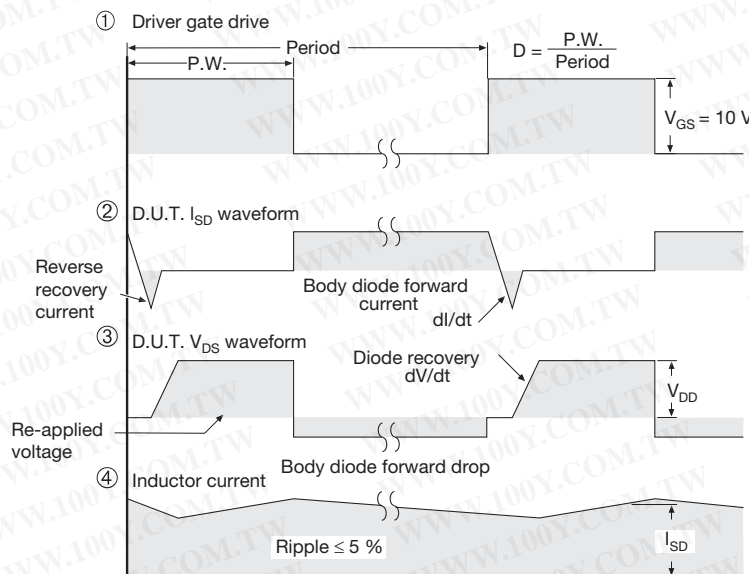
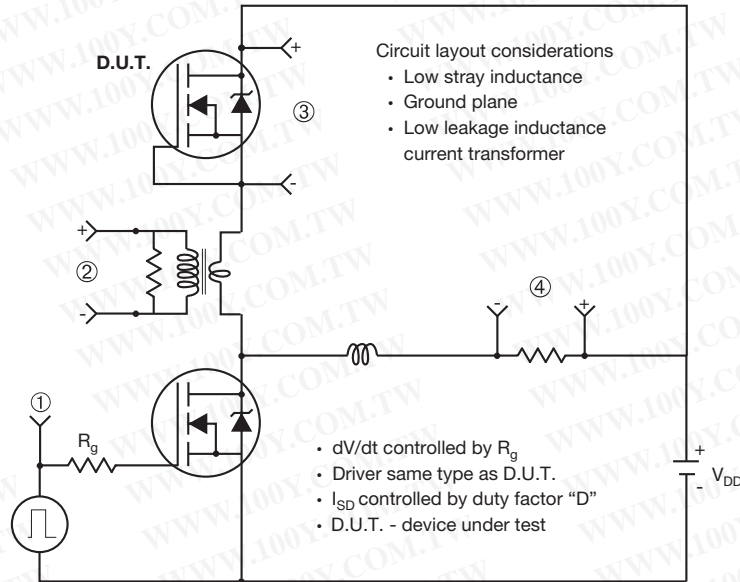


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

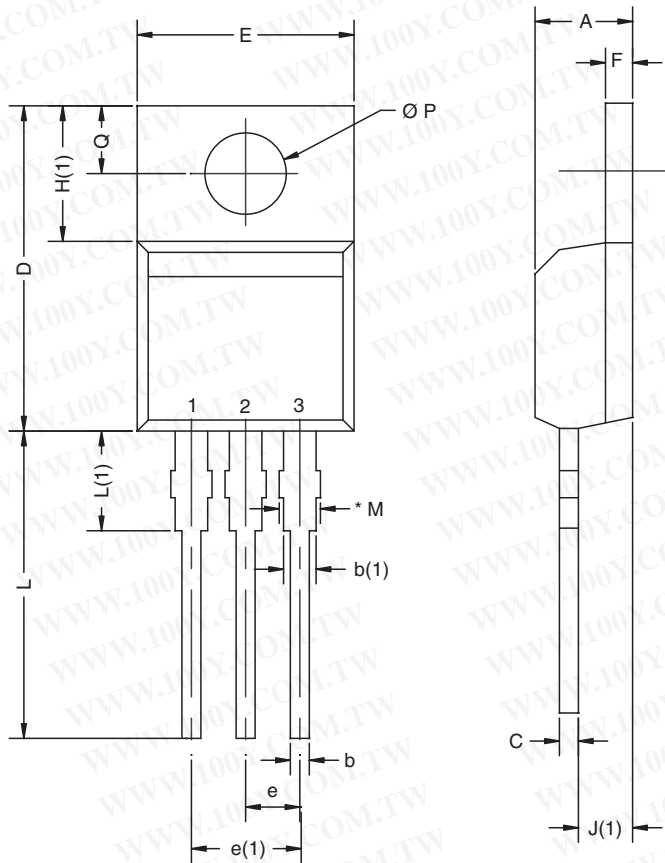
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X10-0416-Rev. M, 01-Nov-10
DWG: 5471

Note

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM



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