



N- and P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
N-Channel	30	0.065 at V _{GS} = 10 V	4 ^a	2 nC
		0.100 at V _{GS} = 4.5 V	4 ^a	
P-Channel	-30	0.140 at V _{GS} = -10 V	-3.7	2.2 nC
		0.235 at V _{GS} = -4.5 V	-2.8	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC

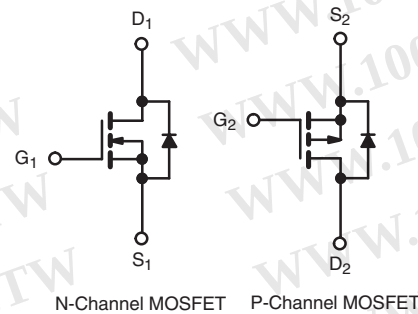
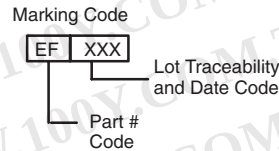
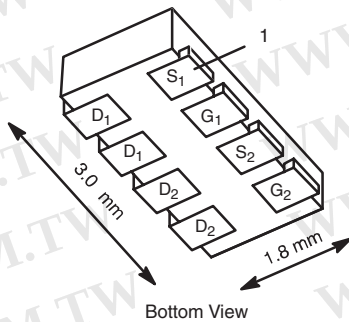


RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- DC/DC for Portable Applications
- Load Switch

1206-8 ChipFET[®] Dual



Ordering Information: Si5504BDC-T1-E3 (Lead (Pb)-free)
 Si5504BDC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	30	- 30	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	4 ^a	- 3.7	A
	T _C = 85 °C		3.8	- 2.7	
	T _A = 25 °C		3.7 ^{b, c}	- 2.5 ^{b, c}	
	T _A = 85 °C		2.6 ^{b, c}	- 1.8 ^{b, c}	
Pulsed Drain Current		I _{DM}	10	- 10	W
Source Drain Current Diode Current	T _C = 25 °C	I _S	2.5	- 2.5	
	T _A = 25 °C		1.3 ^{b, c}	- 1.3 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	3.12	3.1	W
	T _C = 85 °C		2	2	
	T _A = 25 °C		1.5 ^{b, c}	1.5 ^{b, c}	
	T _A = 85 °C		0.8 ^{b, c}	0.8 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	70	85	70	85	°C/W
Maximum Junction-to-Foot (Drain)	R _{thJF}	33	40	33	40	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 120 °C/W.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	30		V	
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 30			
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	27		mV/°C	
		I _D = - 250 μA	P-Ch		- 30		
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	- 5			
		I _D = - 250 μA	P-Ch		3.5		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.5		V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 1.5			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch		100	nA	
			P-Ch		- 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = - 30 V, V _{GS} = 0 V	P-Ch		- 1		
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch		5		
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch		- 5		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	10		A	
		V _{DS} ≤ - 5 V, V _{GS} = - 10 V	P-Ch	- 10			
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 3.1 A	N-Ch		0.053	0.065	Ω
		V _{GS} = - 10 V, I _D = - 2.1 A	P-Ch		0.112	0.140	
		V _{GS} = 4.5 V, I _D = 1 A	N-Ch		0.081	0.100	
		V _{GS} = - 4.5 V, I _D = - 0.43 A	P-Ch		0.188	0.235	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.1 A	N-Ch		5	S	
		V _{DS} = - 15 V, I _D = - 2.1 A	P-Ch		3.5		
Dynamic ^a							
Input Capacitance	C _{iss}	N-Channel V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		220	pF	
			P-Ch		170		
Output Capacitance	C _{oss}	P-Channel V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		50		
			P-Ch		50		
Reverse Transfer Capacitance	C _{rss}		N-Ch		25		
			P-Ch		31		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 3.6 A	N-Ch		4.5	7	nC
		V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 2.5 A	P-Ch		4.5	7	
Gate-Source Charge	Q _{gs}	N-Channel V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 3.6 A	N-Ch		2	3	
			P-Ch		2.2	3.5	
Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 2.5 A	N-Ch		0.7		
			P-Ch		0.7		
Gate Resistance	R _g	f = 1 MHz	N-Ch		3	Ω	
			P-Ch		13		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

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SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Dynamic ^a								
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}$, $R_L = 5.8\text{ }\Omega$ $I_D \cong 2.6\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		15	25	ns	
			P-Ch		30	45		
Rise Time	t_r		N-Ch		80	120		
			P-Ch		60	90		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -15\text{ V}$, $R_L = 7.5\text{ }\Omega$ $I_D \cong -2\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		12	20		
			P-Ch		10	15		
Fall Time	t_f		N-Ch		25	40		
			P-Ch		10	15		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}$, $R_L = 5.8\text{ }\Omega$ $I_D \cong 2.6\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		4	8		
			P-Ch		4	8		
Rise Time	t_r		N-Ch		12	20		
			P-Ch		10	15		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -15\text{ V}$, $R_L = 7.5\text{ }\Omega$ $I_D \cong -2\text{ A}$, $V_{GEN} = -10\text{ V}$, $R_g = 1\text{ }\Omega$	N-Ch		10	15		
			P-Ch		10	15		
Fall Time	t_f		N-Ch		5	10		
			P-Ch		5	10		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			2.5	A	
			P-Ch			- 2.5		
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			10		
			P-Ch			- 10		
Body Diode Voltage	V_{SD}	$I_S = 2.6\text{ A}$, $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V	
		$I_S = -2\text{ A}$, $V_{GS} = 0\text{ V}$	P-Ch		- 0.8	- 1.2		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 2.6\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		30	50	ns	
			P-Ch		20	40		
Body Diode Reverse Recovery Charge	Q_{rr}		N-Channel	N-Ch		20	40	nC
				P-Ch		10	20	
Reverse Recovery Fall Time	t_a		P-Channel	N-Ch		23		ns
				P-Ch		13		
Reverse Recovery Rise Time	t_b		N-Ch		7			
			P-Ch		7			

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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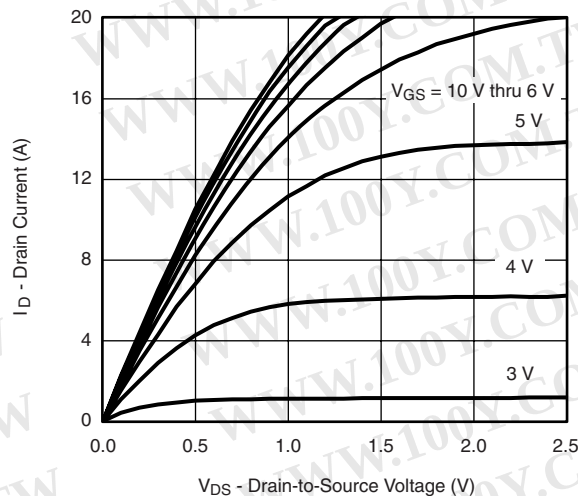
Si5504BDC

Vishay Siliconix

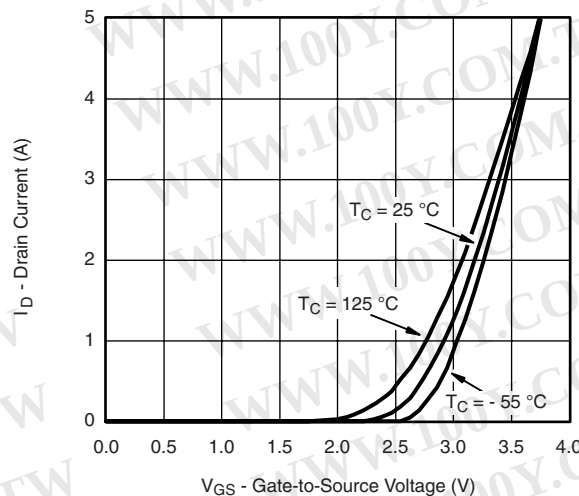
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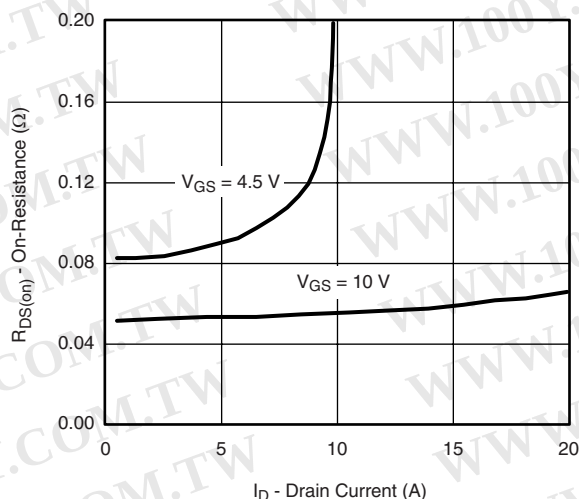
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



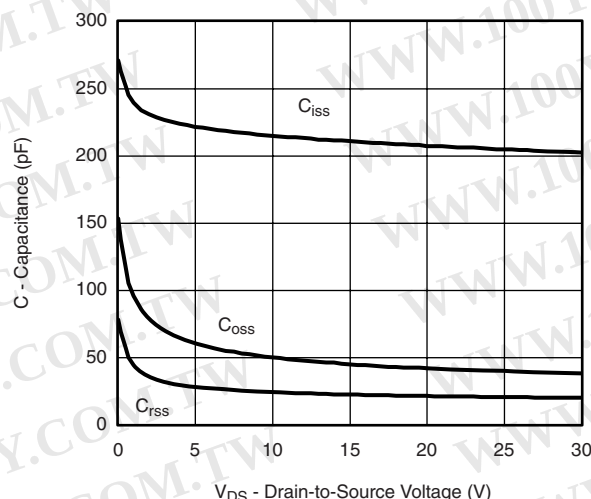
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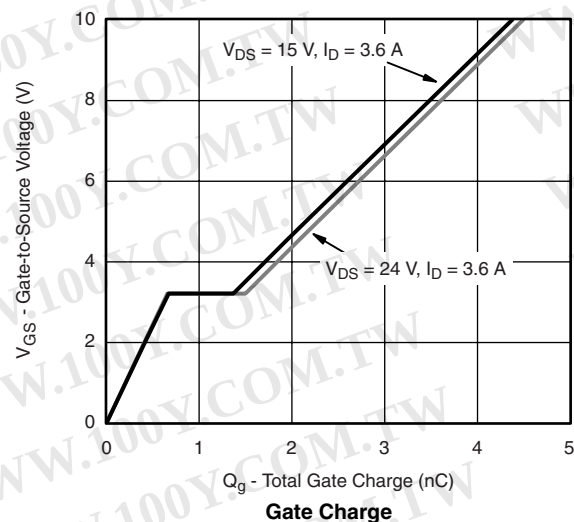
Transfer Characteristics



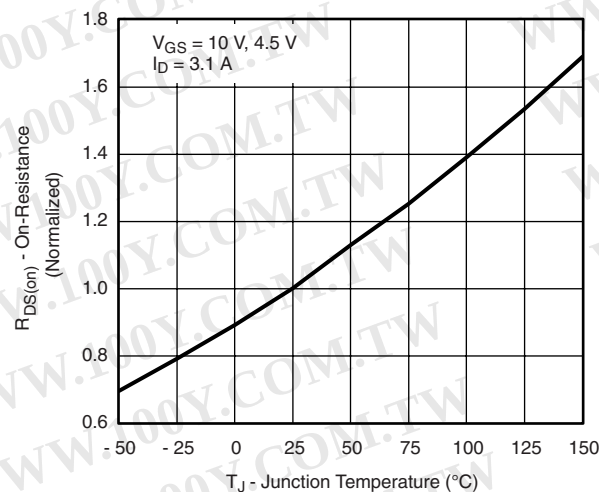
On-Resistance vs. Drain Current



Capacitance



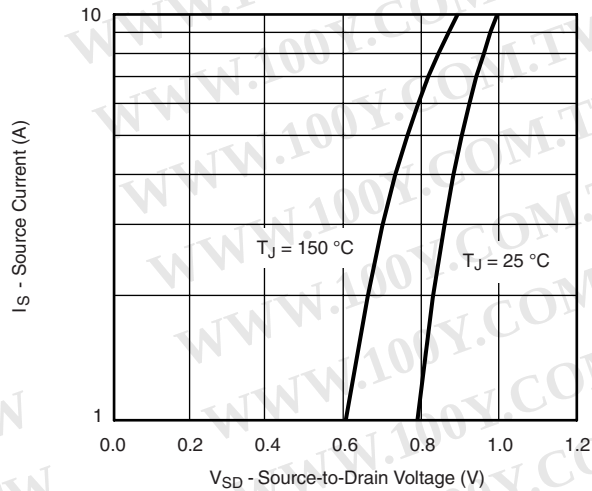
Gate Charge



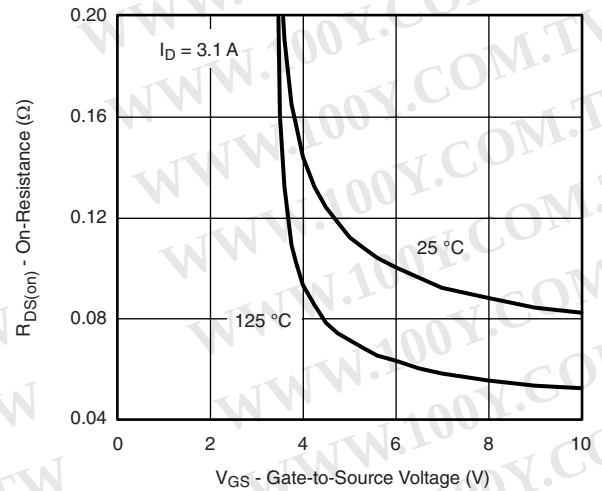
On-Resistance vs. Junction Temperature



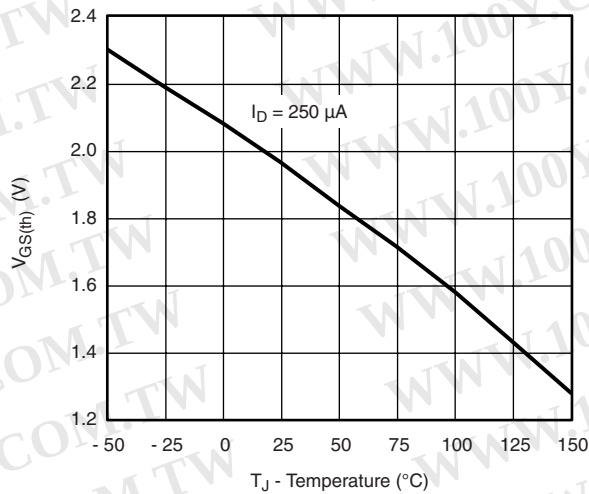
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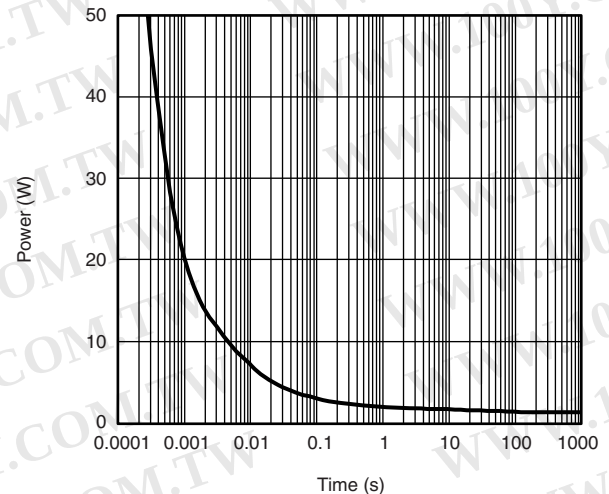
Source-Drain Diode Forward Voltage



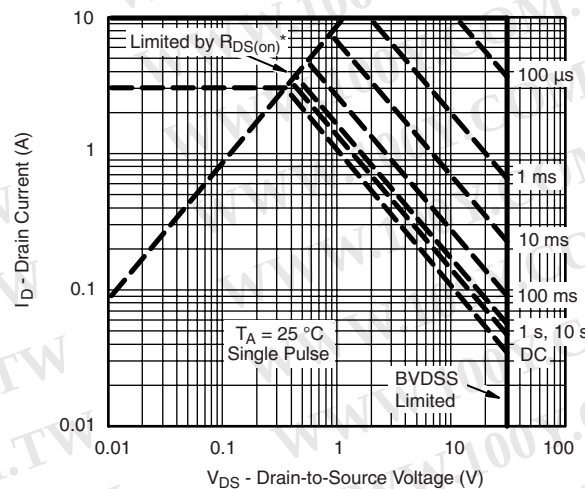
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



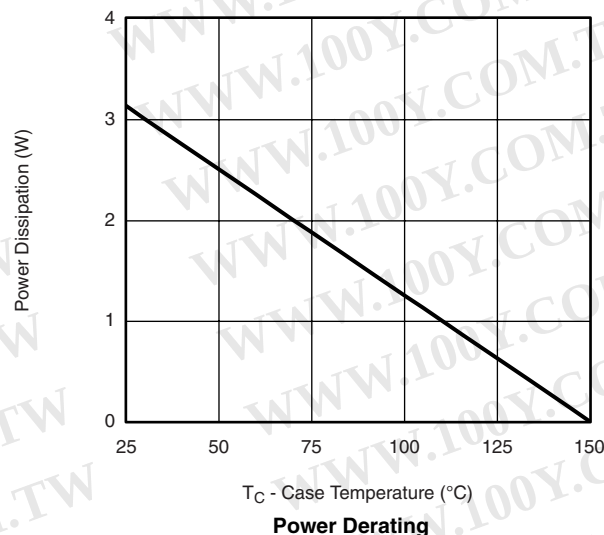
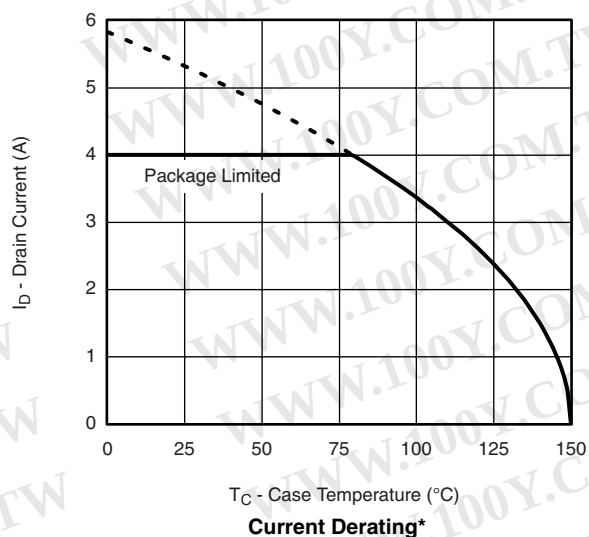
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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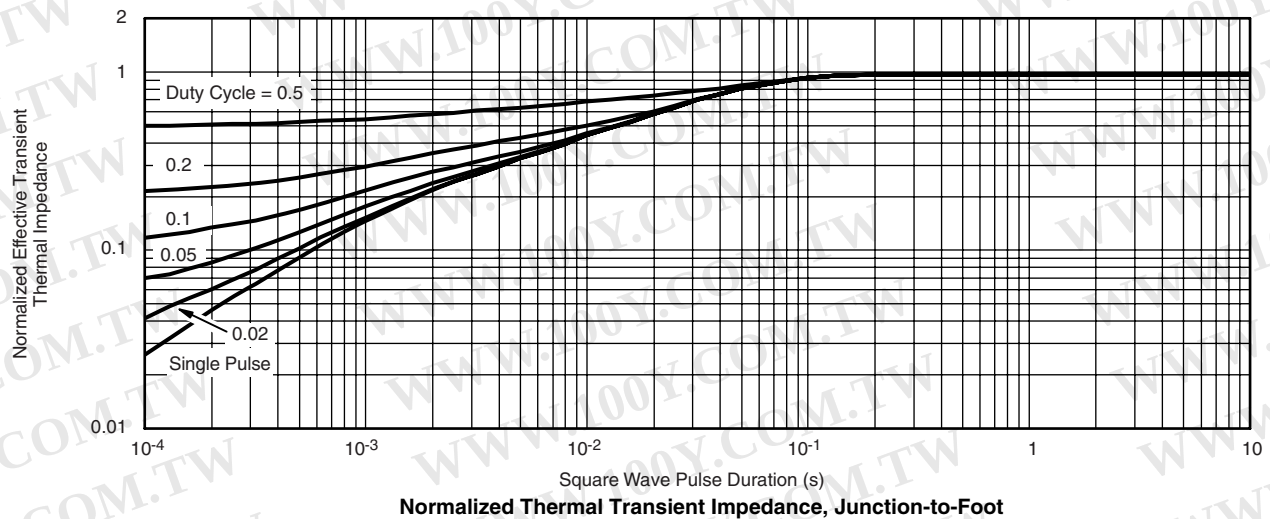
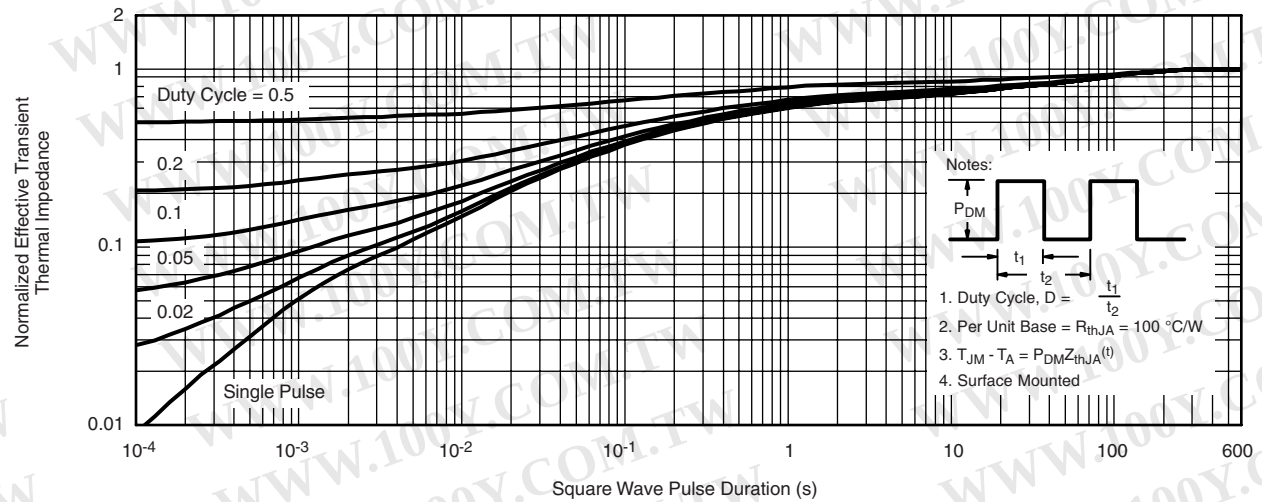
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* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

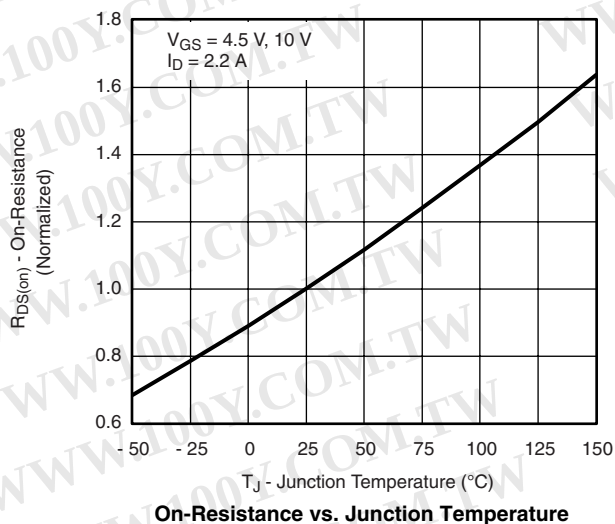
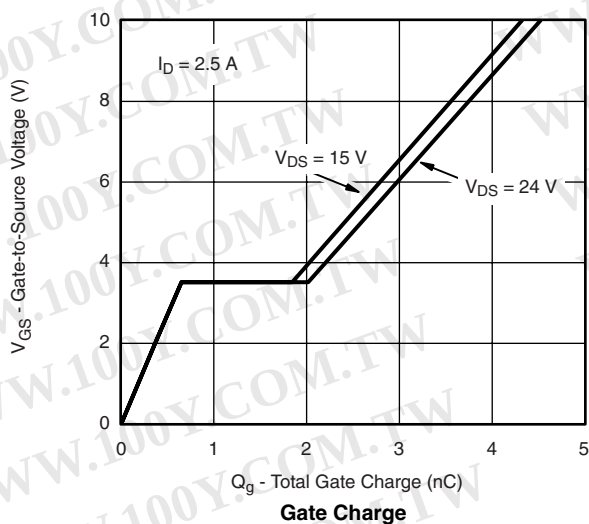
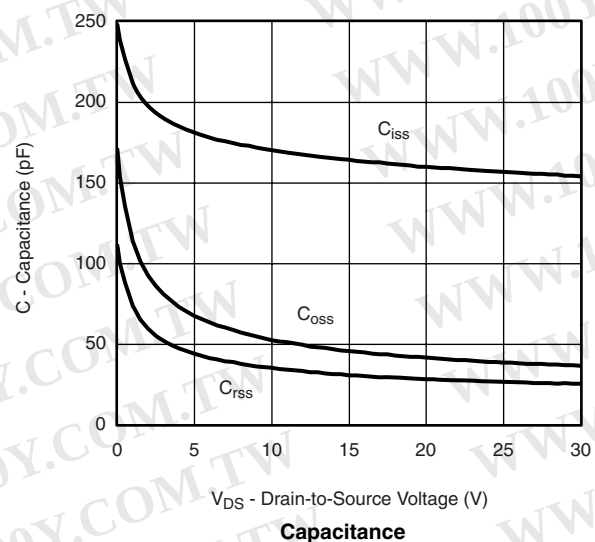
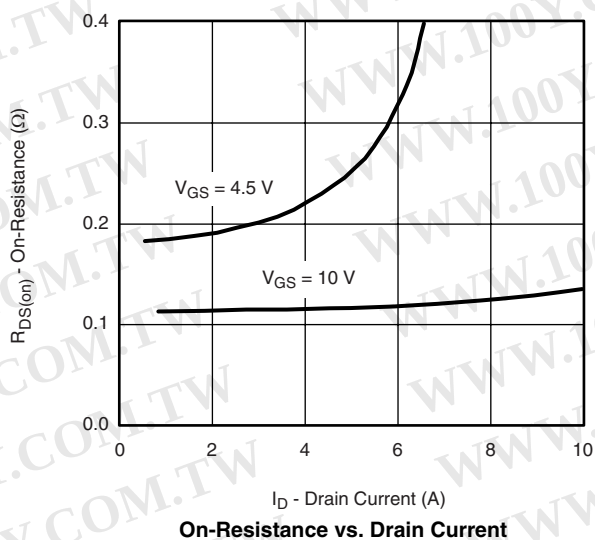
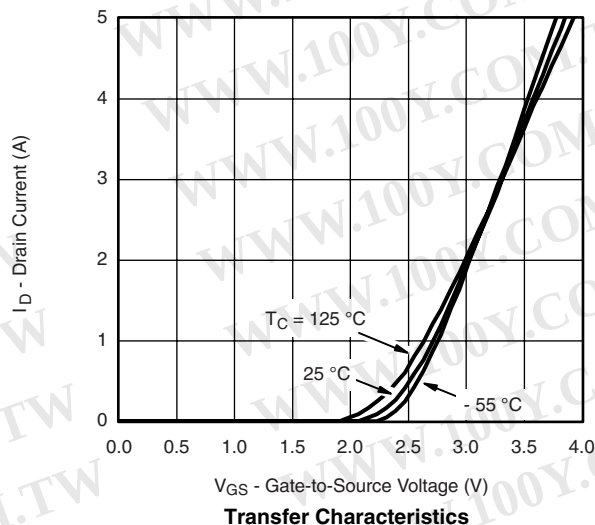
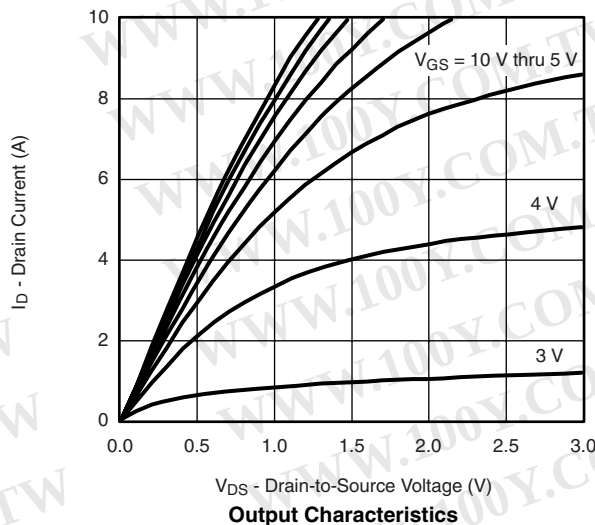
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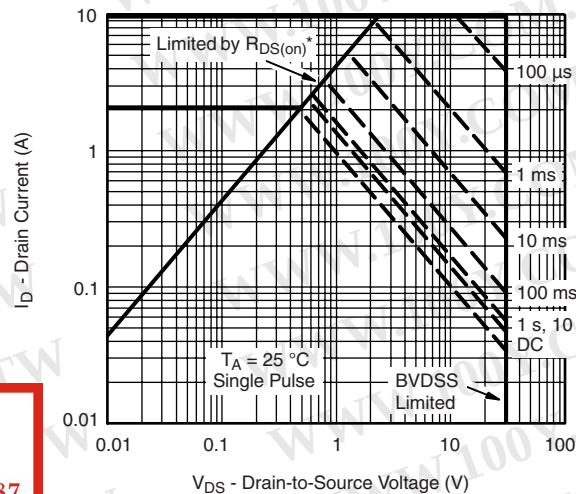
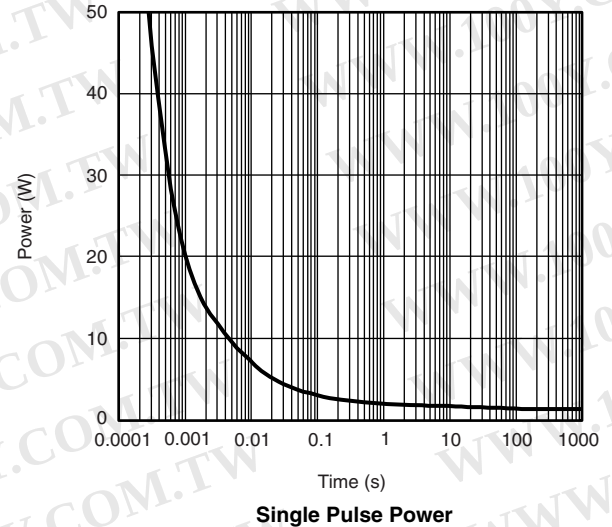
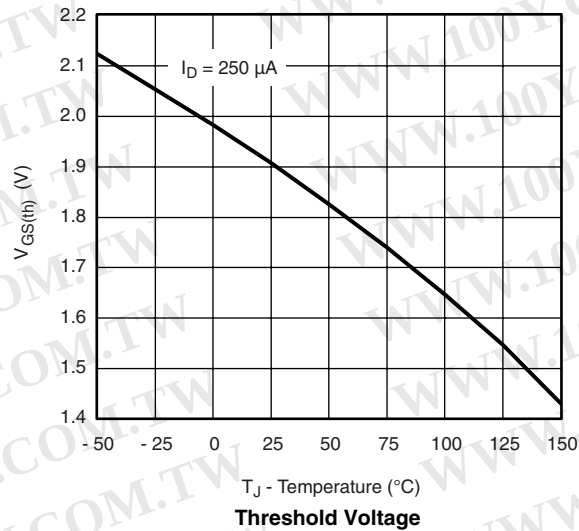
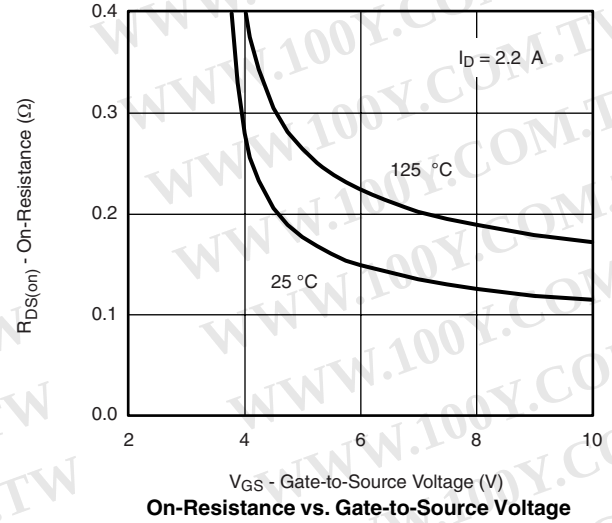
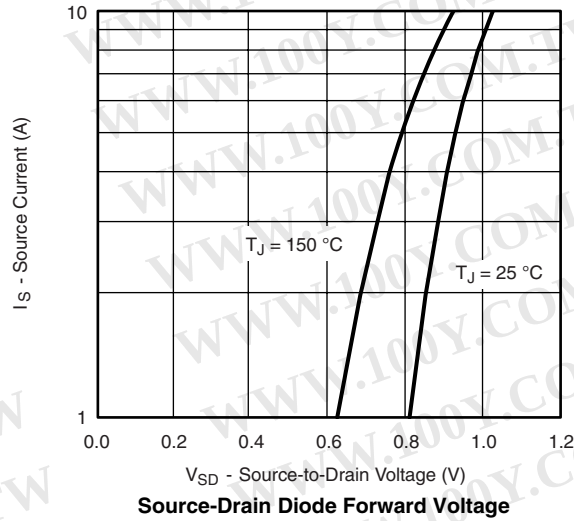


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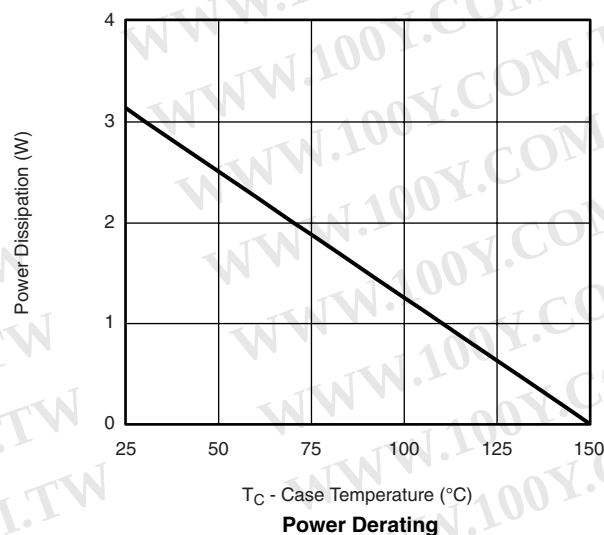
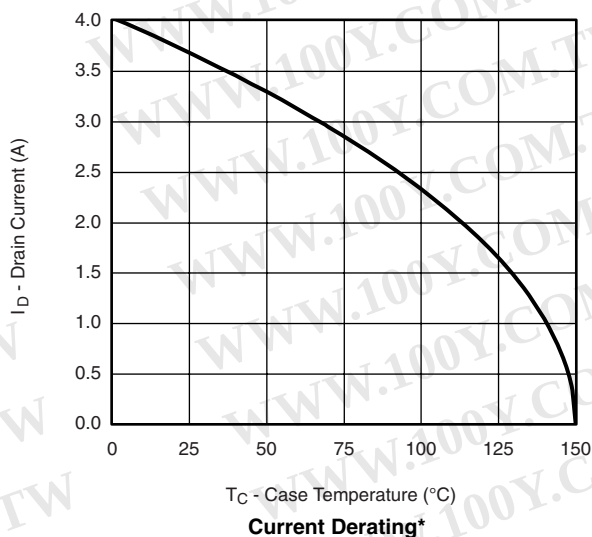
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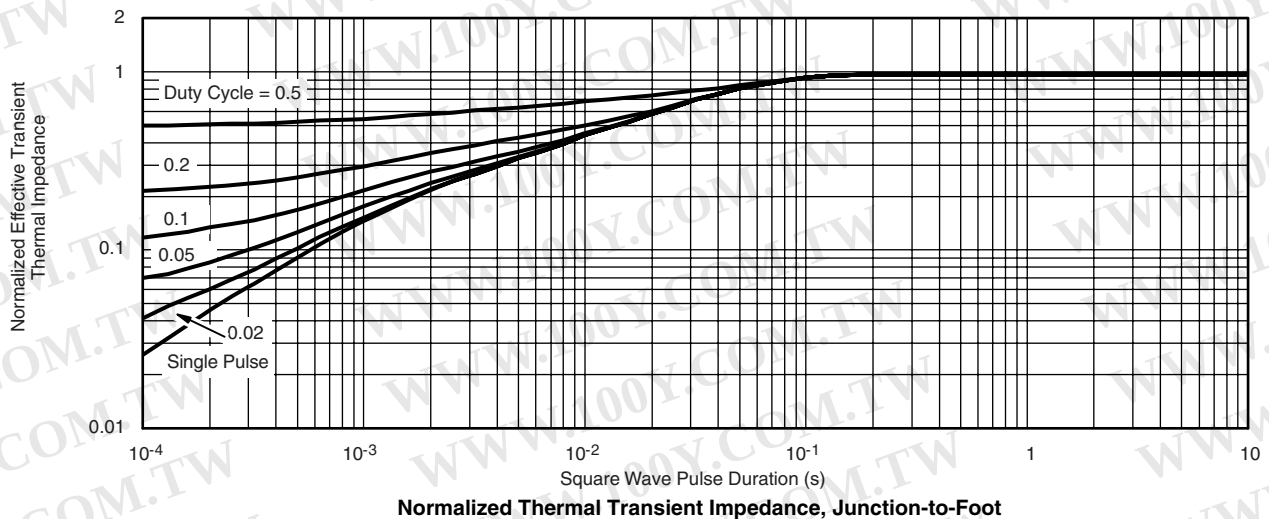
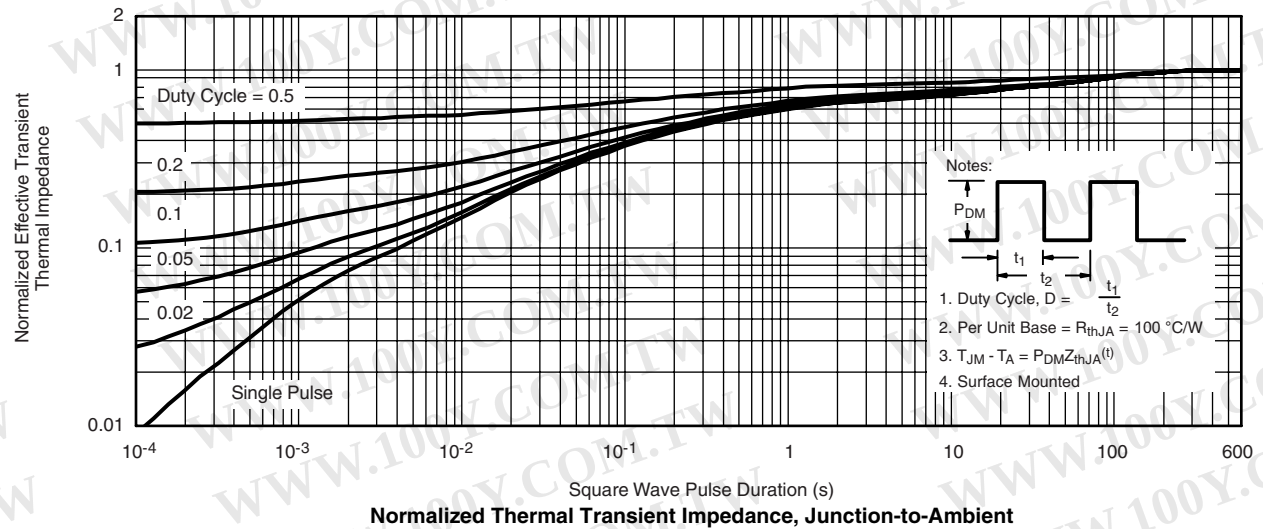
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