Dual N-Channel 1.5 V (G-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
8	0.032 at V_{GS} = 4.5 V	4[a]	7.3 nC
	0.036 at V_{GS} = 2.5 V	4[a]	
	0.045 at V_{GS} = 1.8 V	4[a]	
	0.054 at V_{GS} = 1.5 V	4[a]	

FEATURES

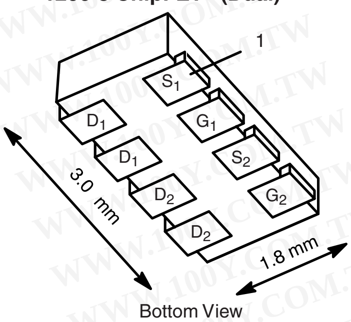
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET: 1.5 V Rated
- Ultra Low On-Resistance in Compact, Thermally Enhanced ChipFET® Package
- Compliant to RoHS Directive 2002/95/EC

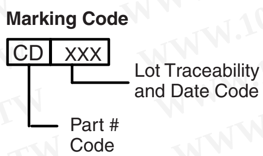
Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

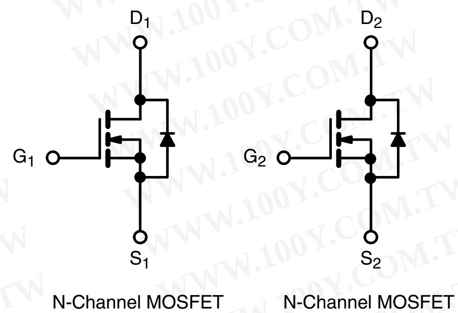
APPLICATIONS

- Load Switch for Portable Applications
  - Guaranteed Operation at V_{GS} = 1.5 V Critical for Optimized Design and Space Savings

1206-8 ChipFET® (Dual)







Ordering Information: Si5920DC-T1-E3 (Lead (Pb)-free)
Si5920DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	8	V
Gate-Source Voltage		V_{GS}	± 5	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	4[a]	A
	T_C = 70 °C		4[a]	
	T_A = 25 °C		4[a]	
	T_A = 70 °C		4[a]	
Pulsed Drain Current		I_{DM}	25	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	2.6	
	T_A = 25 °C		1.7[c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	3.12	W
	T_C = 70 °C		2.0	
	T_A = 25 °C		2.04[b, c]	
	T_A = 70 °C		1.3[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	50	60	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

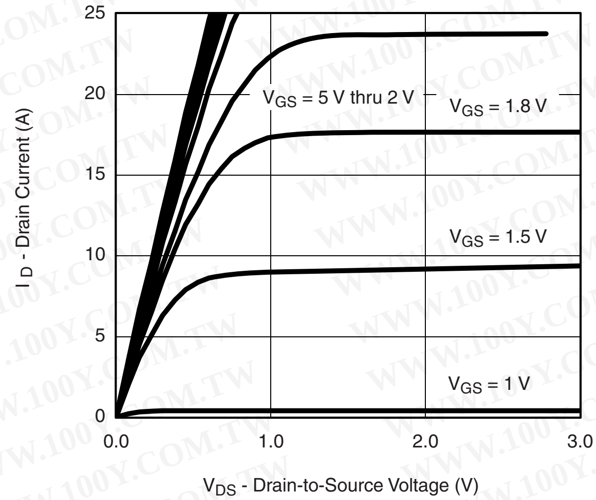
Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See Solder Profile (www.vishay.com/ppg?73257). The 1206-8 ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 90 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	8			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		8.2		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	0.3		1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 5 V			± 100	ns
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 8 V, V_{GS} = 0 V			1	µA
		V_{DS} = 8 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ 5 V, V_{GS} = 4.5 V	25			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6.8 A		0.025	0.032	Ω
		V_{GS} = 2.5 V, I_D = 6.3 A		0.0285	0.036	
		V_{GS} = 1.8 V, I_D = 2.5 A		0.036	0.045	
		V_{GS} = 1.5 V, I_D = 1.8 A		0.041	0.054	
Forward Transconductance[a]	g_{fs}	V_{DS} = 4 V, I_D = 6.8 A		18		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 4 V, V_{GS} = 0 V, f = 1 MHz		680		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			140		
Total Gate Charge	Q_g	V_{DS} = 4 V, V_{GS} = 5 V, I_D = 6.8 A		8	12	nC
		V_{DS} = 4 V, V_{GS} = 4.5 V, I_D = 6.8 A		7.3	11	
Gate-Source Charge	Q_{gs}			0.84		
Gate-Drain Charge	Q_{gd}			1.26		
Gate Resistance	R_g	f = 1 MHz		1.8	2.7	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 4 V, R_L = 0.73 Ω $I_D \cong$ 5.5 A, V_{GEN} = 4.5 V, R_g = 1 Ω		8	12	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			7	11	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			2.6	A
Pulse Diode Forward Current	I_{SM}				25	
Body Diode Voltage	V_{SD}	I_S = 2.6 A, V_{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 2.6 A, dI/dt = 100 A/µs, T_J = 25 °C		12	18	ns
Body Diode Reverse Recovery Charge	Q_{rr}			3	5	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			5		

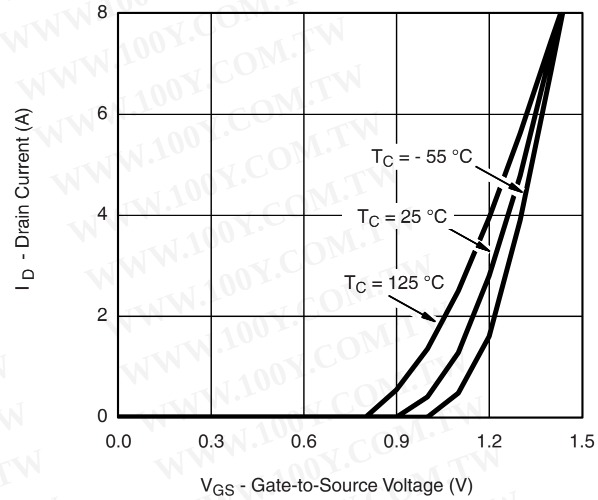
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

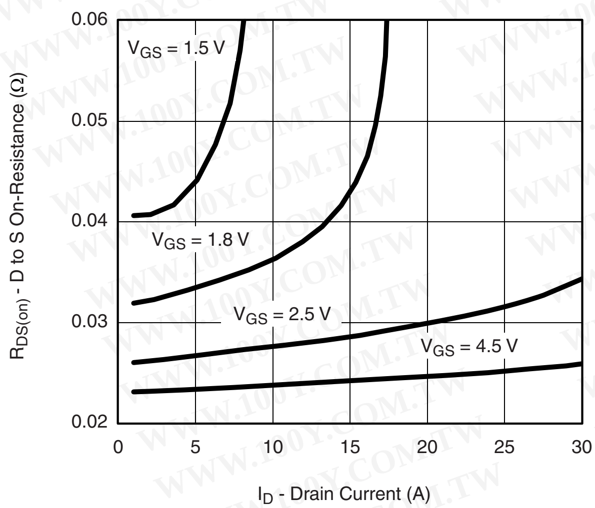
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



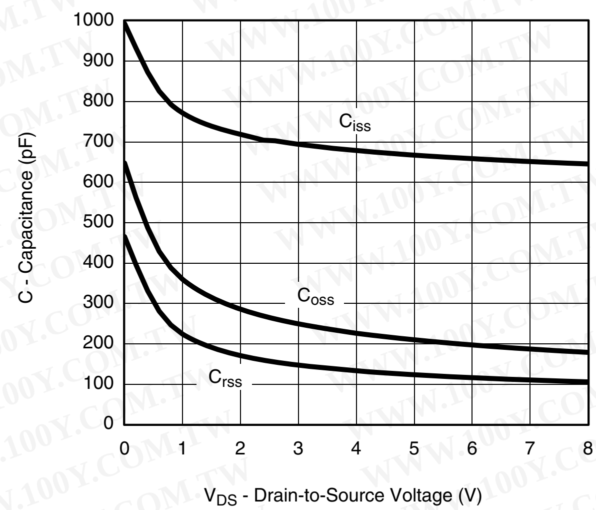
Output Characteristics



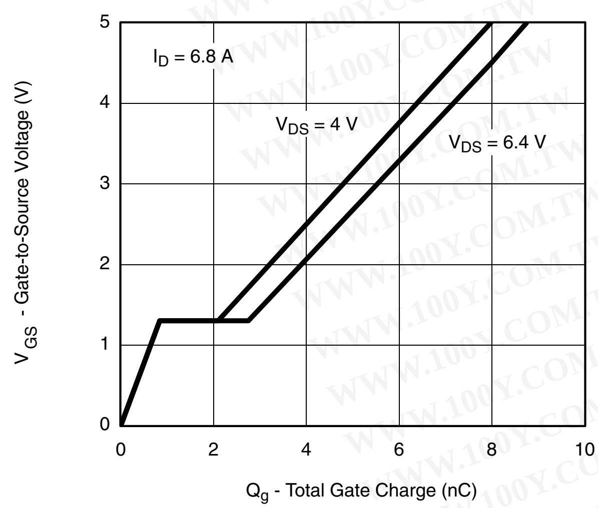
Transfer Characteristics



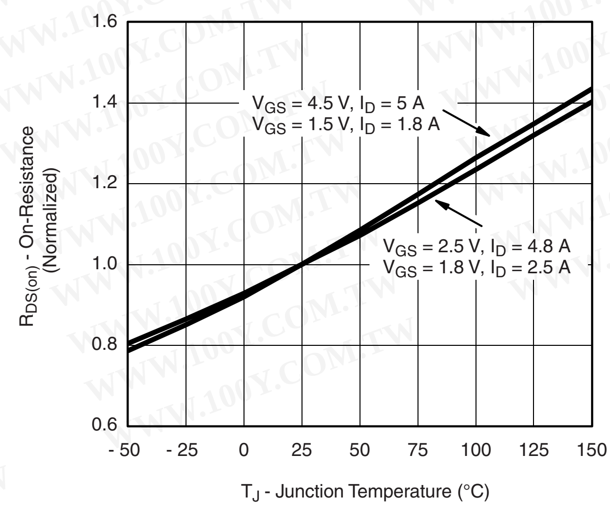
$R_{DS(on)}$ vs. Drain Current



Capacitance

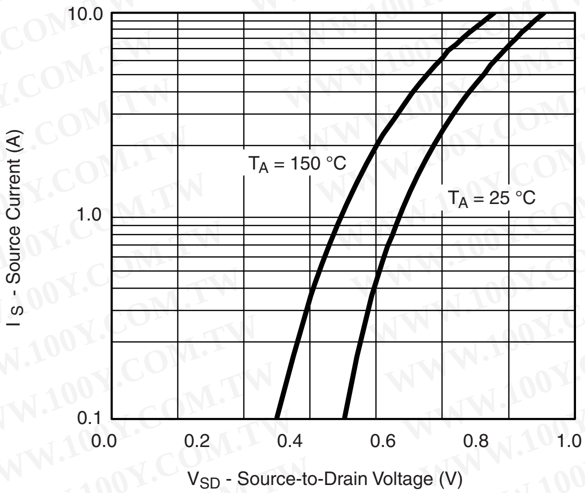


Gate Charge

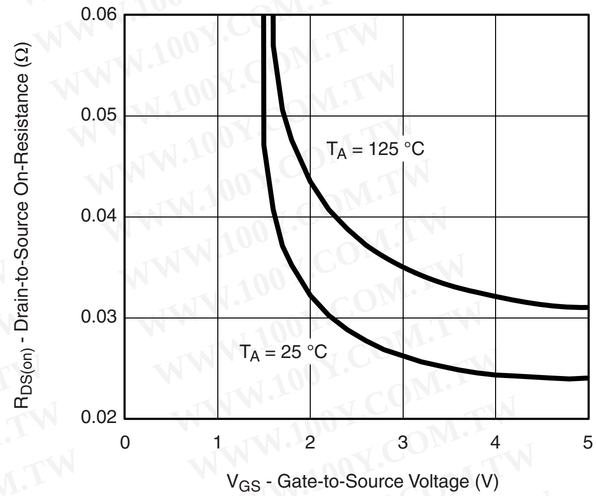


On-Resistance vs. Junction Temperature

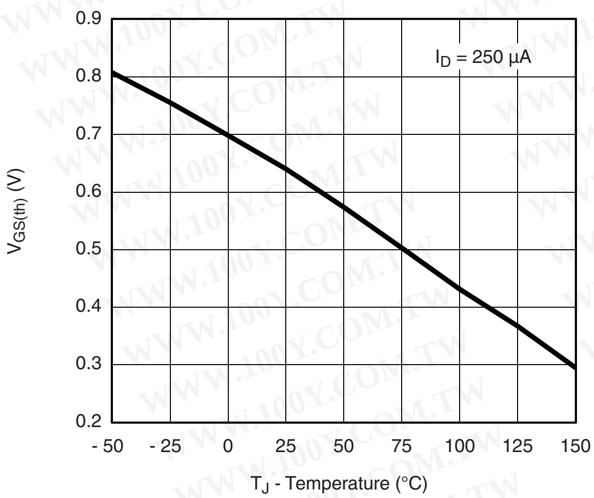
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



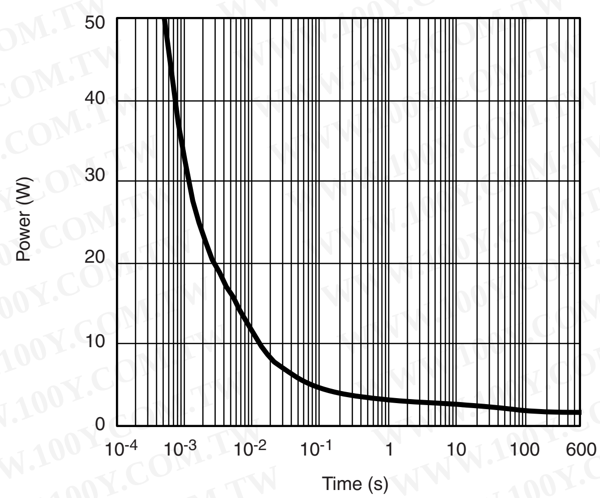
Forward Diode Voltage vs. Temperature



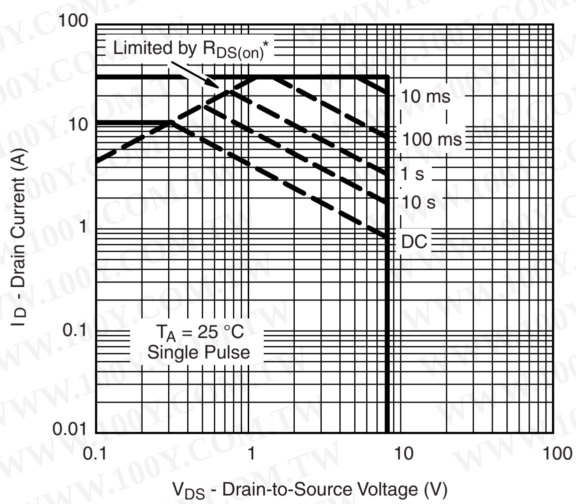
$R_{DS(on)}$ vs. V_{GS} vs. Temperature



Threshold Voltage



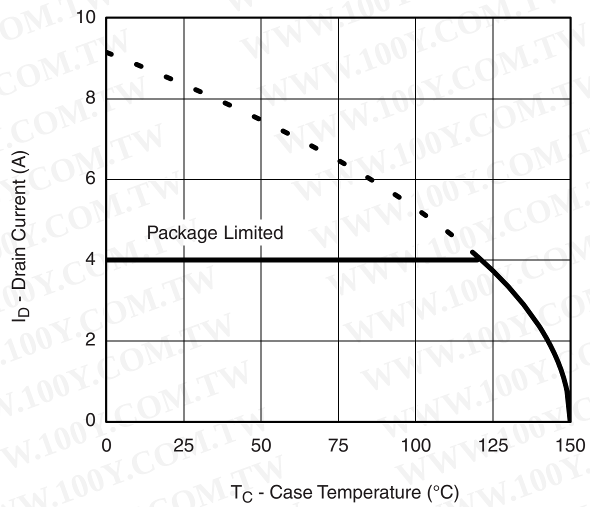
Single Pulse Power



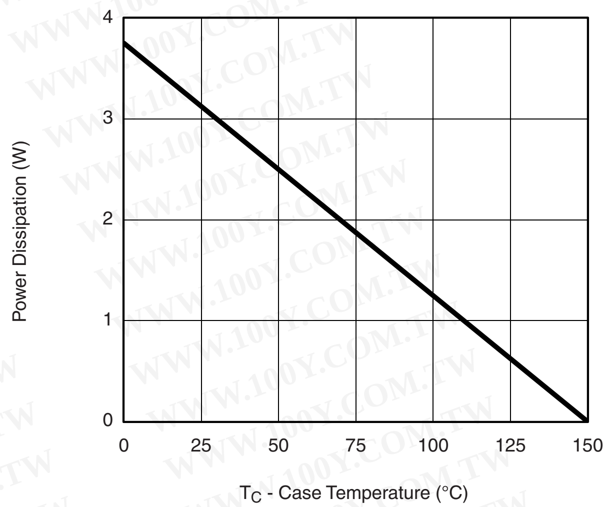
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



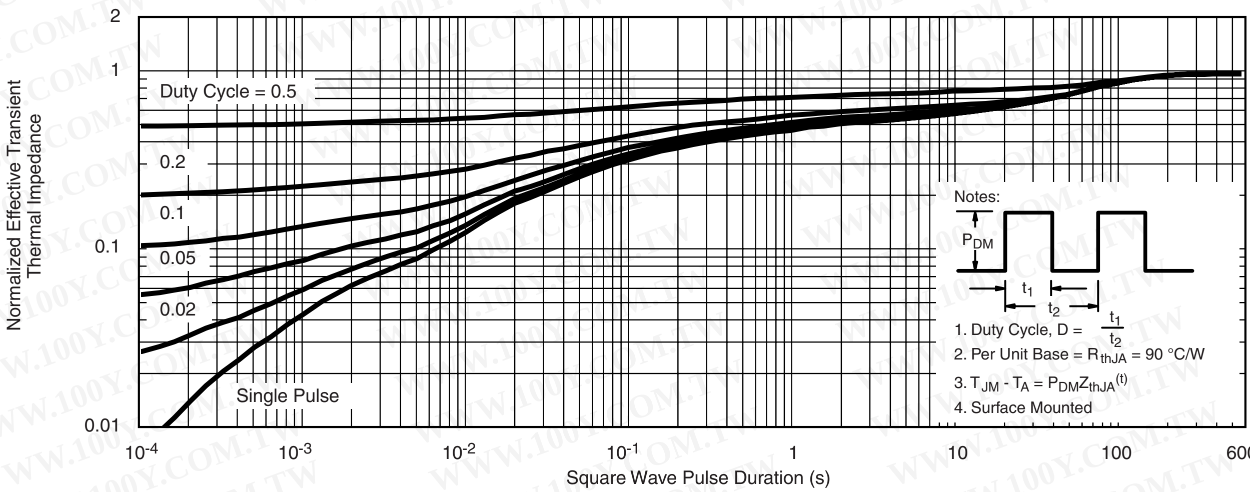
Current Derating*



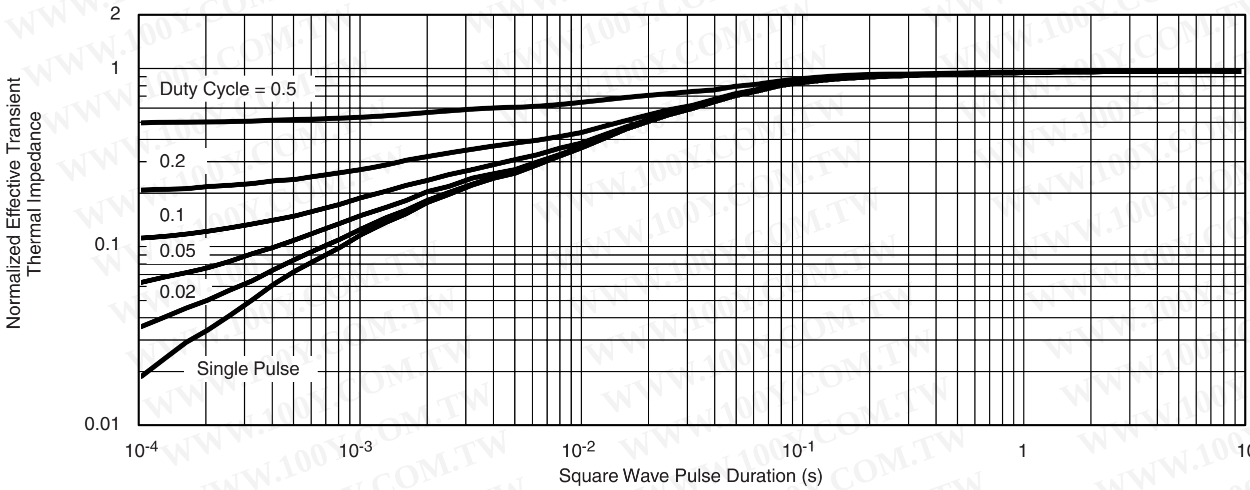
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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