



# N-Channel 55 V (D-S) 175 °C MOSFET

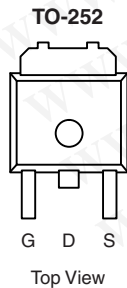
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>
55	0.020 at V <sub>GS</sub> = 10 V	35
	0.026 at V <sub>GS</sub> = 4.5 V	30

## FEATURES

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Rated Maximum Junction Temperature
- Low Input Capacitance

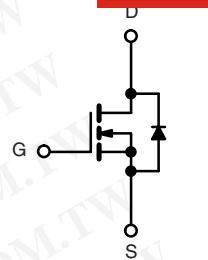


Available  
**RoHS\***  
COMPLIANT



Drain Connected to Tab

Ordering Information: SUD35N05-26L  
SUD35N05-26L (Lead (Pb)-free)



勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-34970699  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	55	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	35
		T <sub>C</sub> = 100 °C	25
Pulsed Drain Current	I <sub>DM</sub>	80	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	35	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	50 <sup>c</sup>
		T <sub>A</sub> = 25 °C	7.5 <sup>b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient <sup>b</sup>	R <sub>thJA</sub>	t ≤ 10 sec	17	20	°C/W
		Steady State	50	60	
Junction-to-Case	R <sub>thJC</sub>	2.5	3.0		
Junction-to-Lead	R <sub>thJL</sub>	5.0	6.0		

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x1" FR4 Board, t ≤ 10 sec.
- c. See SOA curve for voltage derating.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

## SUD35N05-26L



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<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	55			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 44\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 44\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 5\text{ V}$	35			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0165	0.020	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.035	
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		0.0215	0.026	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		25		S
<b>Dynamic<sup>a</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, F = 1\text{ MHz}$		885		$\mu\text{F}$
Output Capacitance	$C_{oss}$			185		
Reverse Transfer Capacitance	$C_{rss}$			80		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 25\text{ V}, V_{GS} = 5\text{ V}, I_D = 35\text{ A}$		10.5	13	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			4		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			4.8		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 25\text{ V}, R_L = 0.3\text{ }\Omega$ $I_D \cong 35\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		5	8	ns
Rise Time <sup>c</sup>	$t_r$			18	30	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			20	30	
Fall Time <sup>c</sup>	$t_f$			100	150	
<b>Source-Drain Diode Ratings and Characteristic</b> ( $T_C = 25\text{ }^\circ\text{C}$ )						
Continuous Current	$I_S$				35	A
Pulsed Current	$I_{SM}$				80	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 80\text{ A}, V_{GS} = 0\text{ V}$			1.5	V
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 35\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		25	40	ns

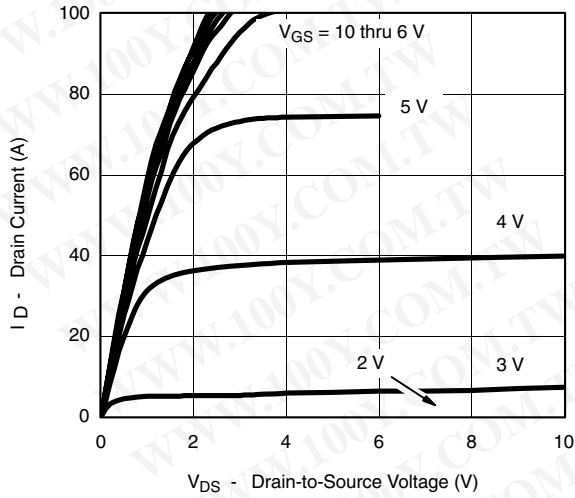
## Notes:

- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.

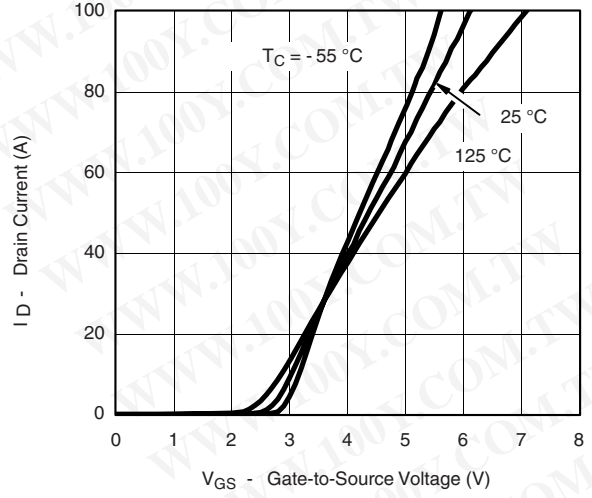
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



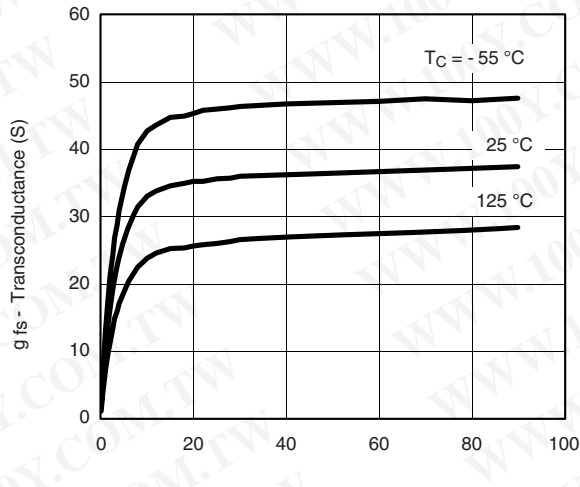
**TYPICAL CHARACTERISTICS** 25 °C unless noted



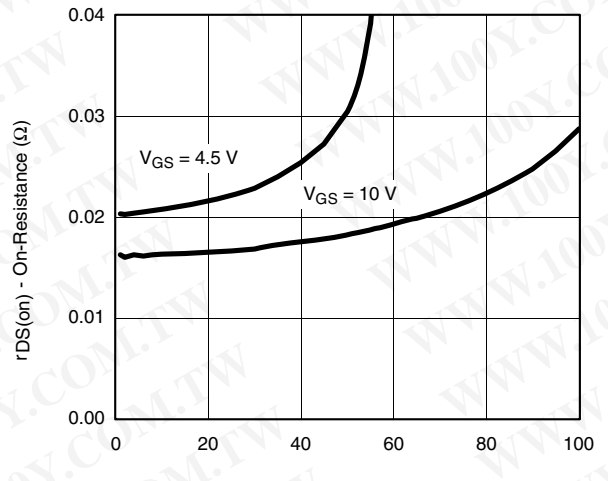
**Output Characteristics**



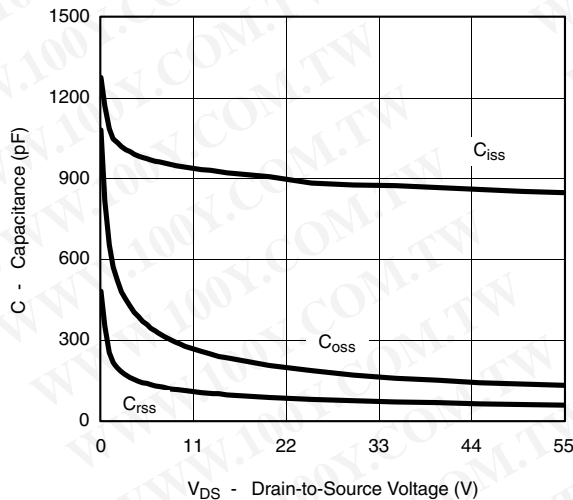
**Transfer Characteristics**



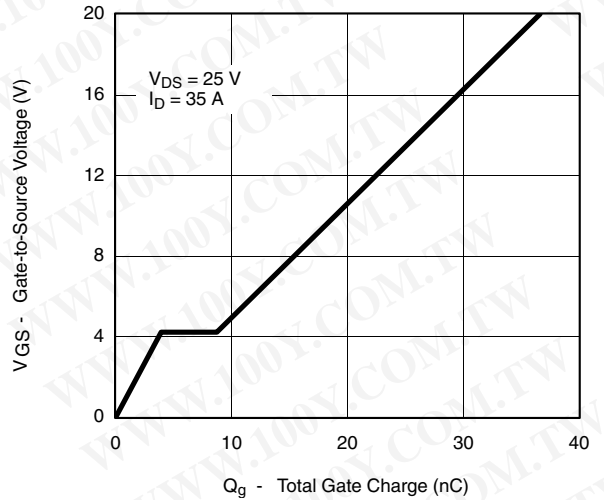
**Transconductance**



**On-Resistance vs. Drain Current**



**Capacitance**



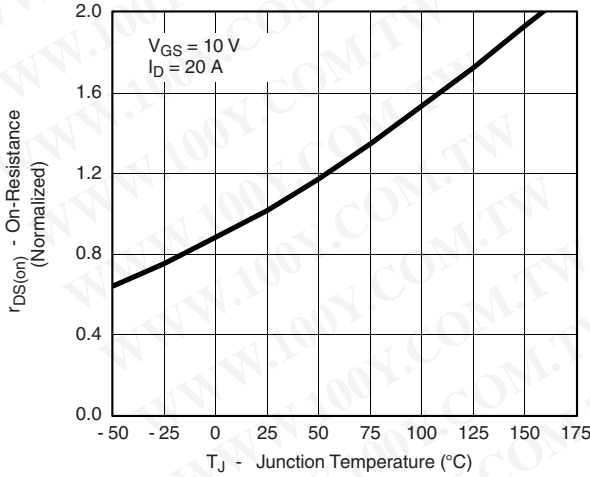
**Gate Charge**

# SUD35N05-26L

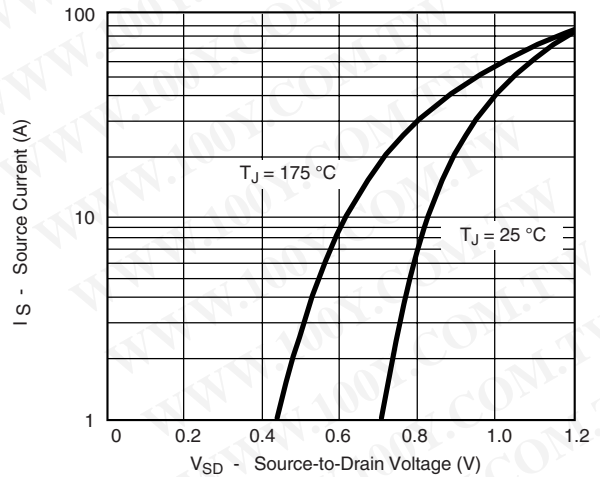


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## TYPICAL CHARACTERISTICS 25 °C unless noted

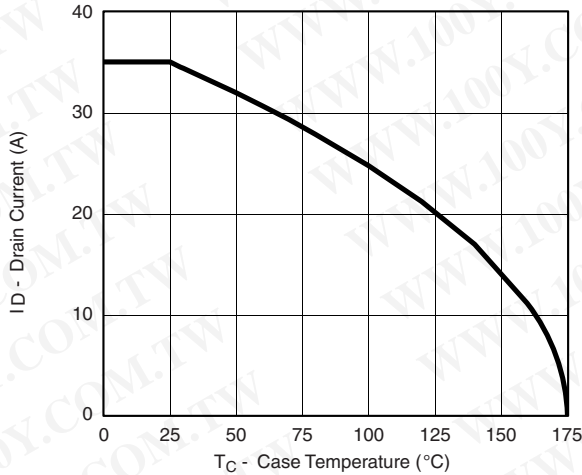


On-Resistance vs. Junction Temperature

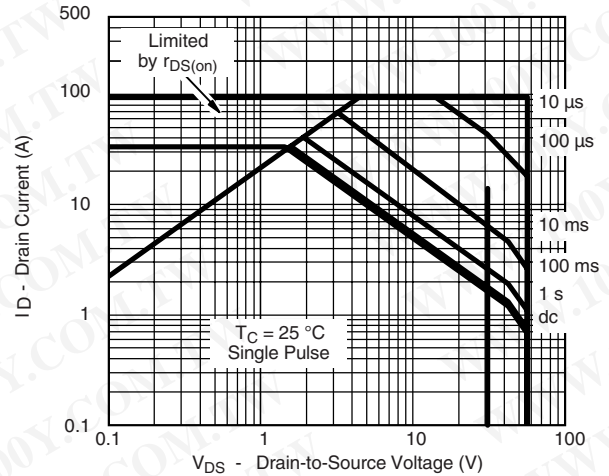


Source-Drain Diode Forward Voltage

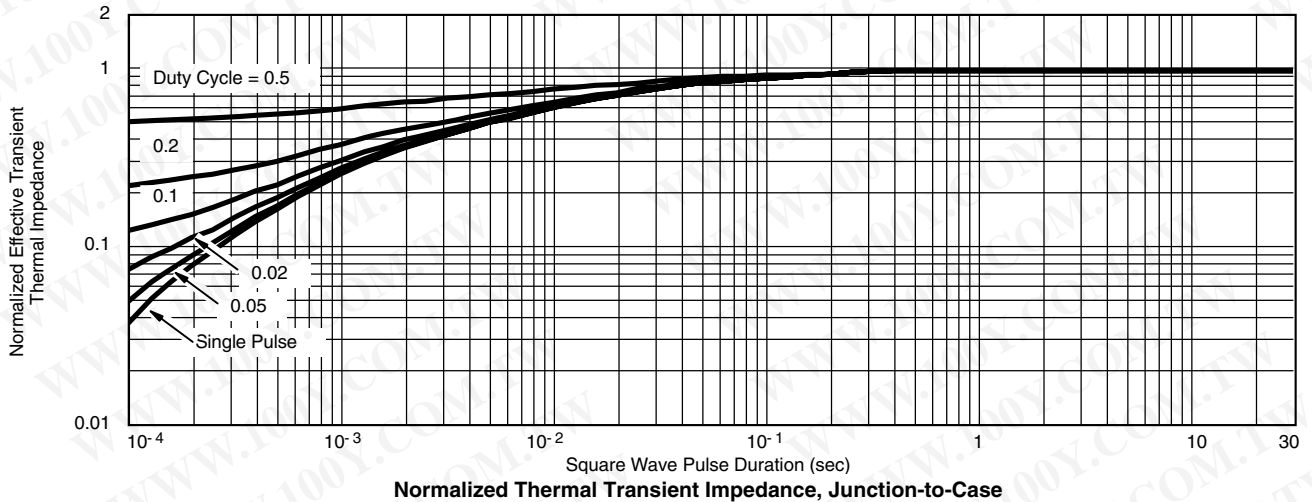
## THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71443>.



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