



N-Channel 200-V (D-S) 175°C MOSFET

PRODUCT SUMMARY

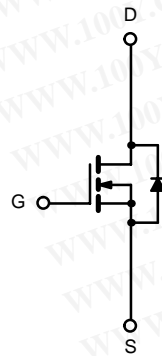
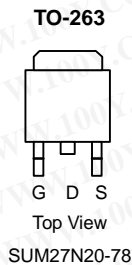
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.078 @ $V_{GS} = 10$ V	27
	0.083 @ $V_{GS} = 6$ V	26

FEATURES

- TrenchFET® Power MOSFET
- 175°C Junction Temperature
- New Low Thermal Resistance Package
- PWM Optimized for Fast Switching

APPLICATIONS

- Isolated DC/DC Converters
 - Primary-Side Switch



N-Channel MOSFET

勝特力材料 886-3-5753170
 勝特力电子(上海) 86-21-34970699
 勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	27	A
	$T_C = 125^\circ\text{C}$		15.5	
Pulsed Drain Current		I_{DM}	60	
Avalanche Current		I_{AR}	18	
Repetitive Avalanche Energy ^a	L = 0.1 mH	E_{AR}	16.2	mJ
Maximum Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	150 ^b	W
	$T_A = 25^\circ\text{C}$		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263) ^c	R_{thJA}	40	$^\circ\text{C/W}$
Junction-to-Case (Drain)		R_{thJC}	1.0	

Notes

- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	200			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V _{GS} = 0 V			1	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 15 V, V _{GS} = 10 V	60			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.064	0.078	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.160	
		V _{GS} = 10 V, I _D = 20 A, T _J = 175 °C			0.205	
Drain-Source on State Resistance		V _{GS} = 6 V, I _D = 15 A		0.068	0.083	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 30 A	15			S
Dynamic^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2150		pF
Output Capacitance	C _{oss}			215		
Reverse Transfer Capacitance	C _{rss}			90		
Total Gate Charge ^c	Q _g	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 20 A		40	60	nC
Gate-Source Charge ^c	Q _{gs}			11		
Gate-Drain Charge ^c	Q _{gd}			14		
Gate Resistance	R _G			2		Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 100 V, R _L = 5 Ω I _D ≅ 20 A, V _{GEN} = 10 V, R _G = 2.5 Ω		15	25	ns
Rise Time ^c	t _r			35	55	
Turn-Off Delay Time ^c	t _{d(off)}			40	60	
Fall Time ^c	t _f			30	45	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)^b						
Continuous Current	I _S				27	A
Pulsed Current	I _{SM}				60	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 50 A, di/dt = 100 A/μs		115	170	ns
Peak Reverse Recovery Current	I _{RM(REC)}			7.5	12	A
Reverse Recovery Charge	Q _{rr}			0.43	1.02	μC

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

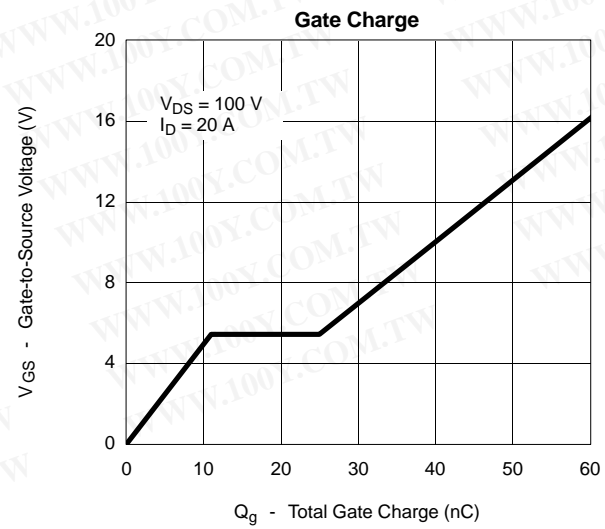
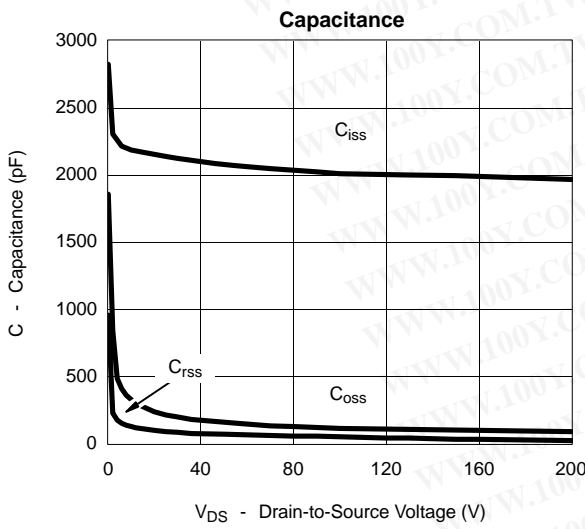
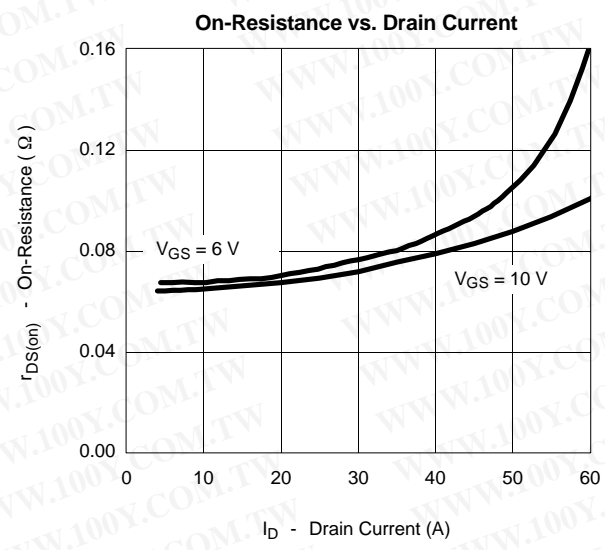
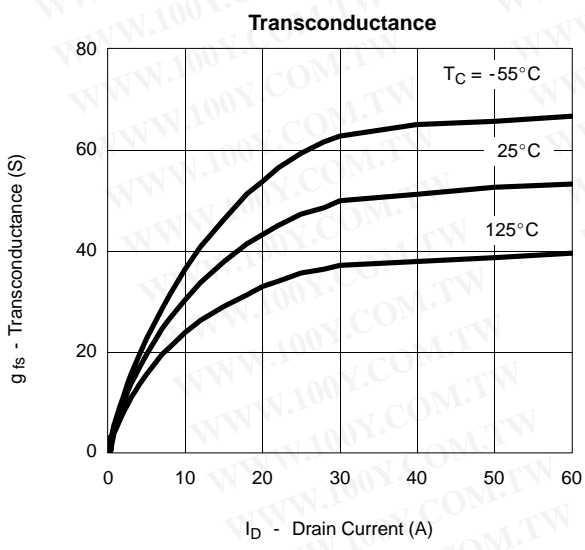
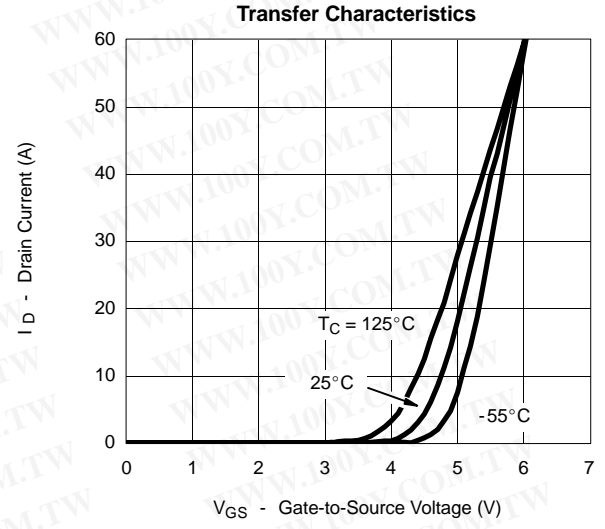
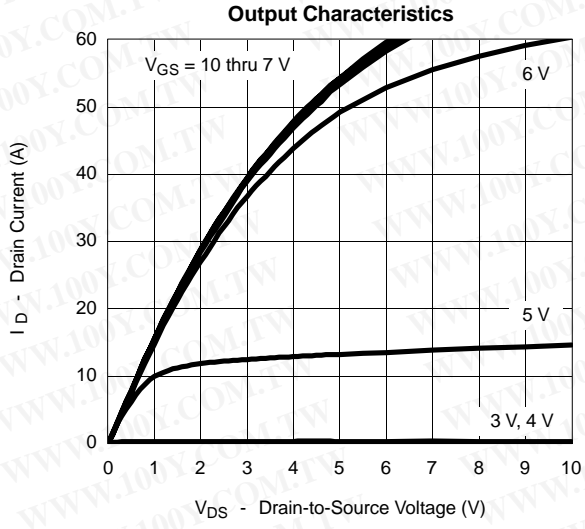
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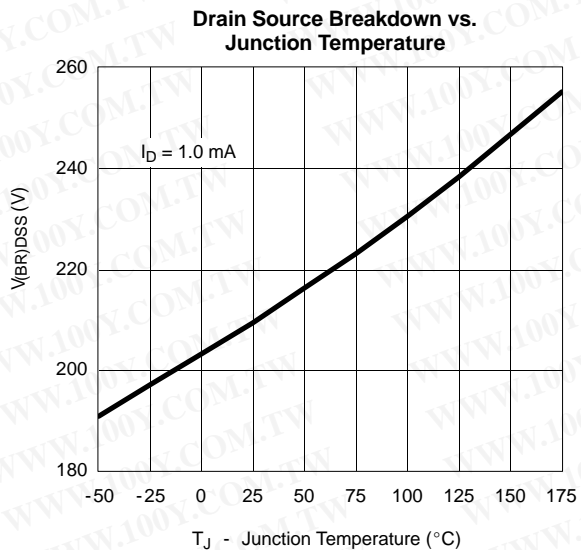
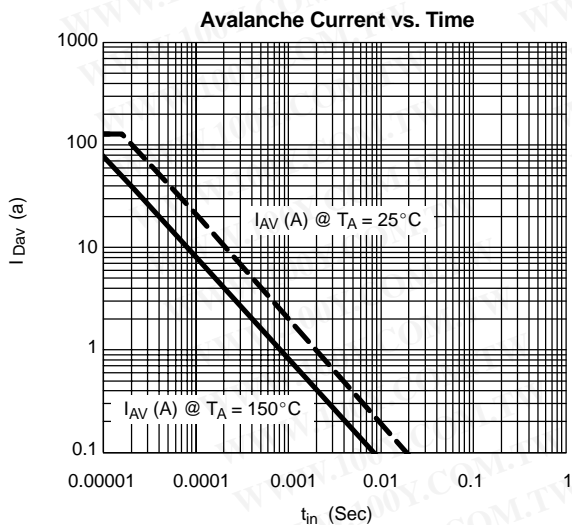
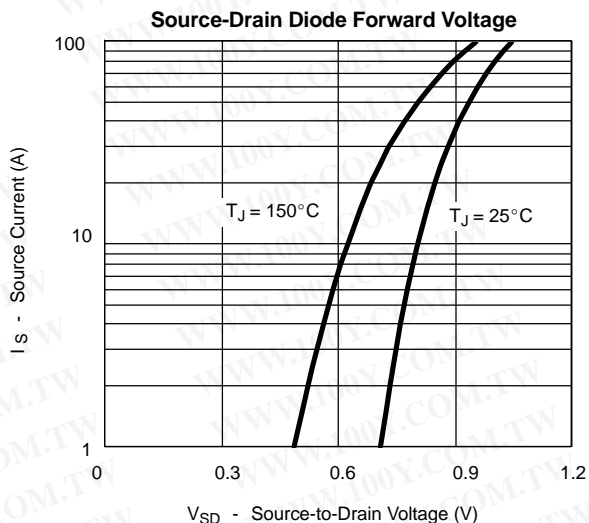
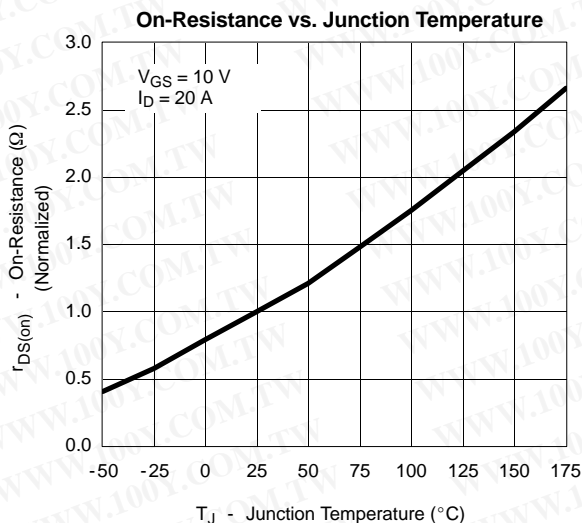
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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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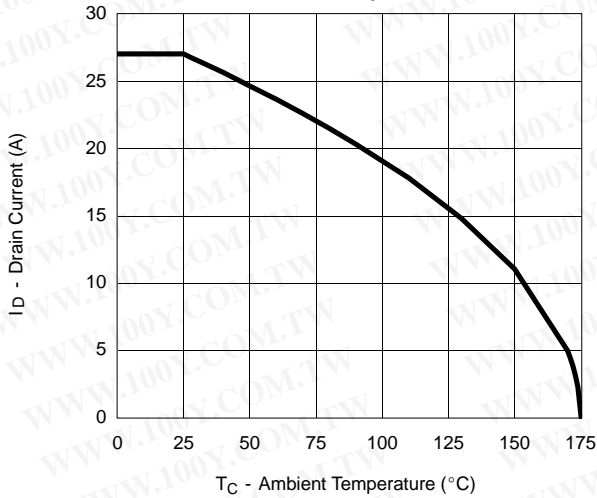


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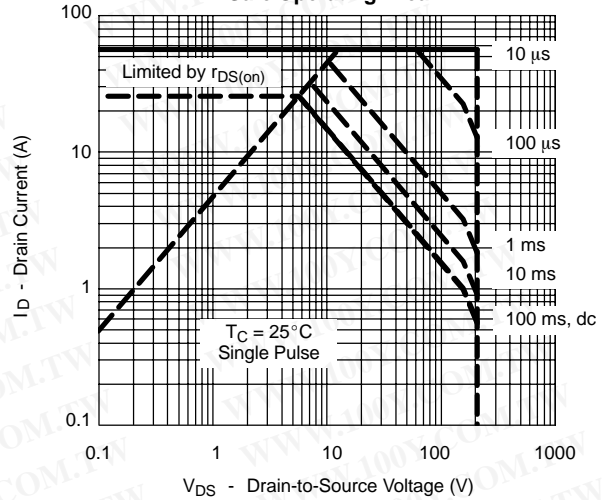


THERMAL RATINGS

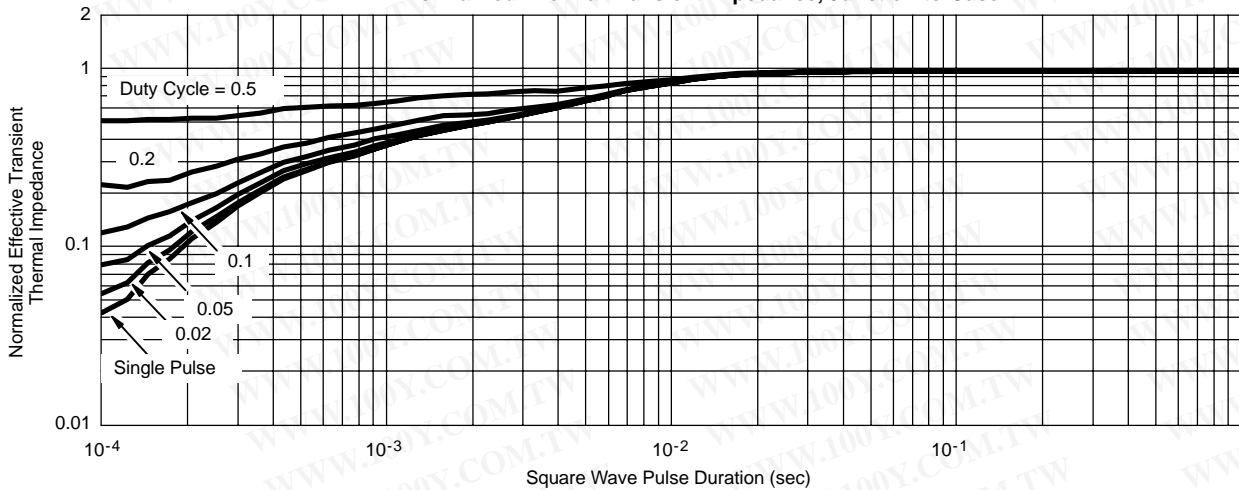
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



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