



## N-Channel 60-V (D-S), 175 °C MOSFET, Logic Level

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
60	0.016 at $V_{GS} = 10$ V	50
	0.022 at $V_{GS} = 4.5$ V	43

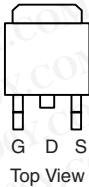
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature



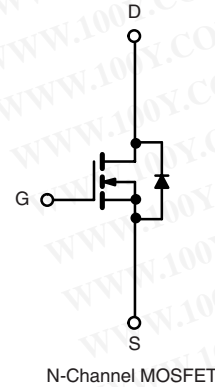
Available  
**RoHS\***  
 COMPLIANT

TO-263



DRAIN connected to TAB

Ordering Information: SUM50N06-16L  
 SUM50N06-16L-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	50	
		$T_C = 100$ °C	35	
Pulsed Drain Current	$I_{DM}$	100	A	
Avalanche Current	$I_{AR}$	40		
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	$E_{AR}$	80	mJ
Power Dissipation	$T_C = 25$ °C	$P_D$	93 <sup>b</sup>	W
	$T_A = 25$ °C <sup>c</sup>		3.7 <sup>c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient	$R_{thJA}$	40	(PCB Mount) <sup>c</sup>	°C/W
Junction-to-Case	$R_{thJC}$	1.6		

Notes:

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- Surface mounted on FR4 Board,  $t \leq 10$  s.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.



<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{DS} = 250\text{ }\mu\text{A}$	1.0	2.0	3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.013	0.016	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.028	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.036	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.017	0.022	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		50		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		1325		pF
Output Capacitance	$C_{oss}$			265		
Reverse Transfer Capacitance	$C_{rss}$			115		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		25	40	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			5.5		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			6.5		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.8\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		10	20	ns
Rise Time <sup>c</sup>	$t_r$			9	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			25	50	
Fall Time <sup>c</sup>	$t_f$			7	15	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	$I_S$				50	A
Pulsed Current	$I_{SM}$				100	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 50\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		35	70	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			2.3	4	A
Reverse Recovery Charge	$Q_{rr}$				0.04	0.14

**Notes:**

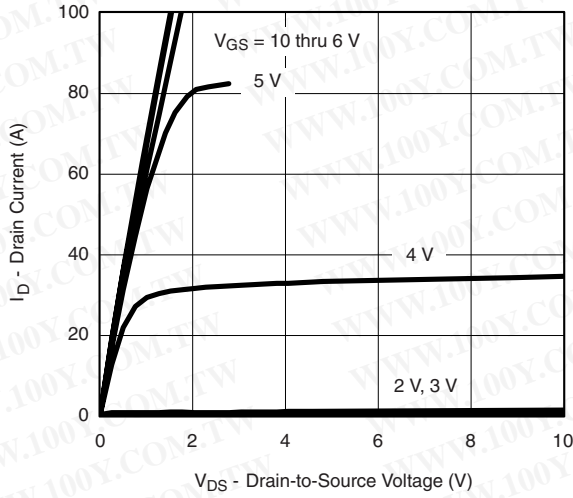
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

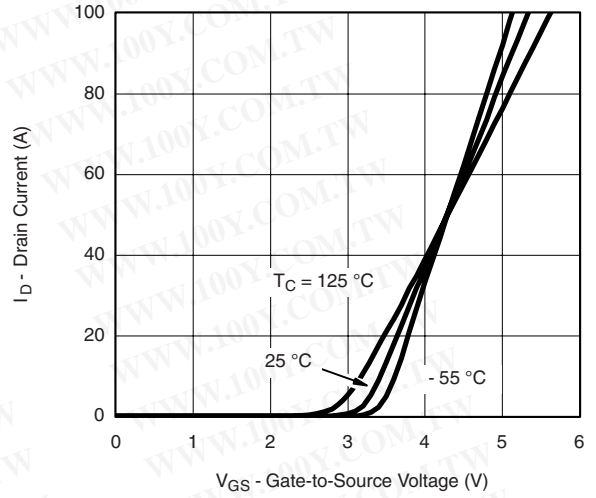
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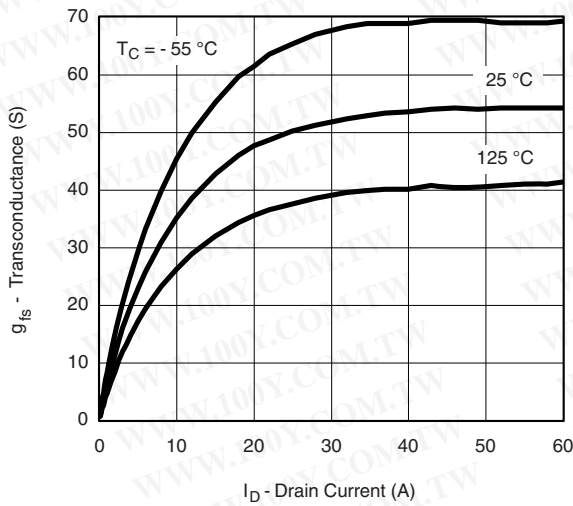
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



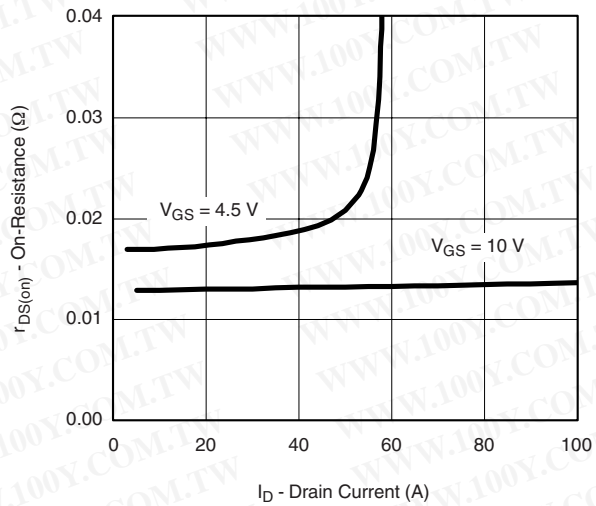
**Output Characteristics**



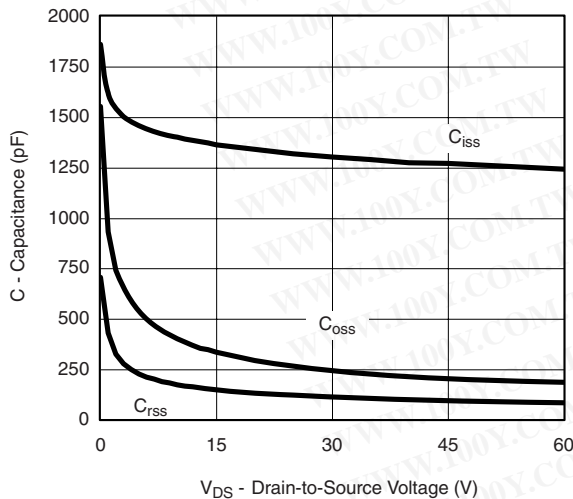
**Transfer Characteristics**



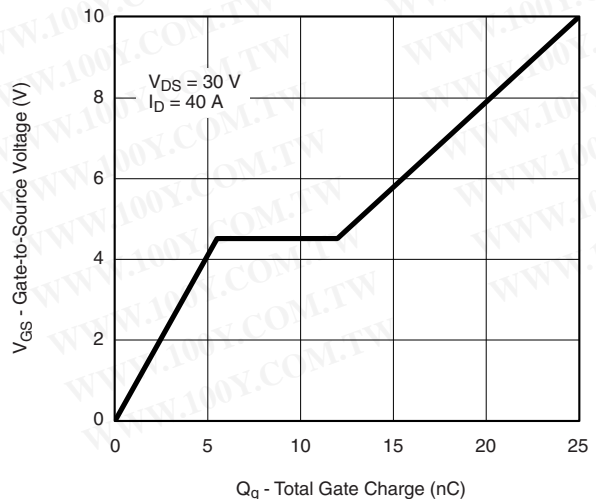
**Transconductance**



**On-Resistance vs. Drain Current**

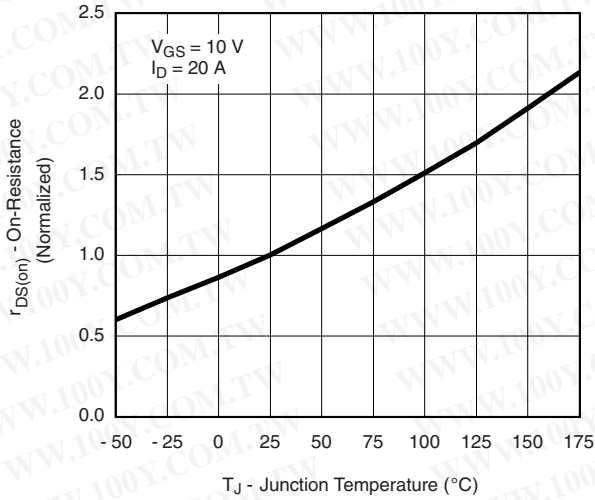


**Capacitance**

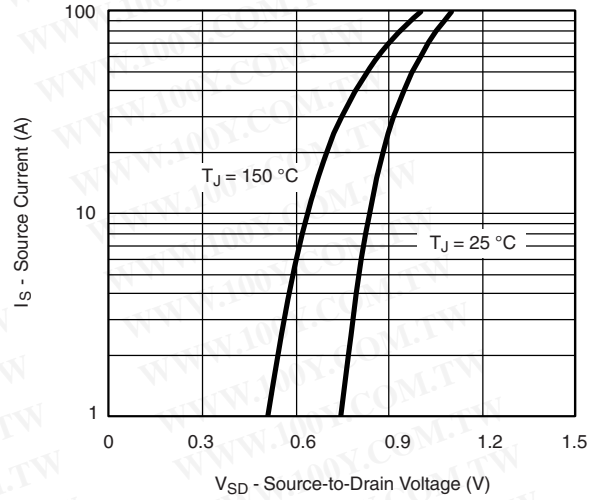


**Gate Charge**

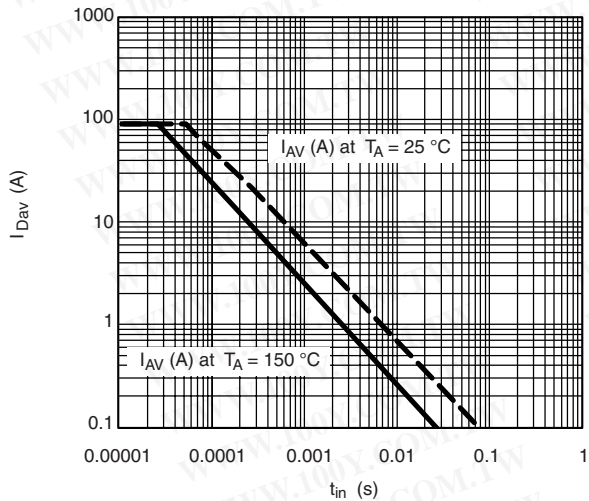
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



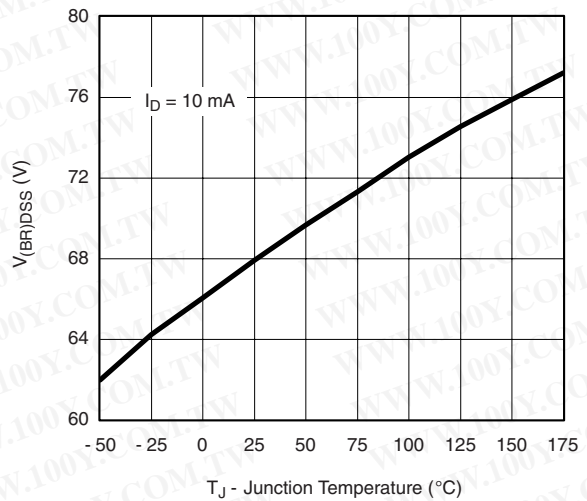
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



**Drain Source Breakdown vs. Junction Temperature**

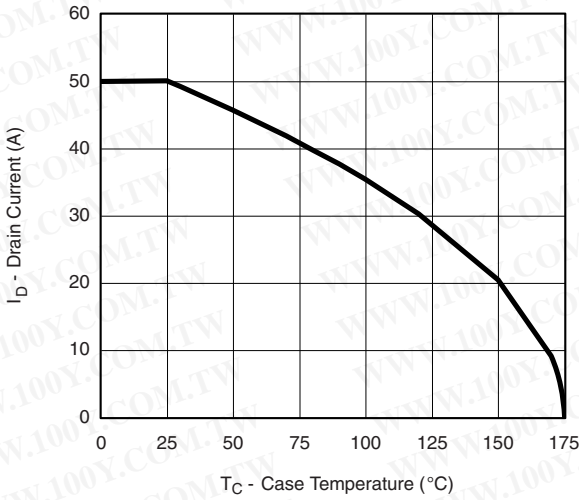


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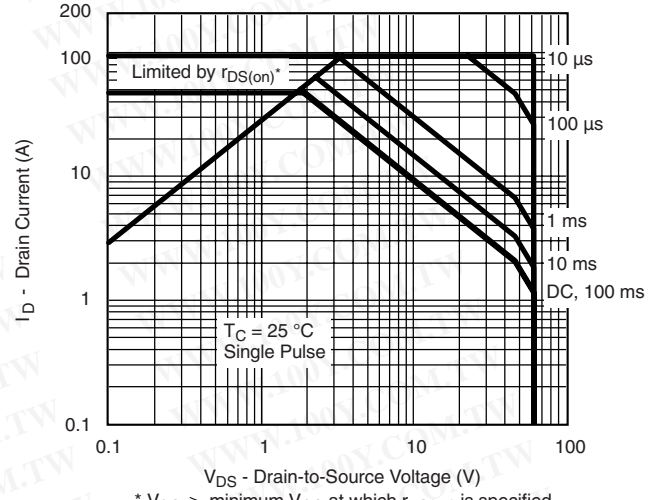




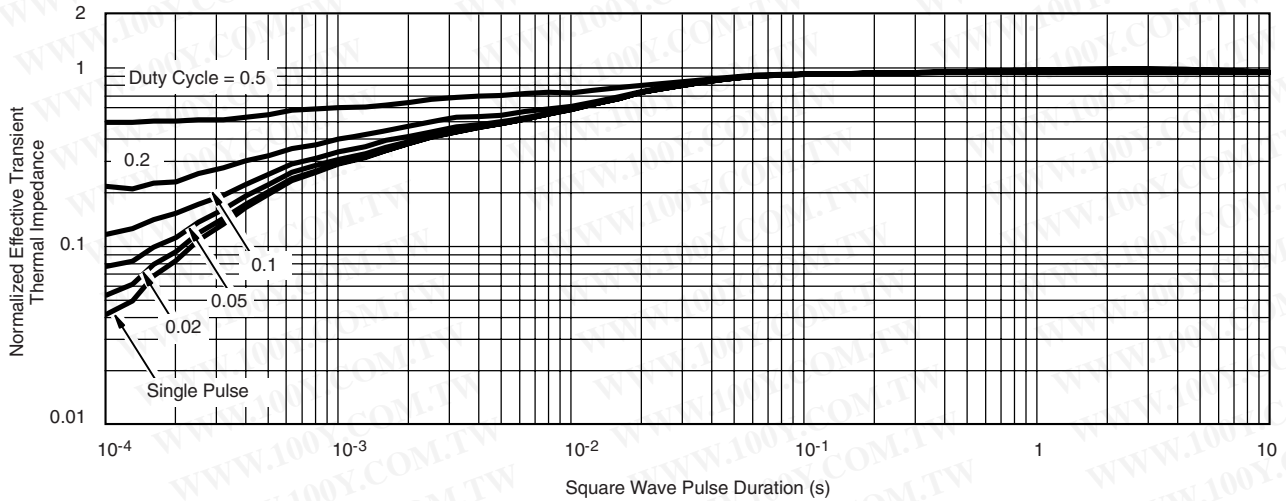
THERMAL RATINGS



Drain Current vs. Case Temperature



Safe Operating Area

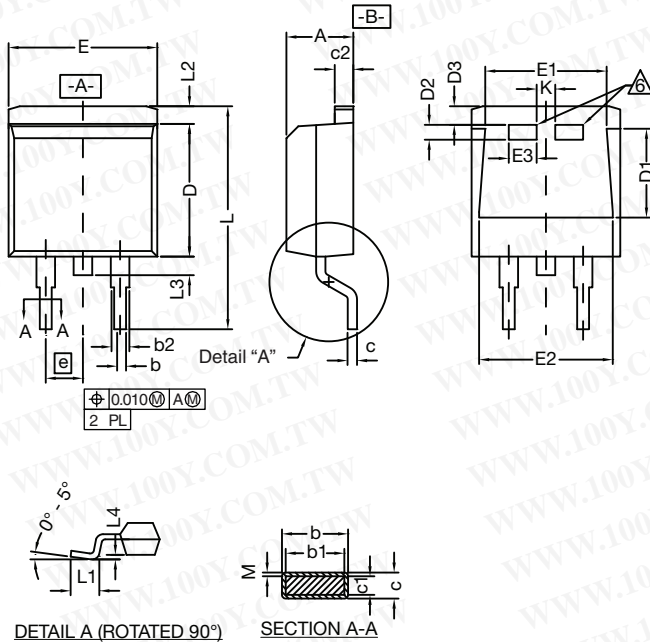


Normalized Thermal Transient Impedance, Junction-to-Case

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### TO-263 (D<sup>2</sup>PAK): 3-LEAD

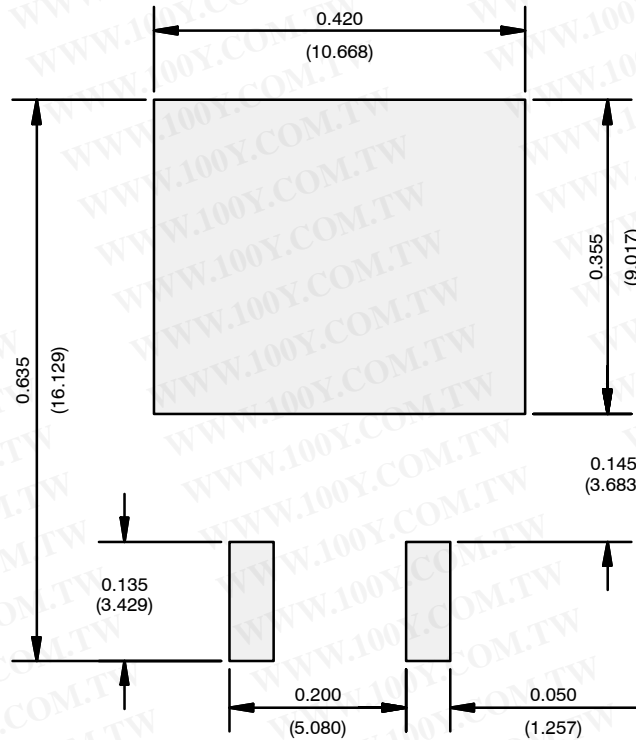


DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T10-0738-Rev. J, 03-Jan-11					
DWG: 5843					

#### Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- $\triangle$  This feature is for thick lead.

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**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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