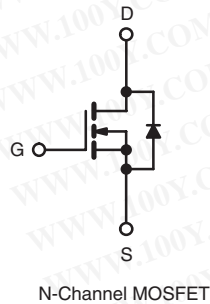


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	1.5
Q_g (Max.) (nC)	38	
Q_{gs} (nC)	5.0	
Q_{gd} (nC)	22	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available


 Available
RoHS*
 COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRF830PbF
	SiHF830-E3
SnPb	IRF830
	SiHF830

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	18	
Linear Derating Factor		0.59	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	280	mJ
Repetitive Avalanche Current ^a	I_{AR}	4.5	A
Repetitive Avalanche Energy ^a	E_{AR}	7.4	mJ
Maximum Power Dissipation	P_D	74	W
Peak Diode Recovery dV/dt^c	dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	
		1.1	N · m



Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 4.5\text{ A}$ (see fig. 12).
- $I_{SD} \leq 4.5\text{ A}$, $dI/dt \leq 75\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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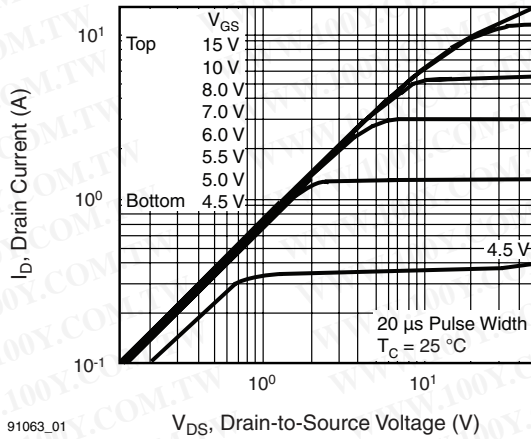
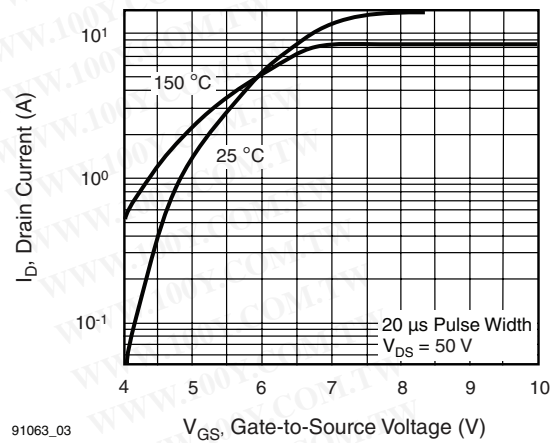
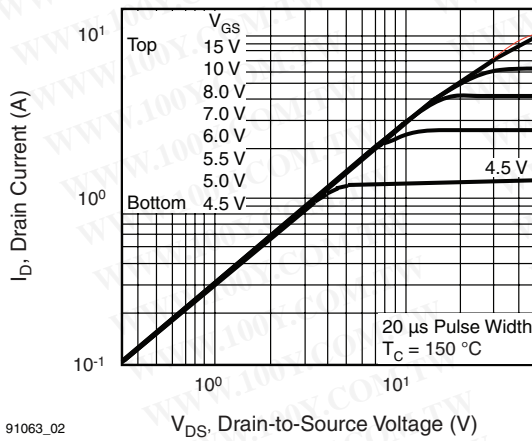
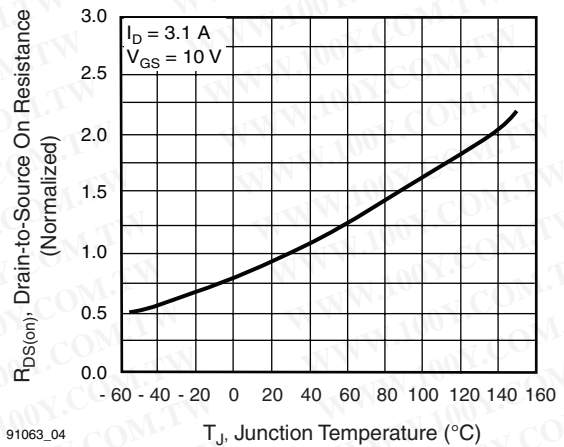
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.61	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 2.7\text{ A}^b$	-	-	1.5	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 2.7\text{ A}^b$	2.5	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	610	-	pF
Output Capacitance	C_{oss}		-	160	-	
Reverse Transfer Capacitance	C_{rss}		-	68	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 3.1\text{ A}, V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	38	nC
Gate-Source Charge	Q_{gs}		-	-	5.0	
Gate-Drain Charge	Q_{gd}		-	-	22	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 3.1\text{ A}, R_G = 12\text{ }\Omega, R_D = 79\text{ }\Omega$, see fig. 10 ^b	-	8.2	-	ns
Rise Time	t_r		-	16	-	
Turn-Off Delay Time	$t_{d(off)}$		-	42	-	
Fall Time	t_f		-	16	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 	-	-	4.5	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	18	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 4.5\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 3.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	320	640	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.0	2.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

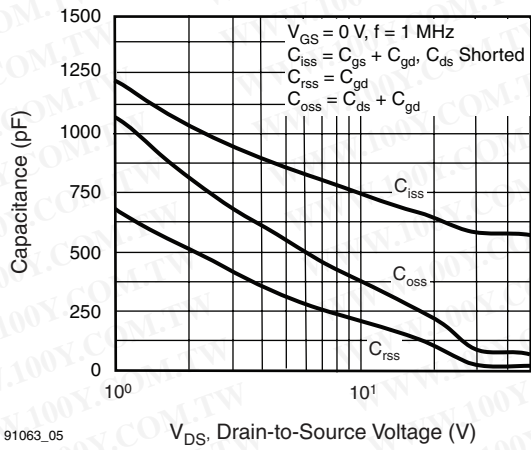
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

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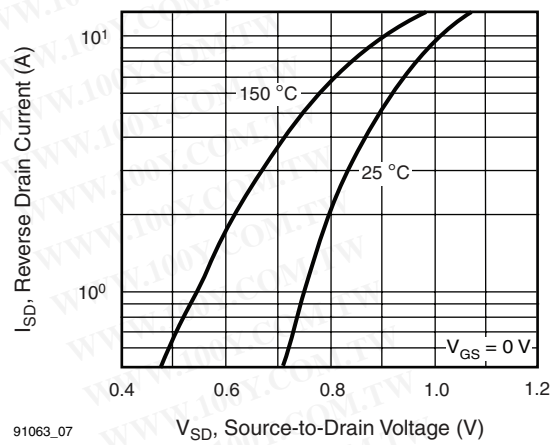
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

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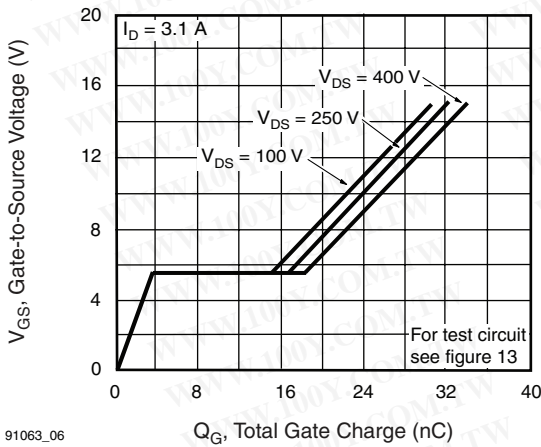
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



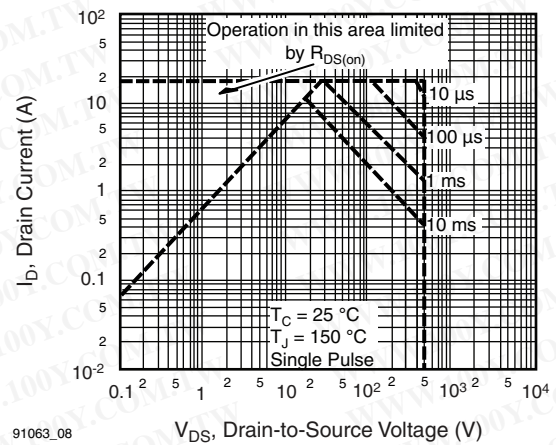
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Drain-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area

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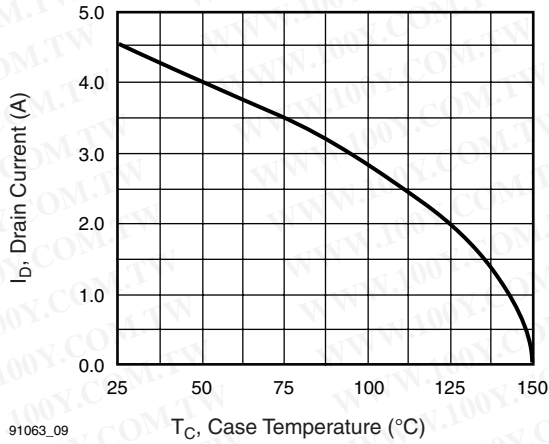


Fig. 9 - Maximum Drain Current vs. Case Temperature

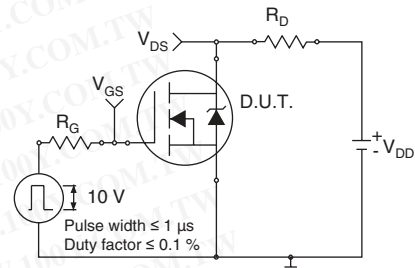


Fig. 10a - Switching Time Test Circuit

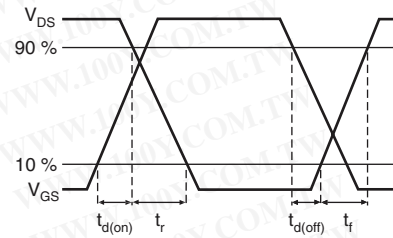


Fig. 10b - Switching Time Waveforms

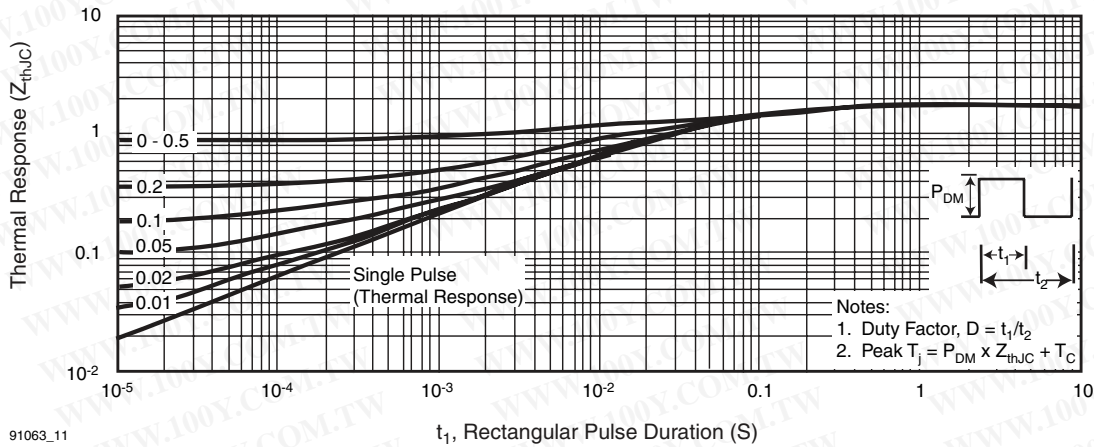


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

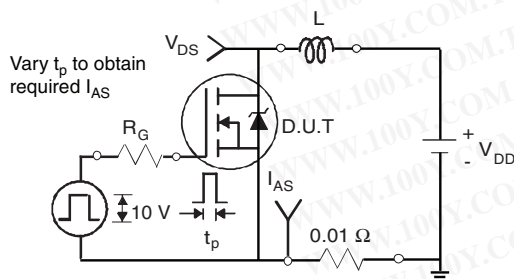


Fig. 12a - Unclamped Inductive Test Circuit

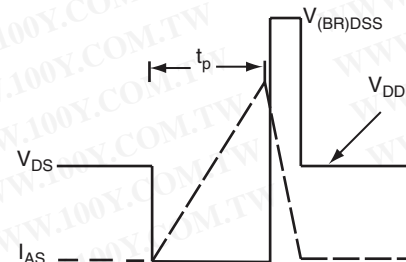


Fig. 12b - Unclamped Inductive Waveforms

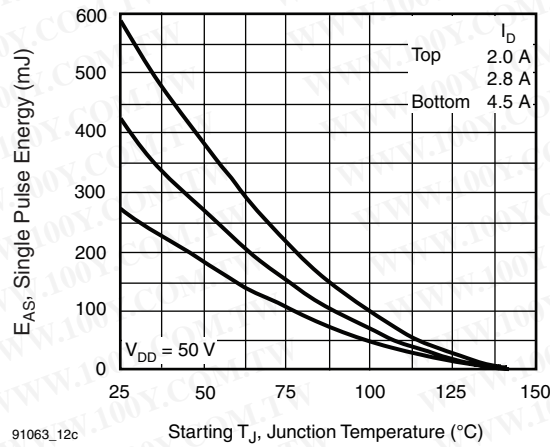


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

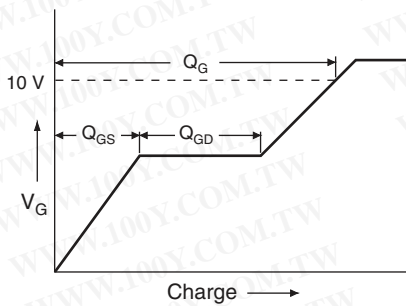


Fig. 13a - Basic Gate Charge Waveform

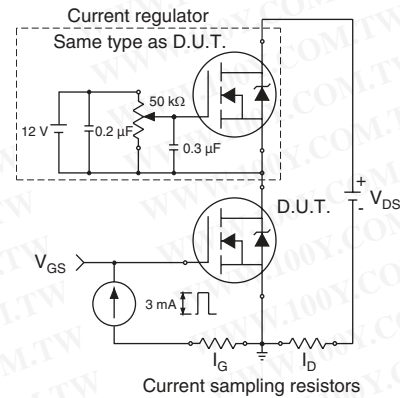
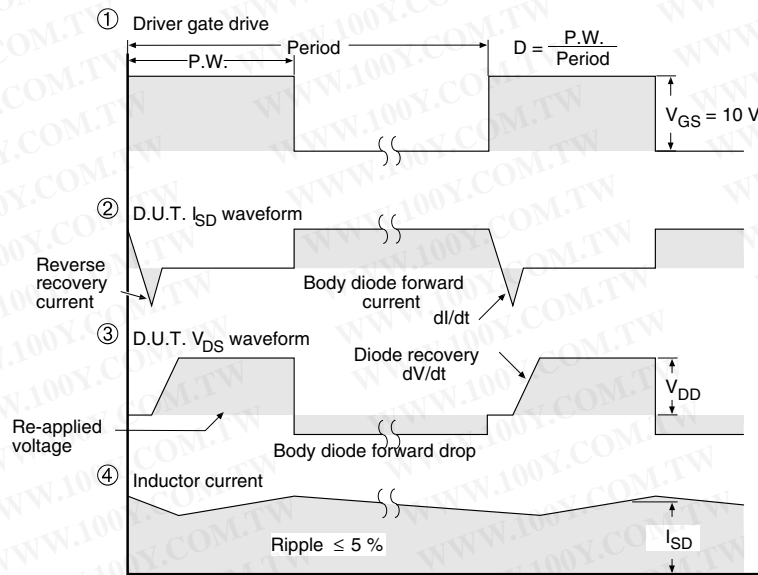
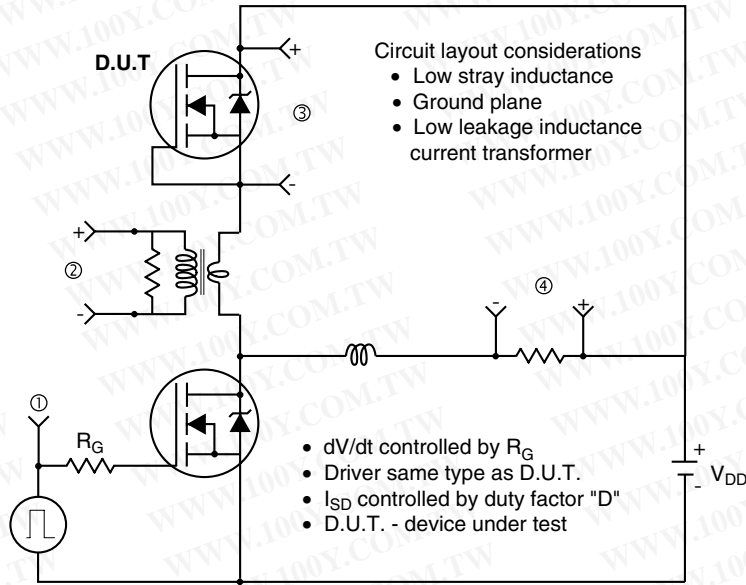


Fig. 13b - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit


* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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