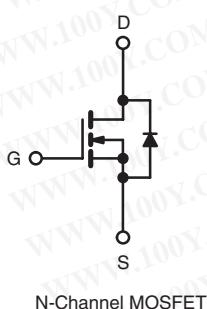


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.20
$Q_g$ (Max.) (nC)		210
$Q_{gs}$ (nC)		30
$Q_{gd}$ (nC)		110
Configuration	Single	



### FEATURES

- Dynamic dV/dt Rated
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Lead (Pb)-free Available


**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

### ORDERING INFORMATION

Package	TO-247
Lead (Pb)-free	IRFP360PbF SiHFP360-E3
SnPb	IRFP360 SiHFP360

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	400	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	23	A
		14	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	92	
Linear Derating Factor		2.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	1200	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	23	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	28	mJ
Maximum Power Dissipation	$P_D$	280	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 4.0$  mH,  $R_G = 25 \Omega$ ,  $I_{AS} = 23$  A (see fig. 12).
- $I_{SD} \leq 23$  A,  $dI/dt \leq 170$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

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**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.45	

**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$	$I_D = 250 \mu\text{A}$	400	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1 \text{ mA}$		-	0.56	-	$\text{V}/^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$	
		$V_{DS} = 320 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125^\circ\text{C}$		-	-	250		
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 14 \text{ A}^b$	-	-	0.20	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50 \text{ V}$ , $I_D = 14 \text{ A}^b$		14	-	-	S	
<b>Dynamic</b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	4500	-	pF	
Output Capacitance	$C_{oss}$			-	1100	-		
Reverse Transfer Capacitance	$C_{rss}$			-	490	-		
Total Gate Charge	$Q_g$	$V_{GS} = 10 \text{ V}$	$I_D = 23 \text{ A}$ , $V_{DS} = 320 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	210	nC	
Gate-Source Charge	$Q_{gs}$			-	-	30		
Gate-Drain Charge	$Q_{gd}$			-	-	110		
Turn-On Delay Time	$t_{d(\text{on})}$			-	18	-		
Rise Time	$t_r$	$V_{DD} = 200 \text{ V}$ , $I_D = 23 \text{ A}$ , $R_G = 4.3 \Omega$ , $R_D = 8.3 \Omega$ , see fig. 10 <sup>b</sup>		-	79	-	ns	
Turn-Off Delay Time	$t_{d(\text{off})}$			-	100	-		
Fall Time	$t_f$			-	67	-		
Internal Drain Inductance	$L_D$			-	5.0	-	nH	
Internal Source Inductance	$L_S$	Between lead, 6 mm (0.25") from package and center of die contact		-	13	-		
<b>Drain-Source Body Diode Characteristics</b>								
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	23	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	92		
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 23 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	1.8	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 23 \text{ A}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	420	630	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	5.6	8.4	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )						

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

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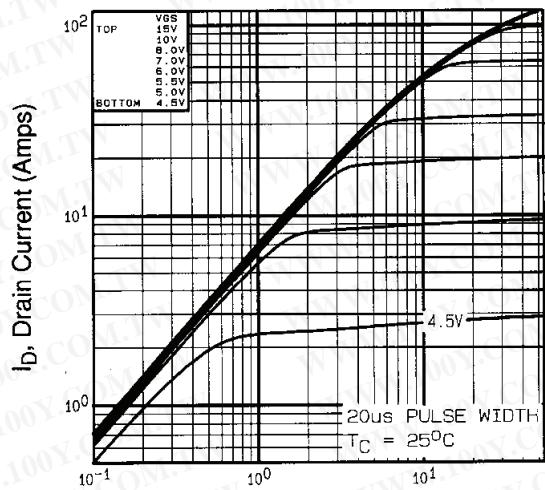
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

 $V_{DS}$ , Drain-to-Source Voltage (volts)

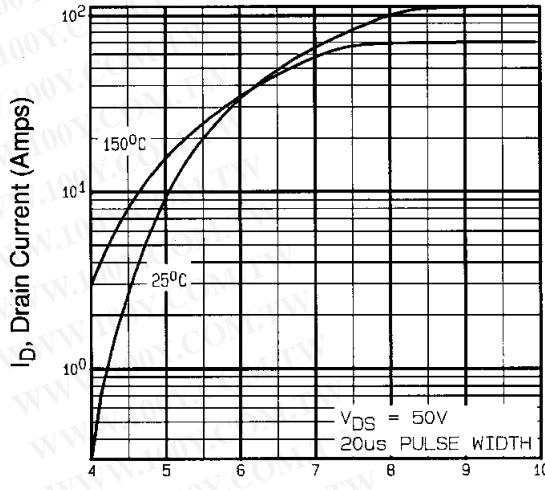
Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$ 

 $V_{GS}$ , Gate-to-Source Voltage (volts)

Fig. 3 - Typical Transfer Characteristics

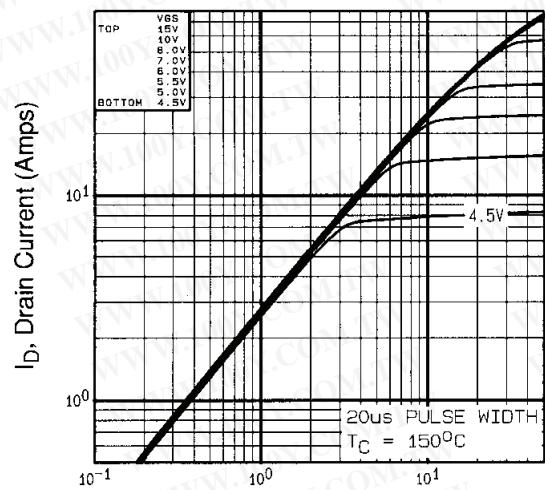

 $V_{DS}$ , Drain-to-Source Voltage (volts)

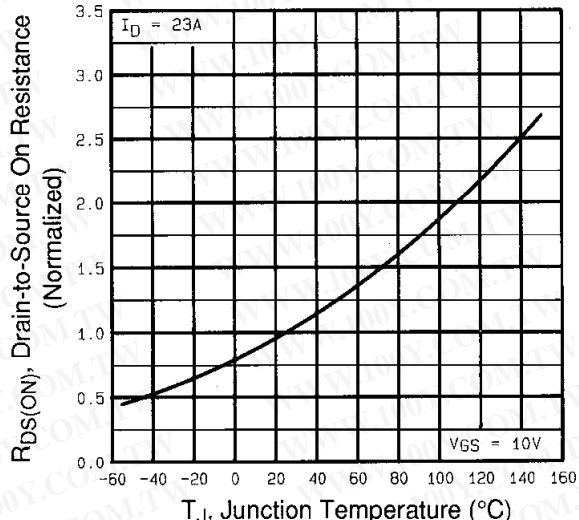
Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$ 


Fig. 4 - Normalized On-Resistance vs. Temperature

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# IRFP360, SiHFP360



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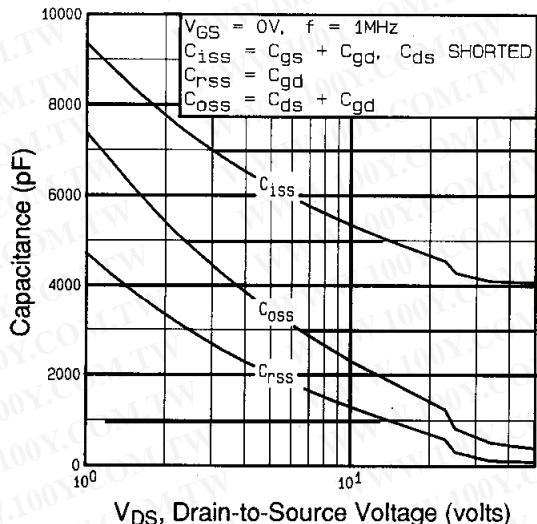


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

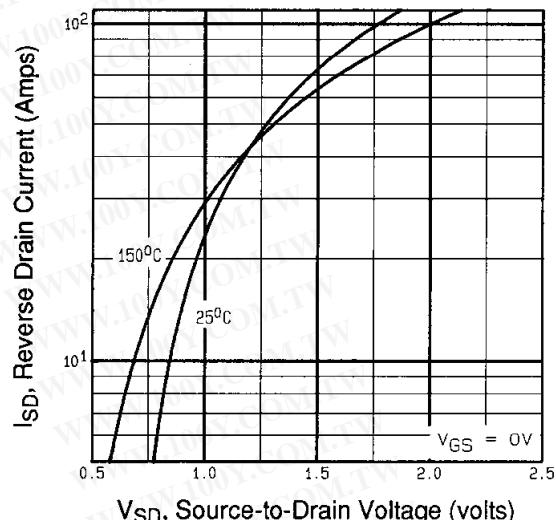


Fig. 7 - Typical Source-Drain Diode Forward Voltage

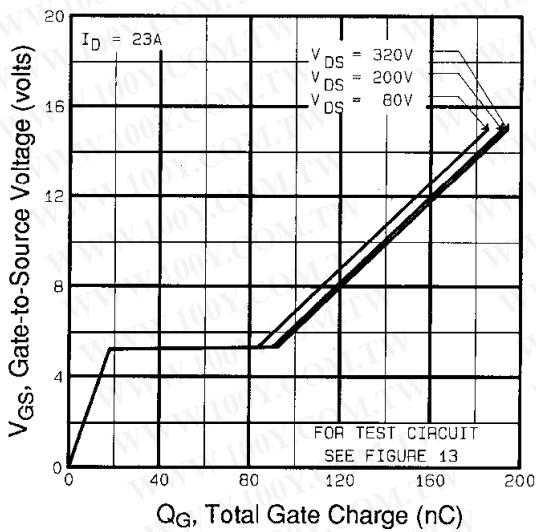


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

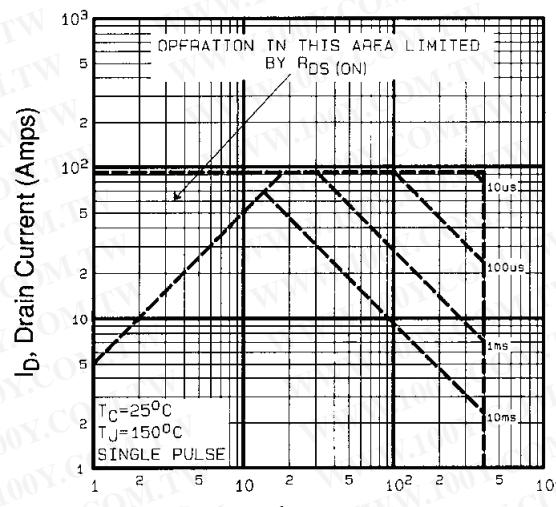


Fig. 8 - Maximum Safe Operating Area

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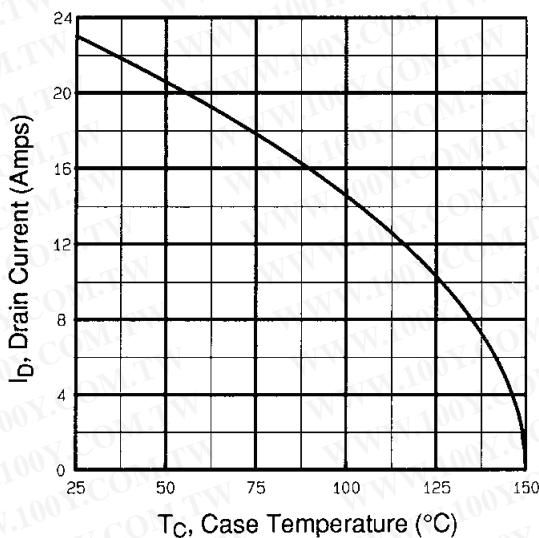


Fig. 9 - Maximum Drain Current vs. Case Temperature

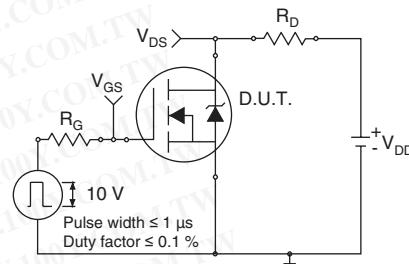


Fig. 10a - Switching Time Test Circuit

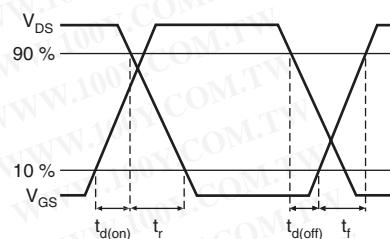


Fig. 10b - Switching Time Waveforms

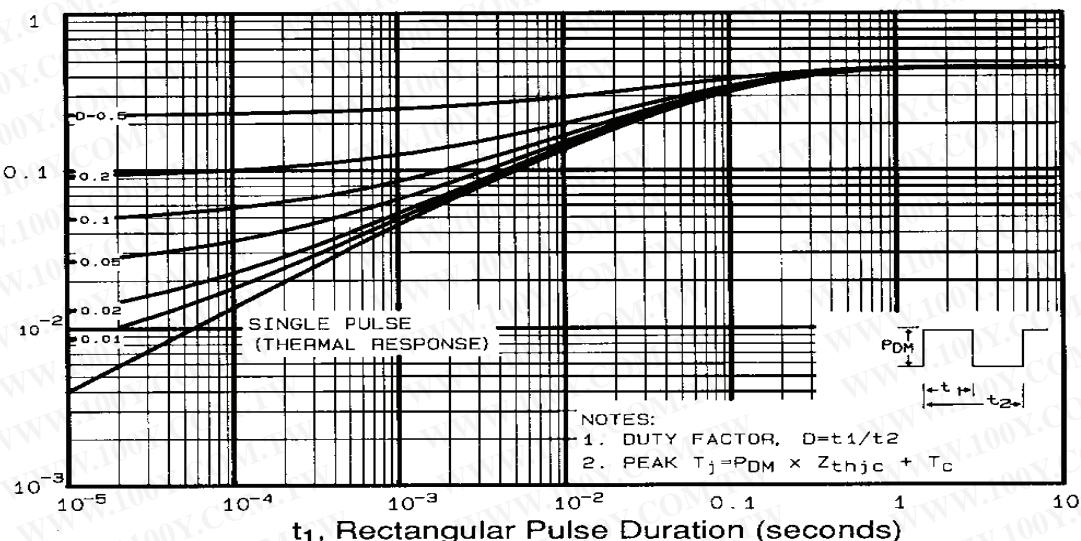


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

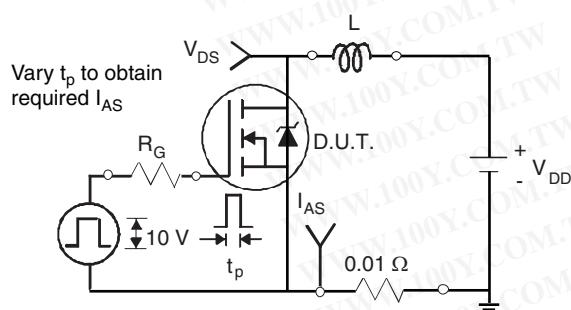


Fig. 12a - Unclamped Inductive Test Circuit

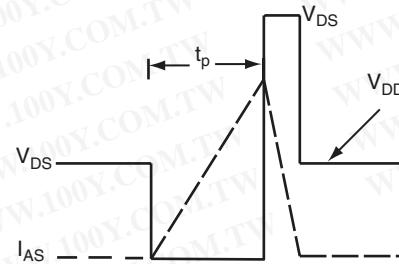


Fig. 12b - Unclamped Inductive Waveforms

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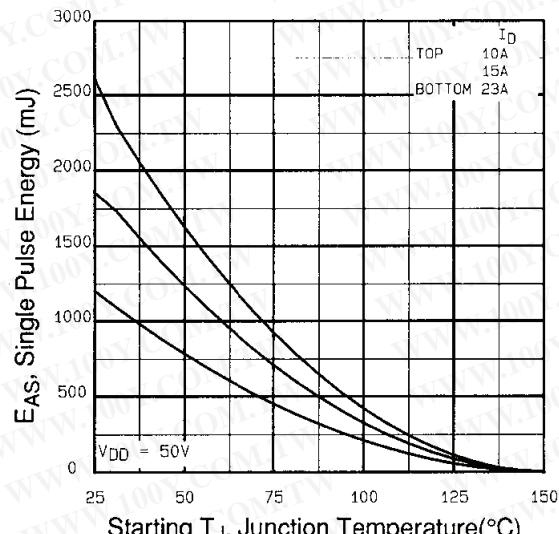


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

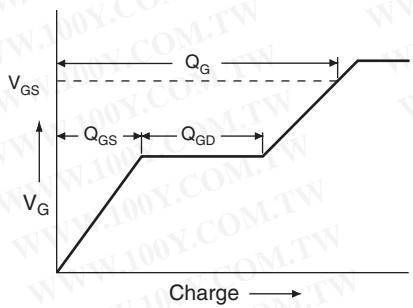


Fig. 13a - Basic Gate Charge Waveform

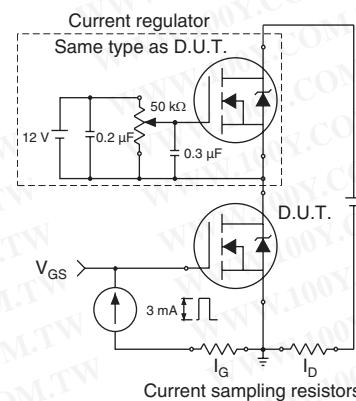
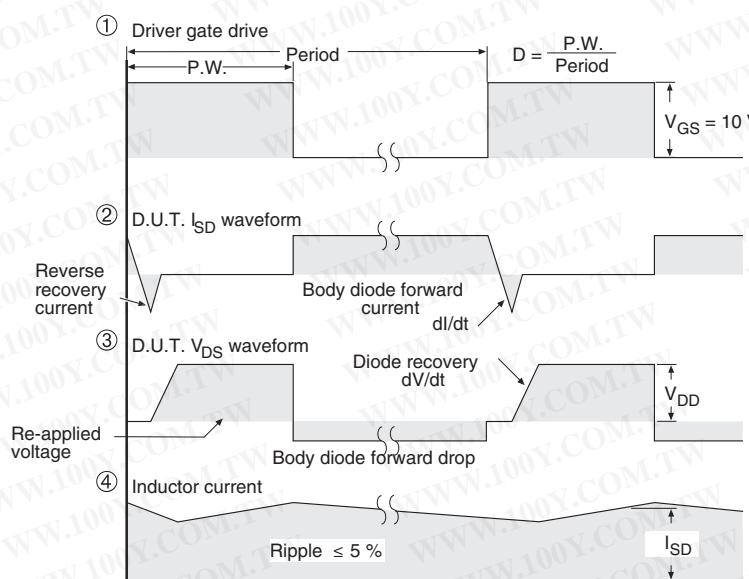
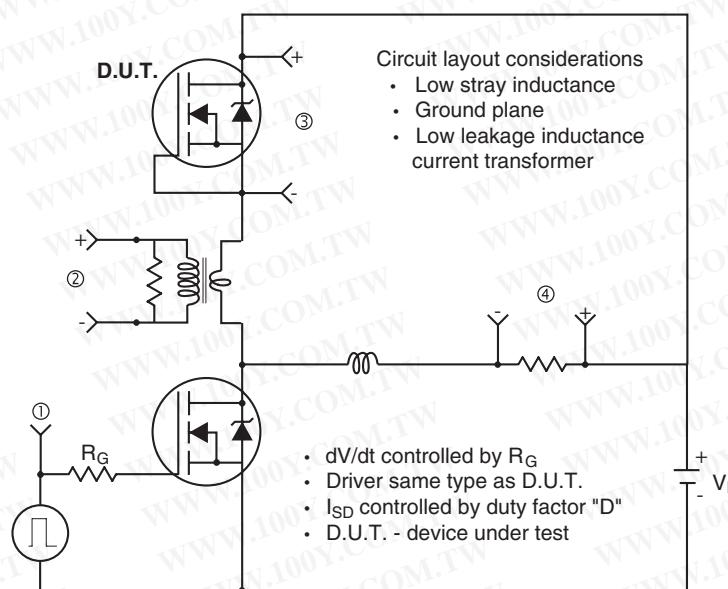


Fig. 13b - Gate Charge Test Circuit

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### Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 \text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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