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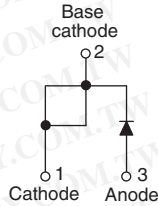
# VS-15ETX06PbF, VS-15ETX06FPPbF

Vishay Semiconductors

## Ultrafast Rectifier, 15 A FRED Pt®



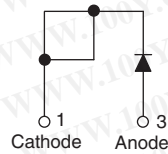
TO-220AC



VS-15ETX06PbF



TO-220 FULL-PAK



VS-15ETX06FPPbF

### FEATURES

- Hyperfast recovery time
- Low forward voltage drop
- 175 °C operating junction temperature
- Benchmark ultralow forward voltage drop
- Low leakage current
- Fully isolated package ( $V_{INS} = 2500 V_{RMS}$ )
- UL E78996 pending
- Compliant to RoHS Directive 2002/95/EC
- Designed and qualified for industrial level



RoHS  
COMPLIANT

### DESCRIPTION/APPLICATIONS

State of the art hyperfast recovery rectifiers designed with optimized performance of forward voltage drop, hyperfast recovery time, and soft recovery.

The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness and reliability characteristics.

These devices are intended for use in PFC boost stage in the AC/DC section of SMPS, inverters or as freewheeling diodes.

Their extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

### PRODUCT SUMMARY

Package	TO-220AC, TO-220FP
$I_{F(AV)}$	15 A
$V_R$	600 V
$V_F$ at $I_F$	3.2 V
$t_{rr}$ typ.	18 ns
$T_J$ max.	175 °C
Diode variation	Single die

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	$V_{RRM}$		600	V
Average rectified forward current	$I_{F(AV)}$	$T_C = 133\text{ °C}$	15	A
		$T_C = 62\text{ °C (FULL-PAK)}$		
Non-repetitive peak surge current	$I_{FSM}$	$T_J = 25\text{ °C}$	170	
Peak repetitive forward current	$I_{FM}$		30	
Operating junction and storage temperatures	$T_J, T_{Stg}$		- 65 to 175	°C

### ELECTRICAL SPECIFICATIONS ( $T_J = 25\text{ °C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Breakdown voltage, blocking voltage	$V_{BR}, V_R$	$I_R = 100\text{ }\mu\text{A}$	600	-	-	V
$I_F = 15\text{ A}, T_J = 150\text{ °C}$	1.5	1.8				
Reverse leakage current	$I_R$	$V_R = V_R$ rated	-	0.1	50	
		$T_J = 150\text{ °C}, V_R = V_R$ rated	-	40	300	
Junction capacitance	$C_T$	$V_R = 600\text{ V}$	-	20	-	pF
Series inductance	$L_S$	Measured lead to lead 5 mm from package body	-	8.0	-	nH

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Vishay Semiconductors Ultrafast Rectifier, 15 A FRED Pt®

DYNAMIC RECOVERY CHARACTERISTICS ( $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse recovery time	$t_{rr}$	$I_F = 1\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 30\text{ V}$	-	18	22	ns
		$I_F = 15\text{ A}$ , $di_F/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 30\text{ V}$	-	20	32	
		$T_J = 25\text{ }^\circ\text{C}$	-	22	-	
		$T_J = 125\text{ }^\circ\text{C}$	-	52	-	
Peak recovery current	$I_{RRM}$	$T_J = 25\text{ }^\circ\text{C}$	-	2.4	-	A
		$T_J = 125\text{ }^\circ\text{C}$	-	5.1	-	
Reverse recovery charge	$Q_{rr}$	$T_J = 25\text{ }^\circ\text{C}$	-	25	-	$\mu\text{C}$
		$T_J = 125\text{ }^\circ\text{C}$	-	150	-	
Reverse recovery time	$t_{rr}$	$I_F = 15\text{ A}$ $di_F/dt = 200\text{ A}/\mu\text{s}$ $V_R = 390\text{ V}$	-	37	-	ns
Peak recovery current	$I_{RRM}$		-	16	-	A
Reverse recovery charge	$Q_{rr}$		-	350	-	nC

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	$T_J$ , $T_{Stg}$		- 65	-	175	$^\circ\text{C}$
Thermal resistance, junction to case (FULL-PAK)	$R_{thJC}$		-	1.0	1.3	$^\circ\text{C}/\text{W}$
Thermal resistance, junction to ambient per leg	$R_{thJA}$	Typical socket mount	-	3.0	3.5	
Thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, flat, smooth and greased	-	0.5	-	
Weight			-	2.0	-	g
			-	0.07	-	oz.
Mounting torque			6.0 (5.0)	-	12 (10)	kgf · cm (lbf · in)
Marking device		Case style TO-220AC	15ETX06			
		Case style TO-220 FULL-PAK	15ETX06FP			

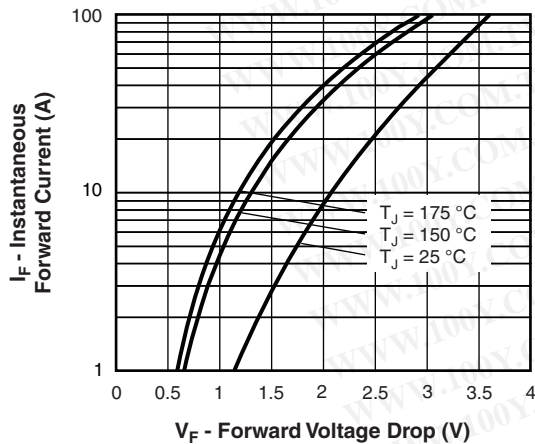


Fig. 1 - Typical Forward Voltage Drop Characteristics

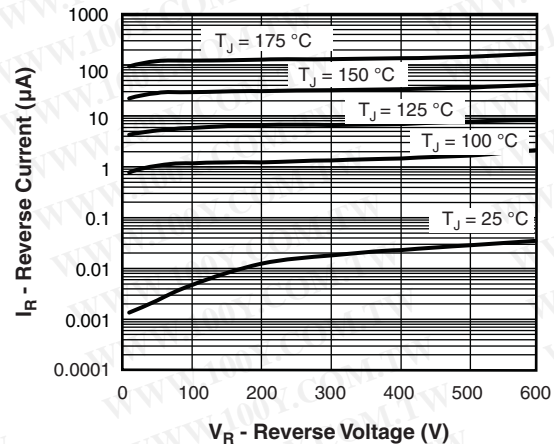


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage



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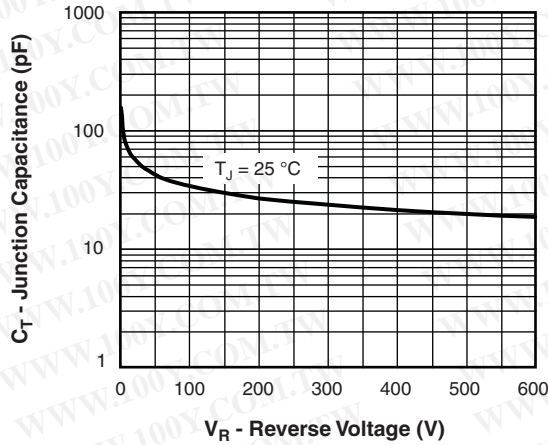


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

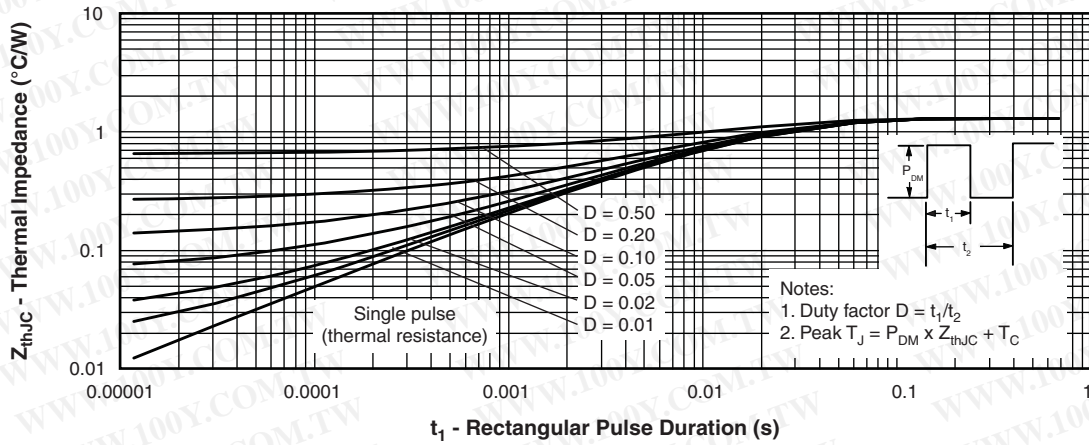


Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics

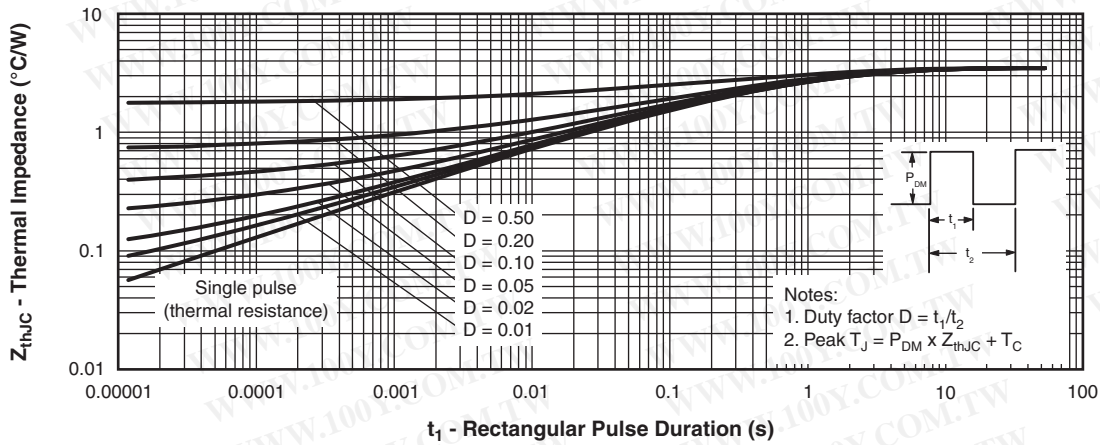


Fig. 5 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics (FULL-PAK)

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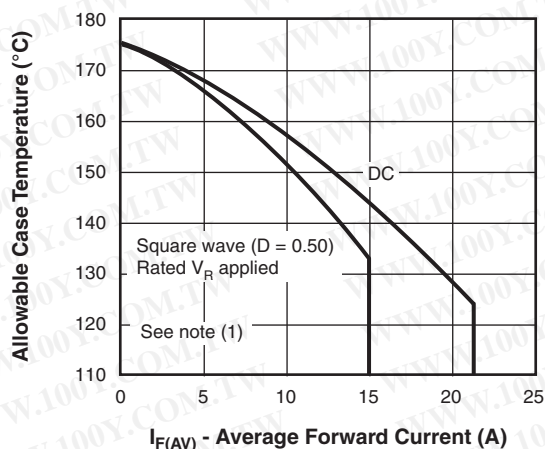


Fig. 6 - Maximum Allowable Case Temperature vs. Average Forward Current

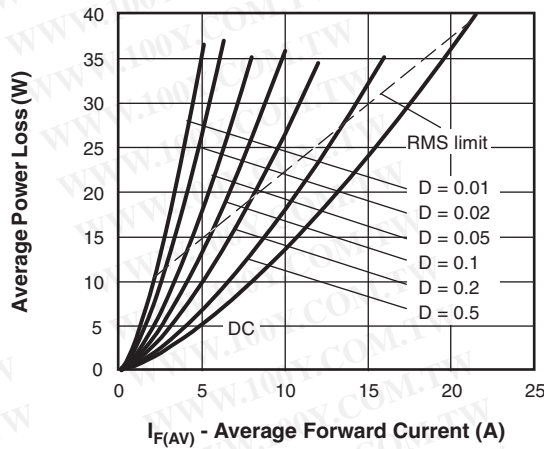


Fig. 8 - Forward Power Loss Characteristics

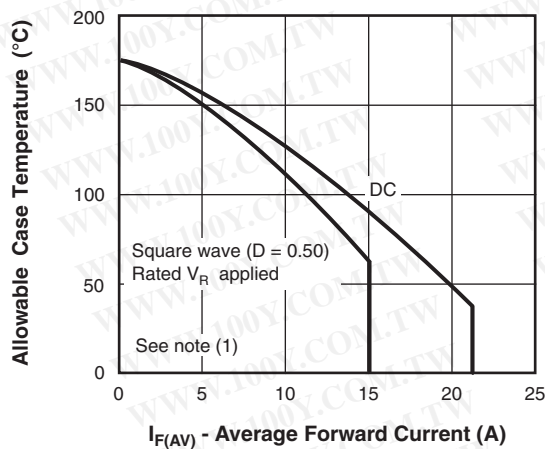


Fig. 7 - Maximum Allowable Case Temperature vs. Average Forward Current (FULL-PAK)

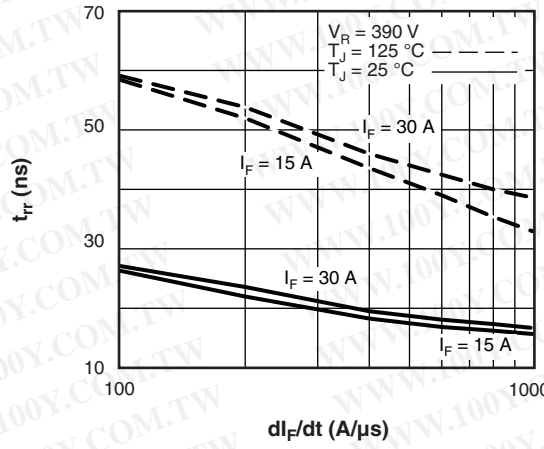


Fig. 9 - Typical Reverse Recovery Time vs.  $di_F/dt$

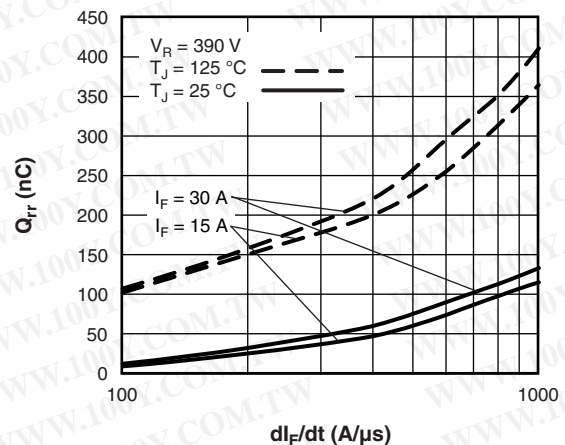


Fig. 10 - Typical Stored Charge vs.  $di_F/dt$

**Note**

(1) Formula used:  $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$ ;  
 $Pd$  = Forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 8);  $Pd_{REV}$  = Inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1}$  = Rated  $V_R$

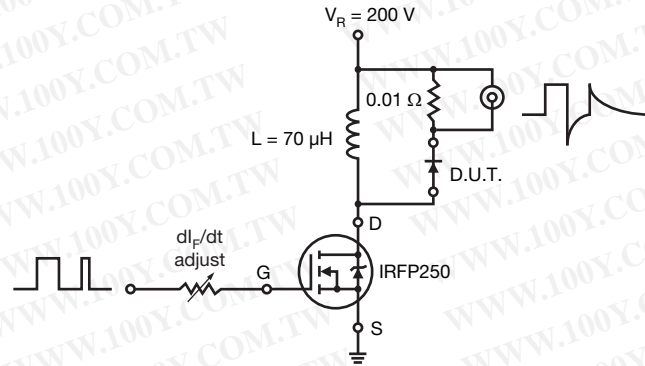
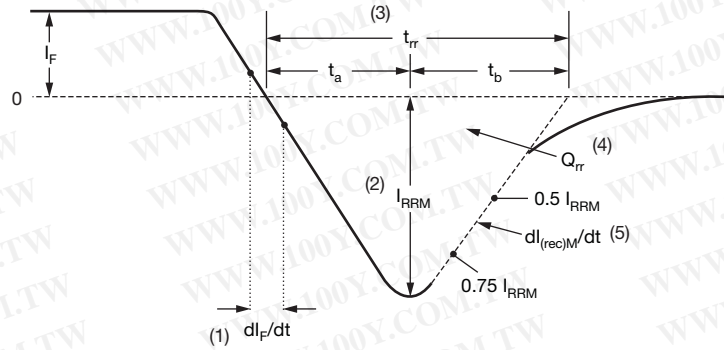


Fig. 11 - Reverse Recovery Parameter Test Circuit



(1)  $di_F/dt$  - rate of change of current through zero crossing

(2)  $I_{RRM}$  - peak reverse recovery current

(3)  $t_{rr}$  - reverse recovery time measured from zero crossing point of negative going  $I_F$  to point where a line passing through  $0.75 I_{RRM}$  and  $0.50 I_{RRM}$  extrapolated to zero current.

(4)  $Q_{rr}$  - area under curve defined by  $t_{rr}$  and  $I_{RRM}$

$$Q_{rr} = \frac{t_{rr} \times I_{RRM}}{2}$$

(5)  $di_{(rec)M}/dt$  - peak rate of change of current during  $t_b$  portion of  $t_{rr}$

Fig. 12 - Reverse Recovery Waveform and Definitions

# VS-15ETX06PbF, VS-15ETX06FPPbF

Vishay Semiconductors Ultrafast Rectifier, 15 A FRED Pt®



## ORDERING INFORMATION TABLE

Device code	<b>VS-</b>	<b>15</b>	<b>E</b>	<b>T</b>	<b>X</b>	<b>06</b>	<b>FP</b>	<b>PbF</b>
	①	②	③	④	⑤	⑥	⑦	⑧

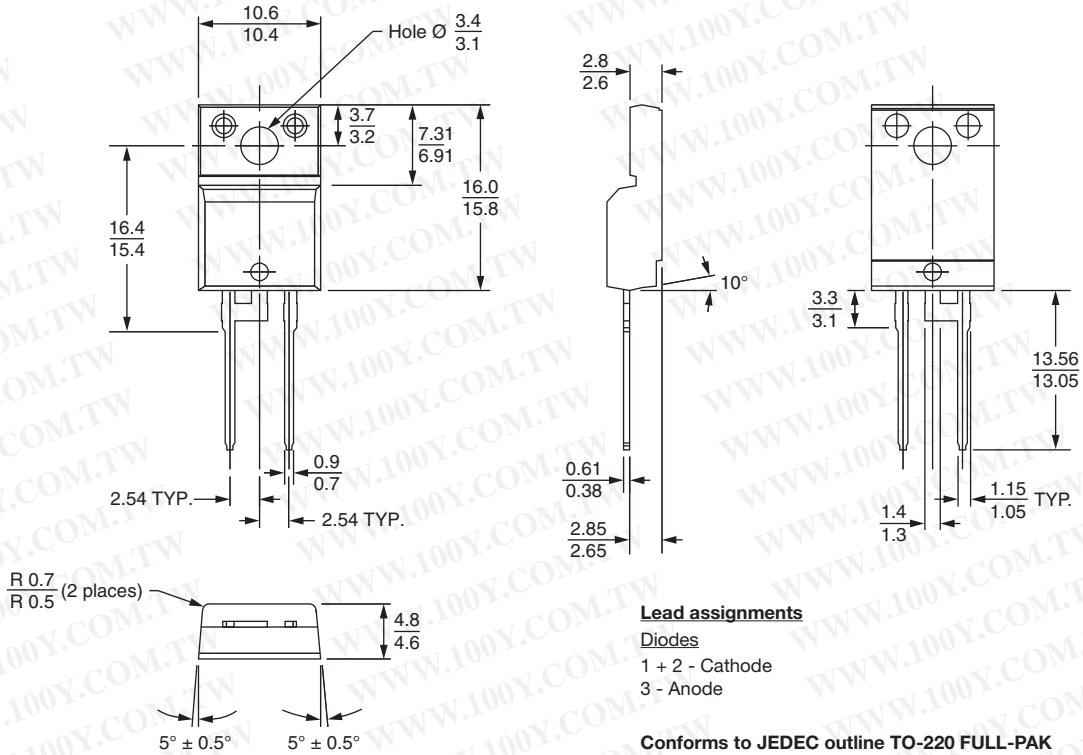
- 1** - Vishay Semiconductors product
- 2** - Current rating (15 = 15 A)
- 3** - E = Single diode
- 4** - T = TO-220, D<sup>2</sup>PAK
- 5** - X = Hyperfast recovery
- 6** - Voltage rating (06 = 600 V)
- 7** -
  - None = TO-220AC
  - FP = TO-220 FULL-PAK
- 8** - PbF = Lead (Pb)-free

Tube standard pack quantity: 50 pieces

LINKS TO RELATED DOCUMENTS		
Dimensions	TO-220AC	<a href="http://www.vishay.com/doc?95221">www.vishay.com/doc?95221</a>
	TO-220AC FULL-PAK	<a href="http://www.vishay.com/doc?95005">www.vishay.com/doc?95005</a>
Part marking information	TO-220AC	<a href="http://www.vishay.com/doc?95224">www.vishay.com/doc?95224</a>
	TO-220AC FULL-PAK	<a href="http://www.vishay.com/doc?95009">www.vishay.com/doc?95009</a>



**DIMENSIONS** in millimeters



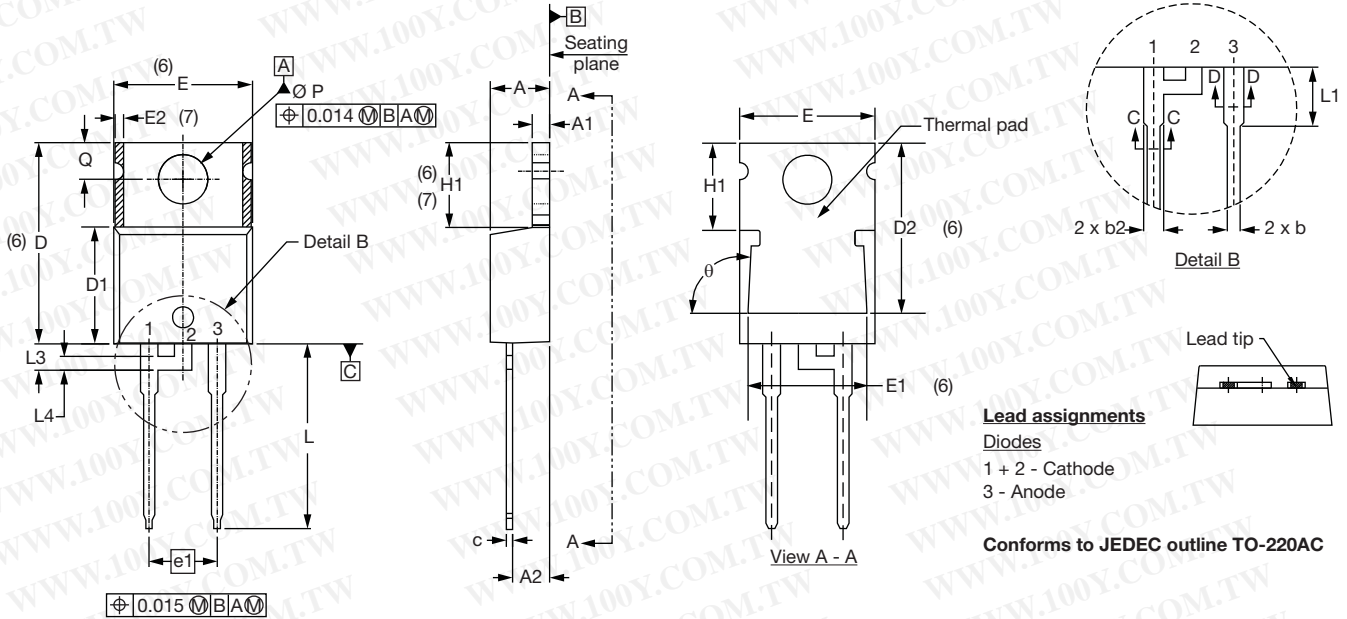
### Lead assignments

- Diodes
- 1 + 2 - Cathode
- 3 - Anode

Conforms to JEDEC outline TO-220 FULL-PAK

### TO-220AC

**DIMENSIONS** in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183		E1	6.86	8.89	0.270	0.350	6
A1	1.14	1.40	0.045	0.055		E2	-	0.76	-	0.030	7
A2	2.56	2.92	0.101	0.115		e	2.41	2.67	0.095	0.105	
b	0.69	1.01	0.027	0.040		e1	4.88	5.28	0.192	0.208	
b1	0.38	0.97	0.015	0.038	4	H1	6.09	6.48	0.240	0.255	6, 7
b2	1.20	1.73	0.047	0.068		L	13.52	14.02	0.532	0.552	
b3	1.14	1.73	0.045	0.068	4	L1	3.32	3.82	0.131	0.150	2
c	0.36	0.61	0.014	0.024		L3	1.78	2.13	0.070	0.084	
c1	0.36	0.56	0.014	0.022	4	L4	0.76	1.27	0.030	0.050	2
D	14.85	15.25	0.585	0.600	3	∅ P	3.54	3.73	0.139	0.147	
D1	8.38	9.02	0.330	0.355		Q	2.60	3.00	0.102	0.118	
D2	11.68	12.88	0.460	0.507	6	θ	90° to 93°		90° to 93°		
E	10.11	10.51	0.398	0.414	3, 6						

**Notes**

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline





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