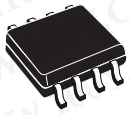
STSJ60NH3LL

N-channel 30V - 0.004Ω - 15A - PowerSO-8™ STripFET™ Power MOSFET for DC-DC conversion

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STSJ60NH3LL	30V	<0.0057Ω	15A (2)

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5 V
- Conduction losses reduced
- Improved junction-case thermal resistance
- Low threshold device

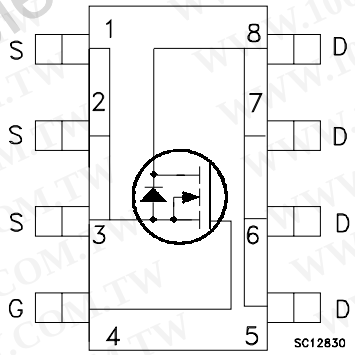


PowerSO-8™

Description

This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This process coupled to unique metallization techniques realizes the most advanced low voltage Power MOSFET in SO-8 ever produced. The exposed slug reduces the Rthj-c improving the current capability.

Internal schematic diagram



DRAIN CONTACT ALSO ON THE BACKSIDE

Application

- Switching application

Order code

Part number	Marking	Package	Packaging
STSJ60NH3LL	60H3LL-	PowerSO-8™	Tape & reel

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D (1)	Drain current (continuous) at T_C = 25°C	60	A
I_D	Drain current (continuous) at T_C = 100°C	37.5	A
I_D (2)	Drain current (continuous) at T_C = 25°C	15	A
I_D	Drain current (continuous) at T_C = 100°C	9.4	A
I_{DM} (3)	Drain current (pulsed)	60	A
P_{tot} (1)	Total dissipation at T_C = 25°C	50	W
P_{tot} (2)	Total dissipation at T_C = 25°C	3	W
T_{stg}	Storage temperature	-55 to 150	°C
Tj	Operating junction temperature		

1. This value is rated according to Rthj-c
2. This value is rated according to Rthj-pcb
3. Pulse width limited by safe operating area

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case (drain) Max	2.5	°C/W
Rthj-pcb	Thermal resistance junction-pcb Max	42	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 7.5A V_{GS} = 4.5V, I_D = 7.5A		0.004 0.005	0.0057 0.0075	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS}=25V, f=1MHz, V_{GS} = 0		1810 565 41		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15V, I_D=15A V_{GS}=4.5V (see Figure 13)		18 4.8 5.3	24	nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20mV open drain	0.5	1.5	3	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise Time	V_{DD} = 15V, I_D = 7.5A R_G = 4.7Ω, V_{GS} = 10V (see Figure 12)		8 65		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 15V, I_D = 7.5A R_G = 4.7Ω , V_{GS} = 10V (see Figure 12)		38 20		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				15 60	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 15A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15A, di/dt = 100A/µs V_{DD} = 15V, T_j = 25°C (see Figure 17)		22 32 1.9		ns nC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

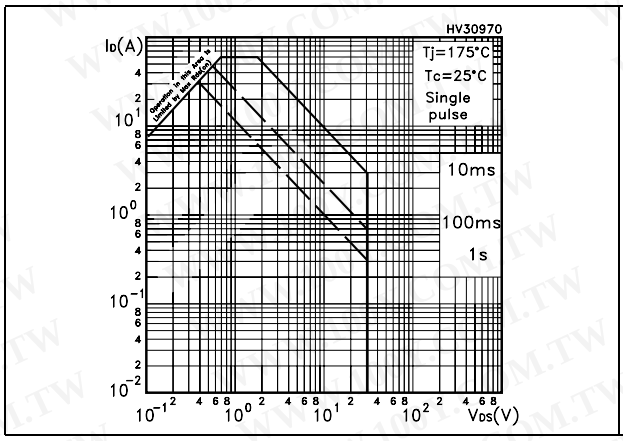


Figure 2. Thermal impedance

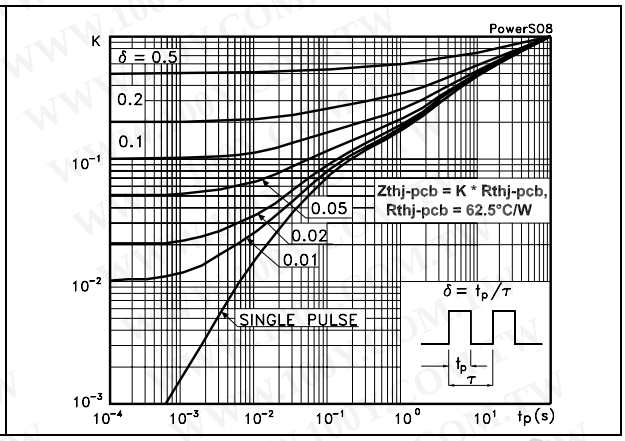


Figure 3. Output characteristics

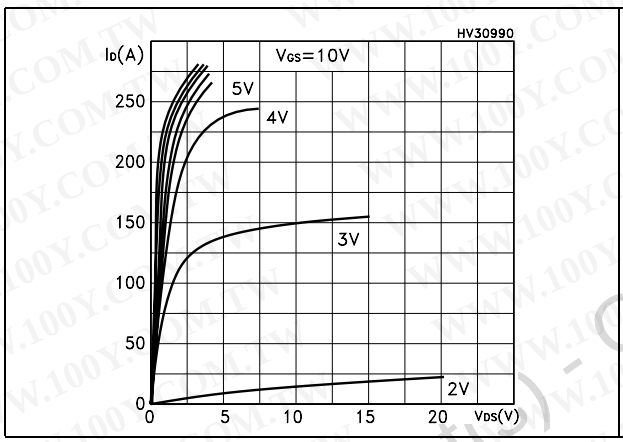


Figure 4. Transfer characteristics

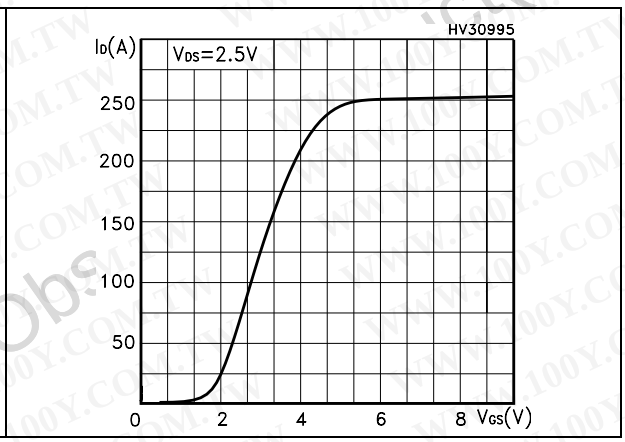


Figure 5. Normalized B_{VDSS} vs temperature

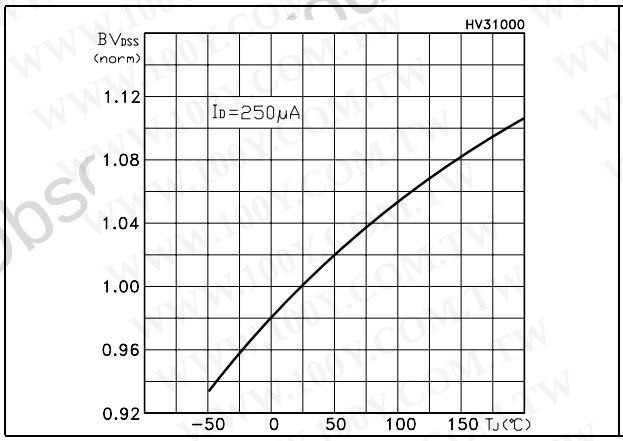


Figure 6. Static drain-source on resistance

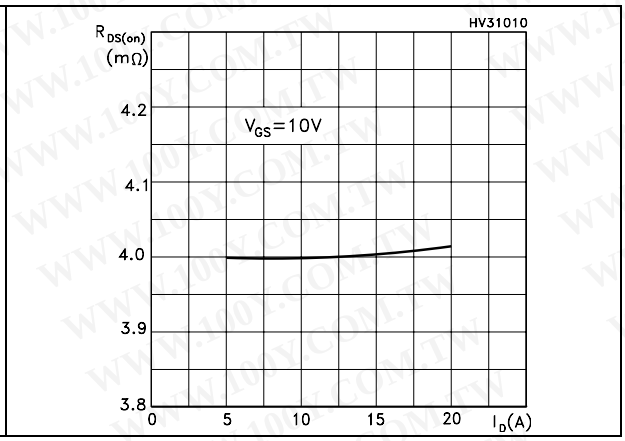


Figure 7. Gate charge vs gate-source voltage

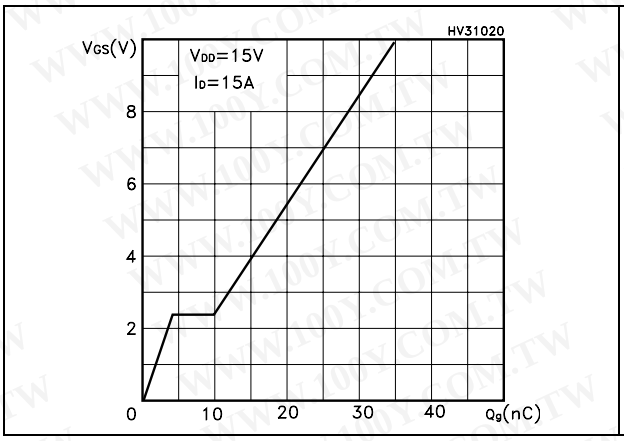


Figure 8. Capacitance variations

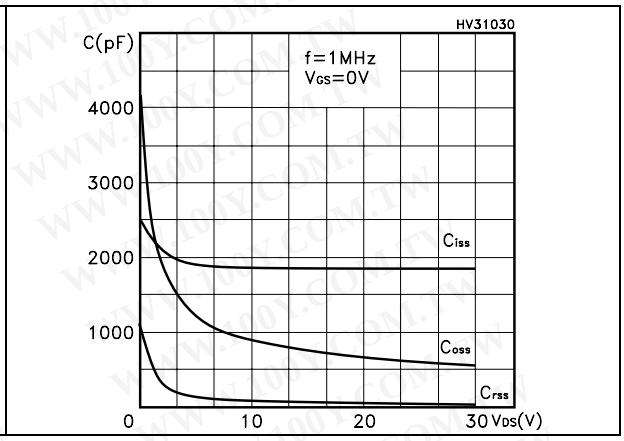


Figure 9. Normalized gate threshold voltage vs temperature

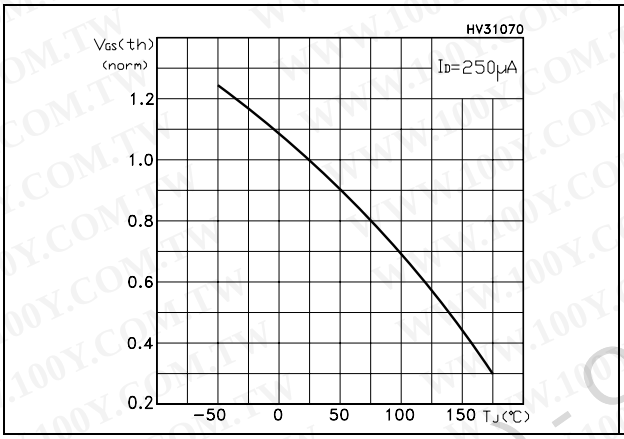


Figure 10. Normalized on resistance vs temperature

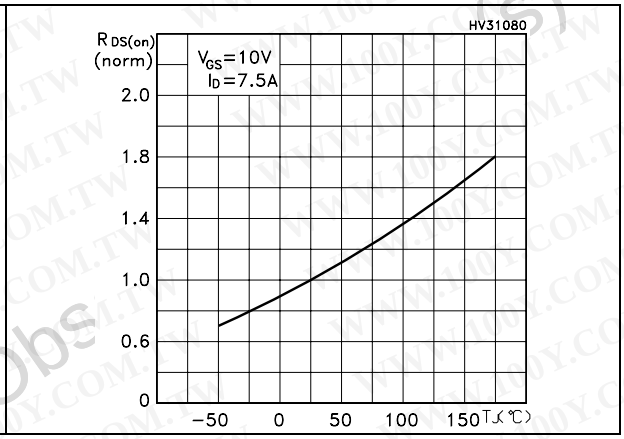
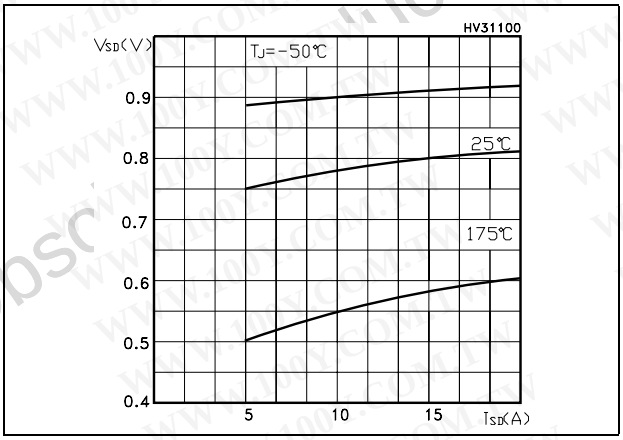


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

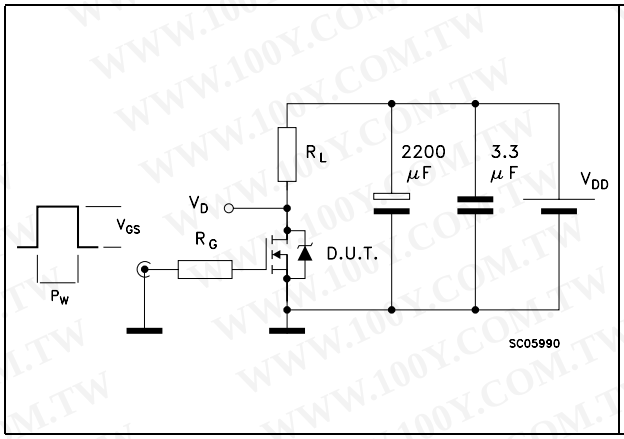


Figure 13. Gate charge test circuit

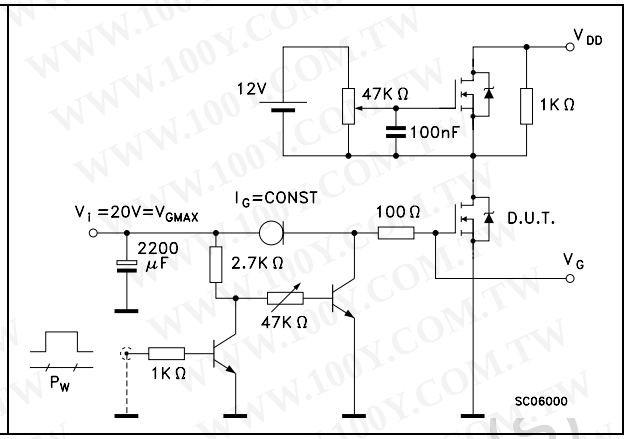


Figure 14. Test circuit for inductive load switching and diode recovery times

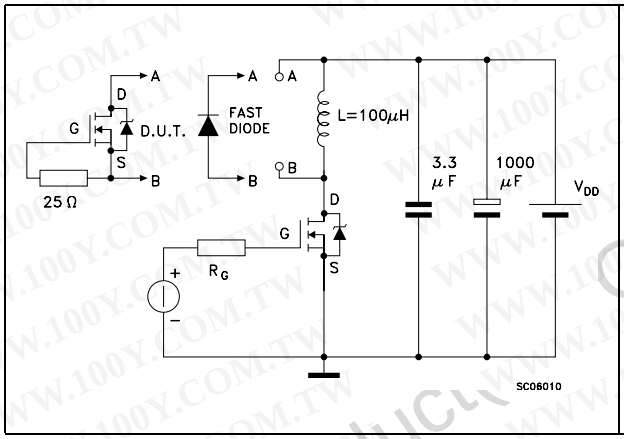


Figure 15. Unclamped inductive load test circuit

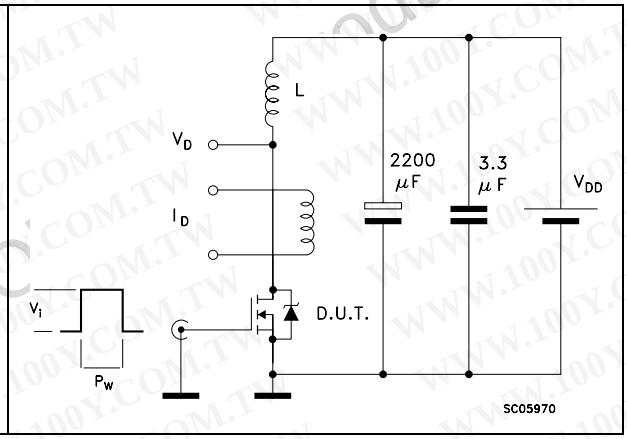


Figure 16. Unclamped inductive waveform

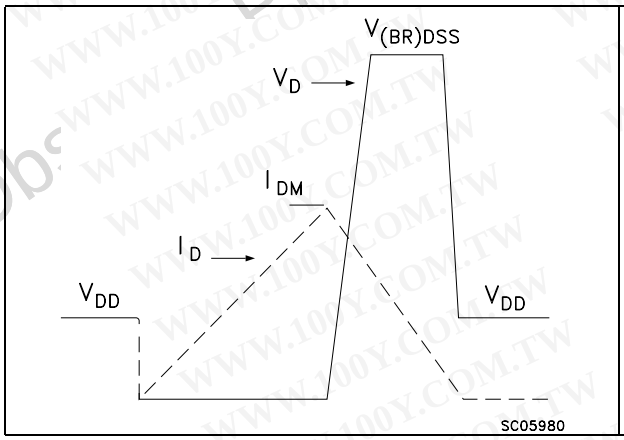
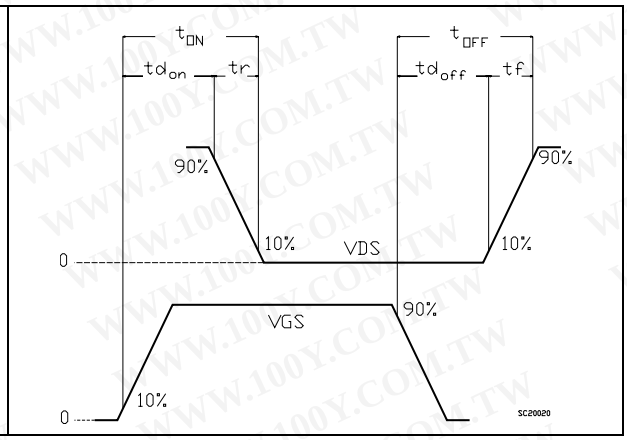


Figure 17. Switching time waveform

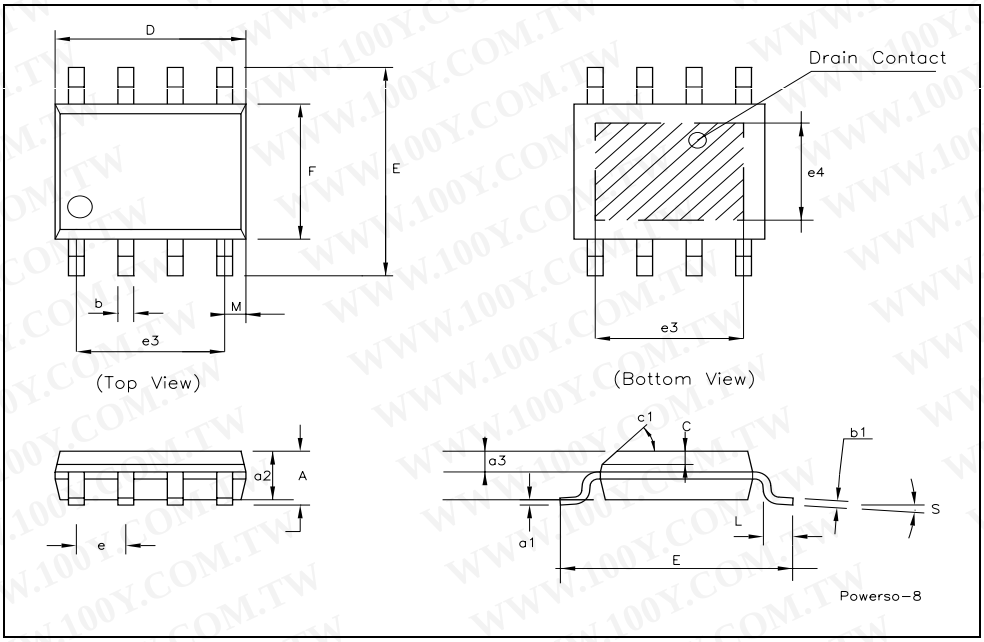


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerSO-8™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
12-Apr-2006	1	First release
17-May-2007	2	*Table 2* has been updated

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