# STW14NM50

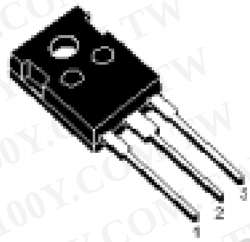
## N-CHANNEL 550V @ Tjmax - 0.32Ω - 14A TO-247 MDmesh™ MOSFET

**Table 1: General Features**

| TYPE | $V_{DSS}$ (@Tjmax) | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STW14NM50 | 550 V | < 0.35 Ω | 14 A |

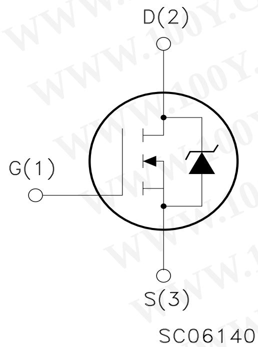
- TYPICAL $R_{DS}$(on) = 0.32 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE RATED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTORING YIELDS

**Figure 1: Package**




TO-247

**Figure 2: Internal Schematic Diagram**




### DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprierati strip technique yields overall dynamic performance that is significantly better than that of similar completition's products.

### APPLICATIONS

The MDmesh™ family is very suitablr for increase the power density of high vo tage converters allowing system miniaturization and higher efficiencies.

**Table 2: Order Codes**

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|---|---|---|---|
| STW14NM50 | W14NM50 | TO-247 | TUBE |

### Table 3: Absolute Maximum ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate- source Voltage | ±30 | V |
| $I_D$ | Drain Current (continuous) at $T_C$ = 25°C | 14 | A |
| $I_D$ | Drain Current (continuous) at $T_C$ = 100°C | 8.8 | A |
| $I_{DM}$ (1) | Drain Current (pulsed) | 56 | A |
| $P_{TOT}$ | Total Dissipation at $T_C$ = 25°C | 175 | W |
| | Derating Factor | 1.28 | W/°C |
| dv/dt | Peak Diode Recovery voltage slope | 6 | V/ns |
| $T_{stg}$ | Storage Temperature | –65 to 150 | °C |
| $T_j$ | Max. Operating Junction Temperature | 150 | °C |

(•)Pulse width limited by safe operating area
(*)Limited only by maximum temperature allowed
(1)$I_{SD}$ ≤14A, di/dt ≤100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

### Table 4: Thermal Data

| | | | |
|---|---|---|---|
| Rthj-case | Thermal Resistance Junction-case Max | 0.715 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 30 | °C/W |
| $T_l$ | Maximum Lead Temperature For Soldering Purpose | 300 | °C |

### Table 5: Avalanche Characteristics

| Symbol | Parameter | Max Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max) | 12 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 400 | mJ |

**ELECTRICAL CHARACTERISTICS** ($T_{CASE}$ =25°C UNLESS OTHERWISE SPECIFIED)

### Table 6: On /Off

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D$ = 250 µA, $V_{GS}$ = 0 | 500 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current ($V_{GS}$ = 0) | $V_{DS}$ = Max Rating<br>$V_{DS}$ = Max Rating, $T_C$ = 125°C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body Leakage Current ($V_{DS}$ = 0) | $V_{GS}$ = ± 30 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on}$ | Static Drain-source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 6 A | | 0.32 | 0.35 | Ω |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

### Table 7: Dynamic

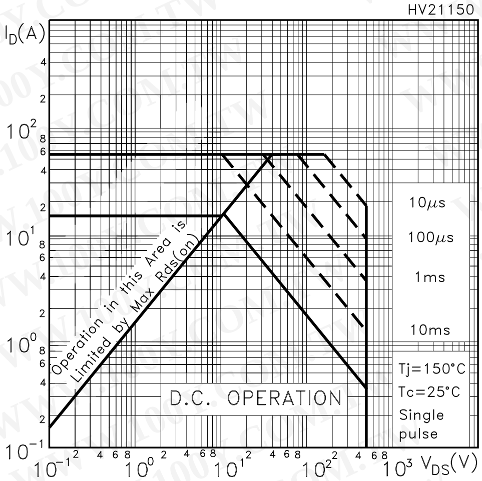
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward Transconductance | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D$ = 6A | | 5.2 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input Capacitance<br>Output Capacitance<br>Reverse Transfer Capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 | | 1000<br>180<br>25 | | pF<br>pF<br>pF |
| $C_{OSS\ eq}$ (3). | Equivalent Output Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 400 V | | 90 | | pF |
| $R_G$ | Gate Input Resistance | f=1 MHz Gate DC Bias = 0<br>Test Signal Level = 20mV<br>Open Drain | | 1.6 | | Ω |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on Delay Time<br>Rise Time<br>Turn-off-Delay Time<br>Fall Time | $V_{DD}$ = 250 V, $I_D$ = 6 A,<br>$R_G$ = 4.7 Ω, $V_{GS}$ = 10 V<br>(see Figure 15) | | 20<br>10<br>19<br>8 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge | $V_{DD}$ = 400 V, $I_D$ = 12 A,<br>$V_{GS}$ = 10 V<br>(see Figure 18) | | 28<br>8<br>15 | 38 | nC<br>nC<br>nC |

### Table 8: Source Drain Diode

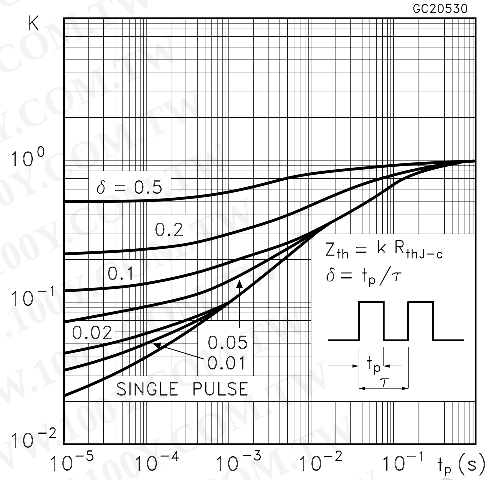
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (2) | Source-drain Current<br>Source-drain Current (pulsed) | | | | 14<br>56 | A<br>A |
| $V_{SD}$ (1) | Forward On Voltage | $I_{SD}$ = 12 A, $V_{GS}$ = 0 | | | 1.5 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 12 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100V<br>(see Figure 16) | | 270<br>2.23<br>16.5 | | ns<br>µC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 12 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100V, $T_j$ = 150°C<br>(see Figure 16) | | 340<br>3<br>18 | | ns<br>µC<br>A |

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

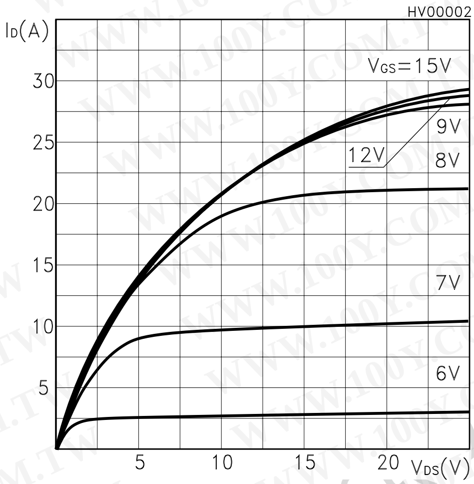
### Figure 3: Safe Operating Area



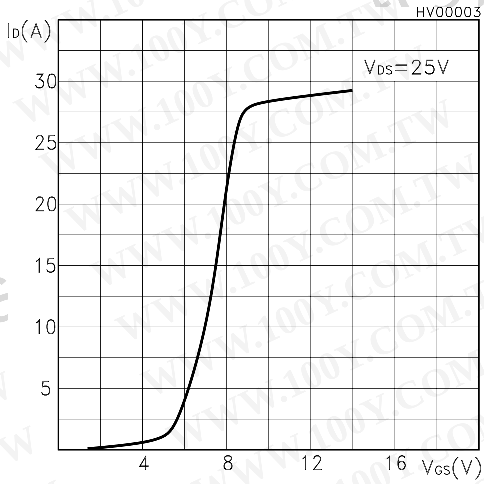

### Figure 6: Thermal Impedance



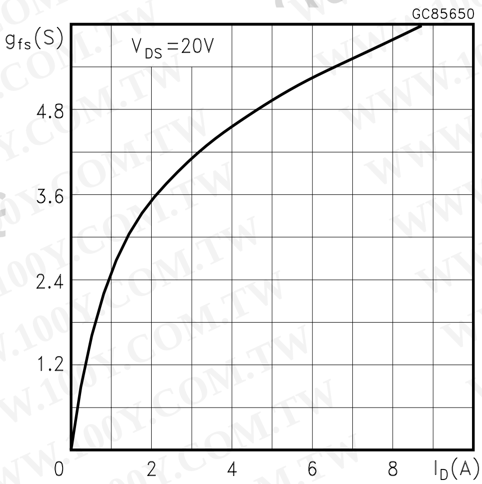

### Figure 4: Output Characteristics




### Figure 7: Transfer Characteristics




### Figure 5: Transconductance




### Figure 8: Static Drain-source On Resistance

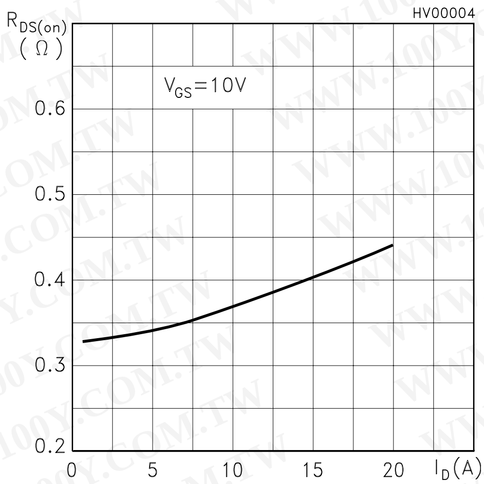


**Figure 9: Gate Charge vs Gate-source Voltage**

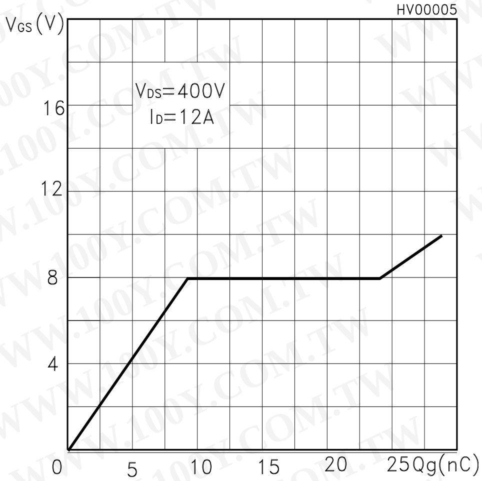



**Figure 12: Capacitance Variations**

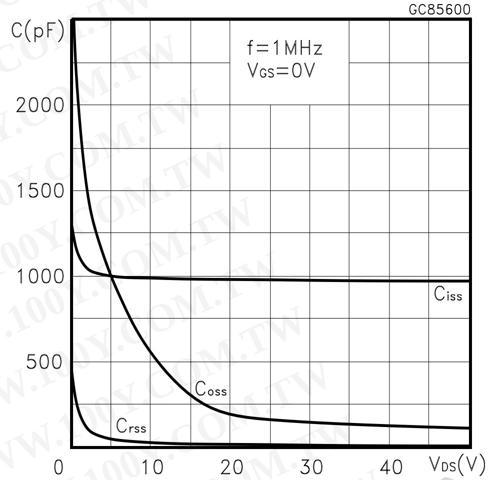



**Figure 10: Normalized Gate Thereshold Voltage vs Temperature**

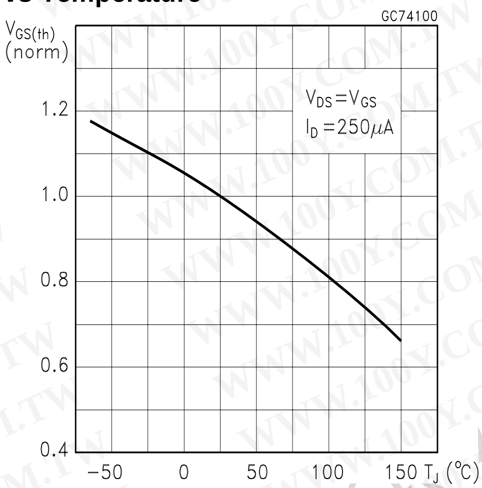



**Figure 13: Normalized On Resistance vs Temperature**

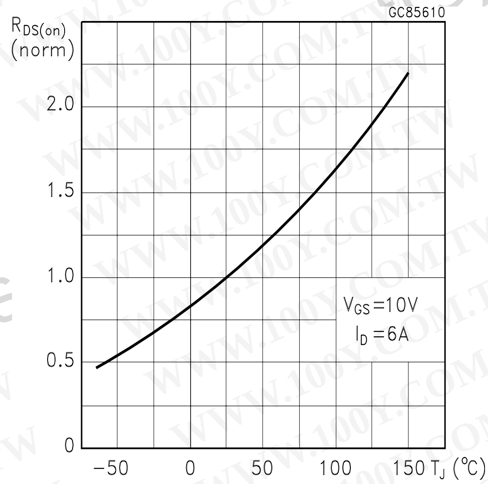



**Figure 11: Dource-Drain Diode Forward Characteristics**

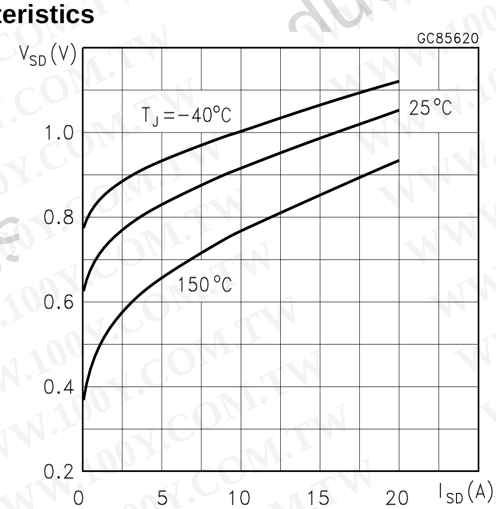


**Figure 14: Unclamped Inductive Load Test Circuit**

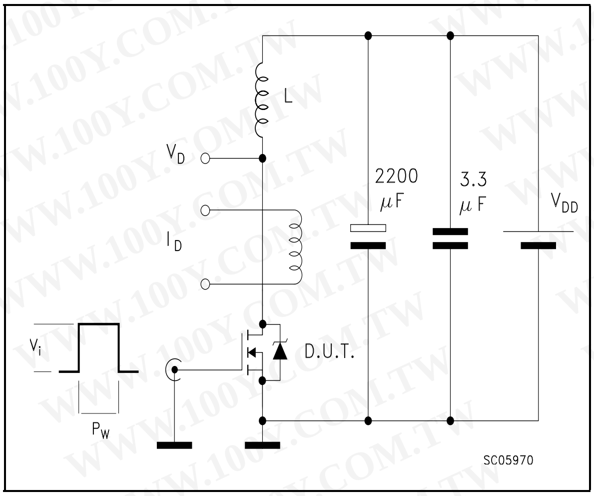



**Figure 17: Unclamped Inductive Wafeform**

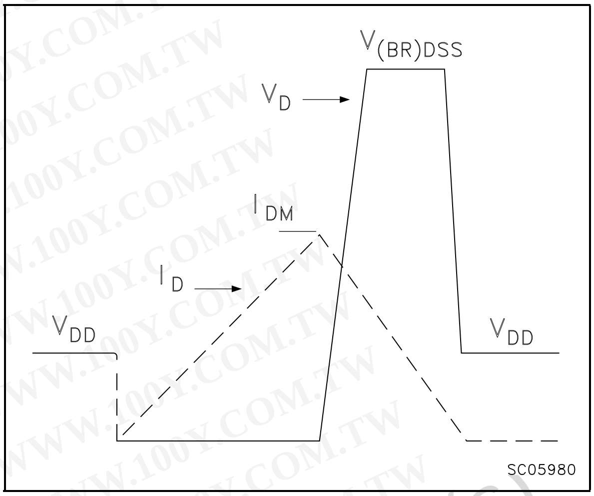



**Figure 15: Switching Times Test Circuit For Resistive Load**

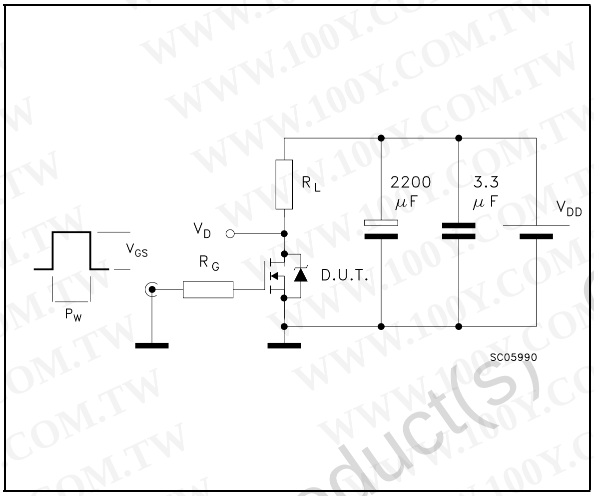



**Figure 18: Gate Charge Test Circuit**

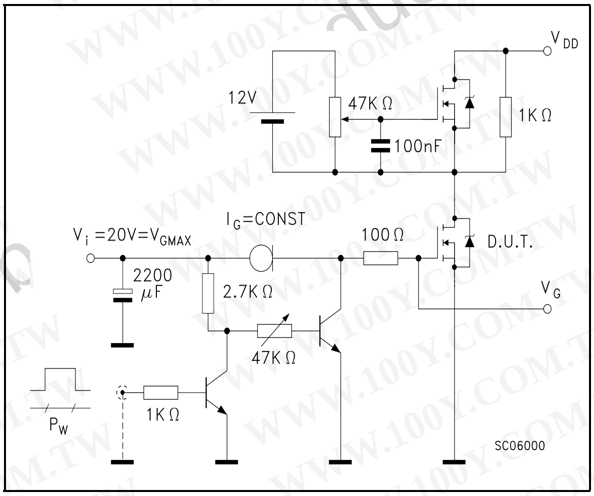
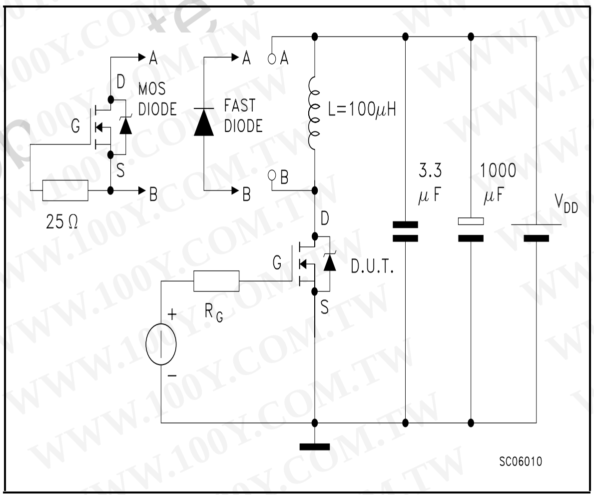



**Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times**



## TO-247 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.85 | | 5.15 | 0.19 | | 0.20 |
| A1 | 2.20 | | 2.60 | 0.086 | | 0.102 |
| b | 1.0 | | 1.40 | 0.039 | | 0.055 |
| b1 | 2.0 | | 2.40 | 0.079 | | 0.094 |
| b2 | 3.0 | | 3.40 | 0.118 | | 0.134 |
| c | 0.40 | | 0.80 | 0.015 | | 0.03 |
| D | 19.85 | | 20.15 | 0.781 | | 0.793 |
| E | 15.45 | | 15.75 | 0.608 | | 0.620 |
| e | | 5.45 | | | 0.214 | |
| L | 14.20 | | 14.80 | 0.560 | | 0.582 |
| L1 | 3.70 | | 4.30 | 0.14 | | 0.17 |
| L2 | | 18.50 | | | 0.728 | |
| øP | 3.55 | | 3.65 | 0.140 | | 0.143 |
| øR | 4.50 | | 5.50 | 0.177 | | 0.216 |
| S | | 5.50 | | | 0.216 | |

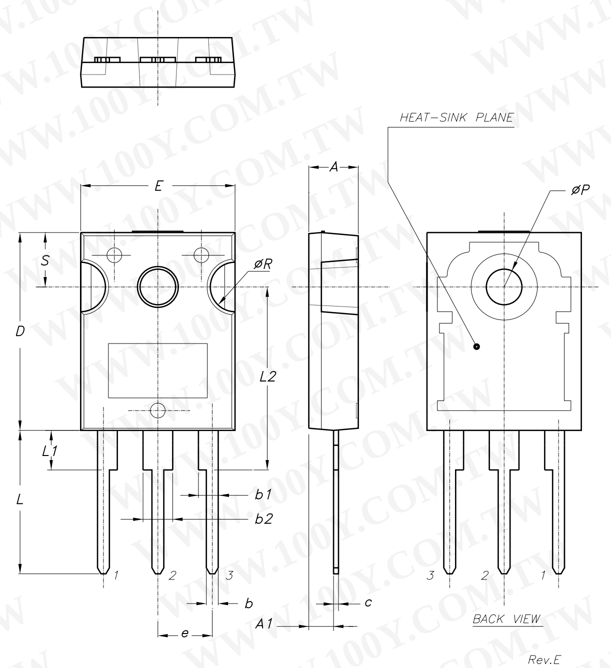


**Table 9: Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 05-July-2004 | 5 | The document change from “PRELIMINARY” to “COMPLETE”.<br>New Stylesheet. |