

## STW28NK60Z

# N-CHANNEL 600 V - 0.155∏ - 27A TO-247 Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	l <sub>D</sub>	Pw
STW28NK60Z	600 V	< 0.185 П	27 A	350 W

- TYPICAL  $R_{DS}(on) = 0.155 \Pi$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

#### **DESCRIPTION**

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high vltage MOSFETs including revolutionary MSmesh™ products.

#### **APPLICATIONS**

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES
- WELDING MACHINES
- LIGHTING

Figure 1: Package

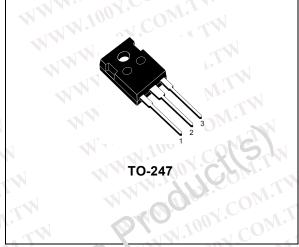


Figure 2: Internal Schematic Diagram

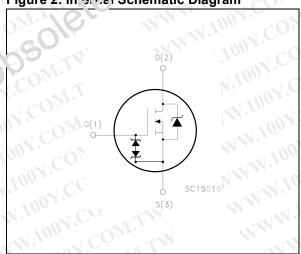


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STW28NK60Z	W28NK60Z	TO-247	TUBE

勝 特 力 材 料 886-3-5753170 胜特力电子(上海) 86-21-34970699 胜特力电子(深圳) 86-755-83298787 Http://www.100y.com.tw

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**Table 3: Absolute Maximum ratings** 

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
$V_{DGR}$	Drain-gate Voltage (R <sub>GS</sub> = 20 KΠ ,	600	V
V <sub>GS</sub>	Gate- source Voltage	⇔30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	27	Α
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	100	Α
I <sub>DM</sub> (*)	Drain Current (pulsed)	108	Α
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	350	W
	Derating Factor	2.77	W/°C
V <sub>ESD(G-S)</sub>	Gate source ESD (HBM-C = 100pF, R = 1.5 KΠ ,	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T <sub>stg</sub> T <sub>j</sub>	Storage Temperature Operating Junction Temperature	-55 to 150	°C

<sup>(\*)</sup> Pulse width limited by safe operating area

#### **Table 4: Thermal Data**

Rthj-case	Thermal Resistance Junction-case Max	0.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W
CTi	Maximum Lead Temperature For Soldering Purpose	300	)∨•°C

#### Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	27	A.C.
Eas	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 50$ V)	500	mJ

#### Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Condition	Min.	Тур.	Max	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown	Igs= ⇔1mA (Open Drain)	30			Α
	Voltage				-1	

#### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2/10

<sup>(1)</sup> I<sub>SD</sub> & 27 A, di/dt & 200 A/µs, VDD & V(BR)DSS, TJ & TJMAX

TABLE 7: ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			S
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125°C	N.CO	N.TW	1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V	OON.CC	OM.T	± 10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150 μA	103	3.75	4.5	V
R <sub>DS(on</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.5 A	N.1007	0.155	0.185	П

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 13.5 A		26	39/	S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	MAN	6350 615 125	41.CO	pF pF pF
$t_{ m d(on)} \ t_{ m r} \ t_{ m d(off)} \ t_{ m f}$	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD}$ = 300 V, $I_D$ = 14 A, $R_G$ = 4.7 $\Pi$ ( $V_{GS}$ = 10 V (Resistive Load see Figure 17))	S W	50 45 135 32	100Y	ns ns ns ns
$egin{array}{c} Q_{g} \ Q_{gs} \ Q_{gd} \end{array}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 28 A, V <sub>GS</sub> = 10 V		189 34 103	264	nC nC nC

#### **Table 9: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Uni
I <sub>SD</sub> I <sub>SDM</sub> (2)	Source-drain Current Source-drain Current (pulsed)	MM M 100X COM	TW	4	27 108	A
V <sub>SD</sub> (1)	Forward On Voltage	I <sub>SD</sub> = 27 A, V <sub>GS</sub> = 0			1.6	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 28 A, di/dt = 100 A/ $\mu$ s $V_{DD}$ = 35V, $T_j$ = 25°C (see test circuit Figure 5)	OM.T	820 10 23.5	W.	ns μC A
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 28 A, di/dt = 100 A/ $\mu$ s $V_{DD}$ = 35V, $T_j$ = 150°C (see test circuit Figure 5)	COM	1020 14 27.5		ns μC Α

<sup>(1)</sup> Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

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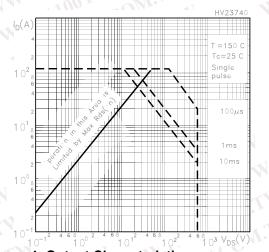
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WWW.100Y.COM.TW (2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area



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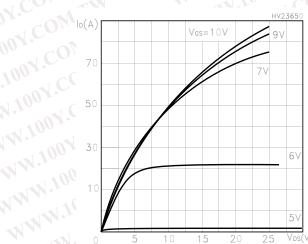


Figure 5: Transconductance

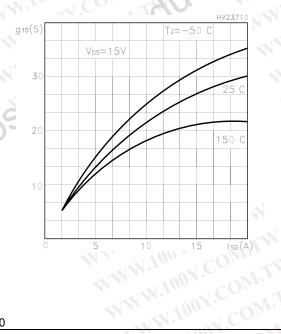
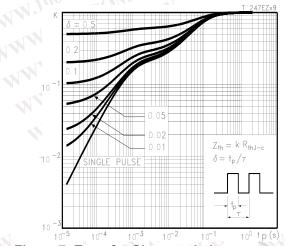
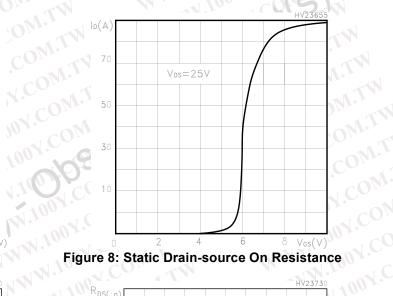
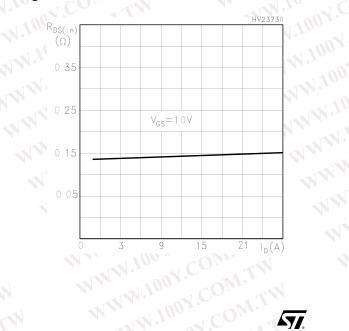


Figure 6: Thermal Impedance



**Figure 7: Transfer Characteristics** 





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Figure 9: Gate Charge vs Gate-source Voltage

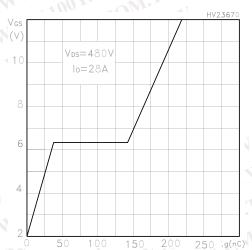


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

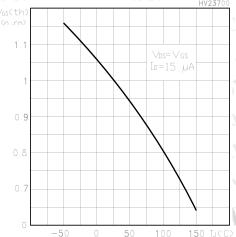
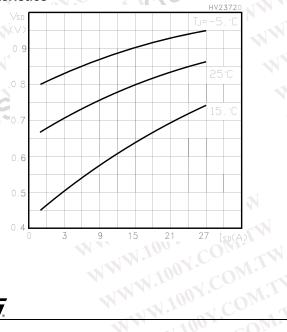


Figure 11: Source-Drain Diode Forward Characteristics



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\*1 100 Y.CO

Figure 12: Capacitance Variations

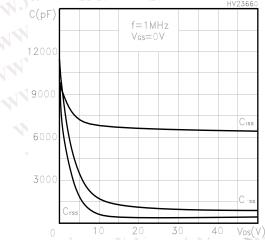


Figure 13: Normalized On Resistance vs Temperature

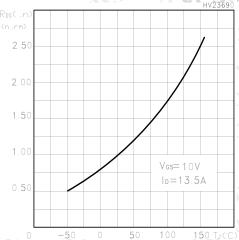
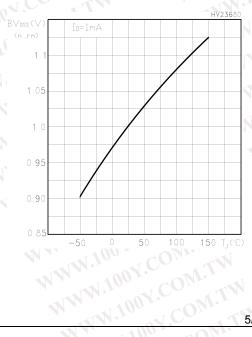


Figure 14: Normalized BV<sub>DSS</sub> vs Temperature



\*1 100 Y.CO

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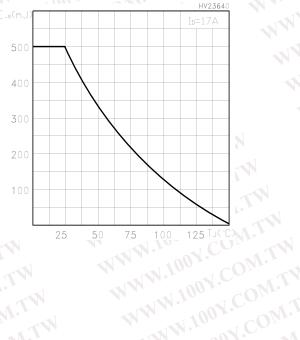
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Figure 16: Unclamped Inductive Load Test Cir-

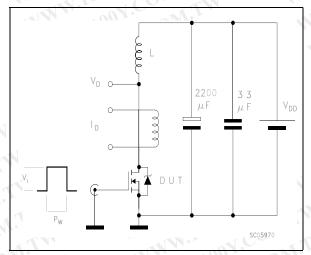


Figure 17: Switching Times Test Circuit For **Resistive Load** 

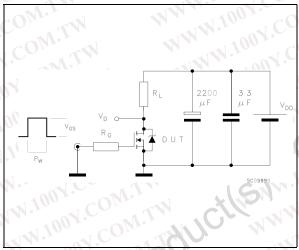


Figure 18: Test Circuit For Inductive Load **Switching and Diode Recovery Times** 

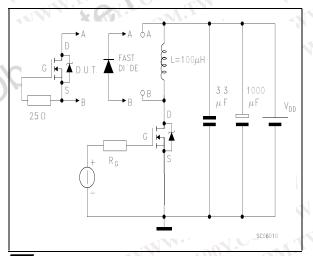


Figure 19: Unclamped Inductive Wafeform

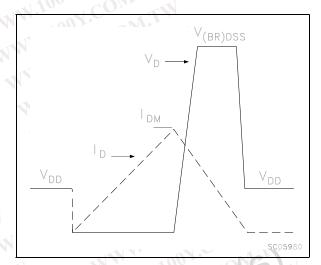
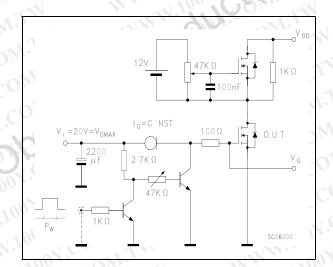


Figure 20: Gate Charge Test Circuit

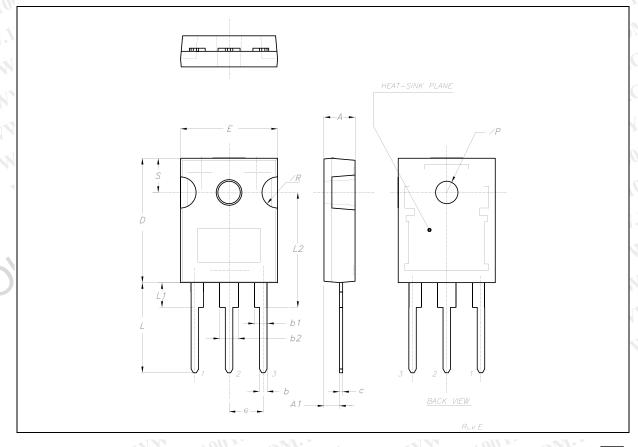


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### **TO-247 MECHANICAL DATA**

DIM.		mm.			inch	
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
С	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
Е	15.45		15.75	0.608		0.620
е		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øΡ	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



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Table 10: Revision History

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Table 10: Revision	History Revision	MMM	Description of Changes	
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