



STW29NK50Z

N-CHANNEL 500 V - 0.105Ω - 31A TO-247 Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DS}	R _{DS(on)}	I _D	P _W
STW29NK50Z	500 V	< 0.13 Ω	31 A	350 W

- TYPICAL R_{DS(on)} = 0.105 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high vltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES
- WELDING MACHINES
- LIGHTING

Figure 1: Package

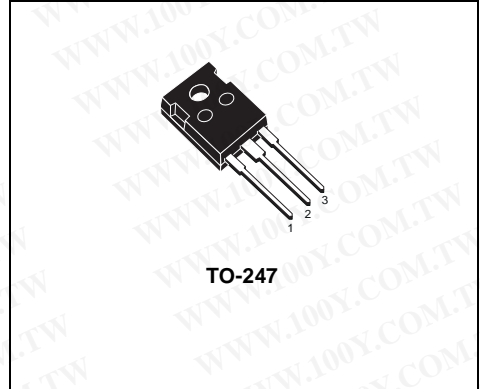


Figure 2: Internal Schematic Diagram

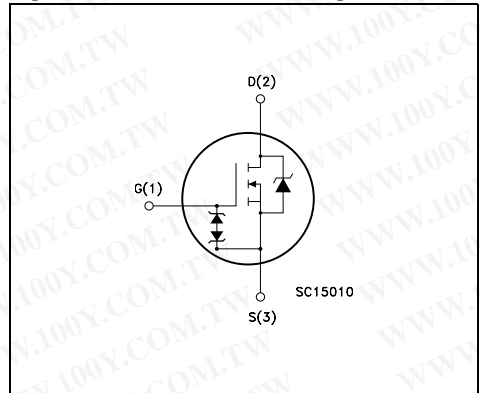


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STW29NK50Z	W29NK50Z	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	500	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ K}\Omega$)	500	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	31	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	19.5	A
$I_{DM} (*)$	Drain Current (pulsed)	124	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	350	W
	Derating Factor	2.77	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100pF, R = 1.5 K Ω)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_{stg} T_J	Storage Temperature Operating Junction Temperature	-55 to 150	°C

(*) Pulse width limited by safe operating area

(1) $I_{SD} \leq 31\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	50	°C/W
T_I	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_J max)	31	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	550	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{ mA}$ (Open Drain)	30			A

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

TABLE 7: ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	500			S
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 150 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 15.5 \text{ A}$		0.105	0.13	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 15.5 \text{ A}$		24		S
C_{iss} C_{oss} C_{riss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		6110 697 166		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 250 \text{ V}, I_D = 15 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see Figure 17)		44.5 41 129 33		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 \text{ V}, I_D = 30 \text{ A},$ $V_{GS} = 10 \text{ V}$		190 35.5 111	266	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				31	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				124	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 31 \text{ A}, V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 30 \text{ A}, di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 44.8 \text{ V}, T_j = 25^{\circ}C$ (see test circuit Figure 5)		436 6.1 28		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 30 \text{ A}, di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 44.8 \text{ V}, T_j = 150^{\circ}C$ (see test circuit Figure 5)		500 7.5 30		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

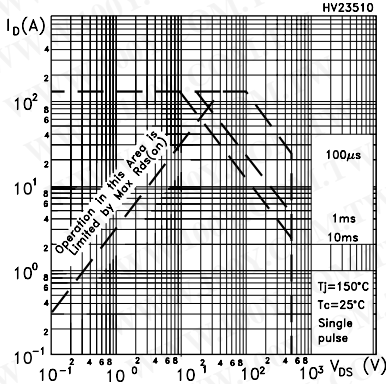


Figure 4: Output Characteristics

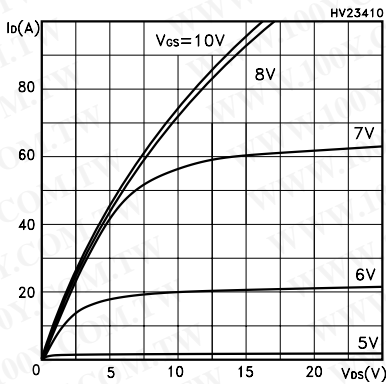


Figure 5: Transconductance

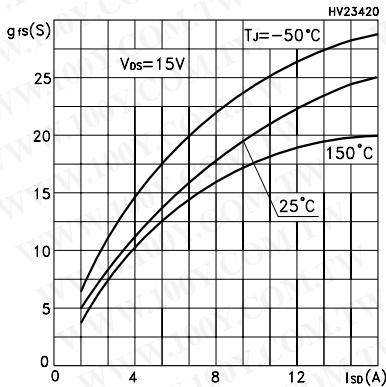


Figure 6: Thermal Impedance

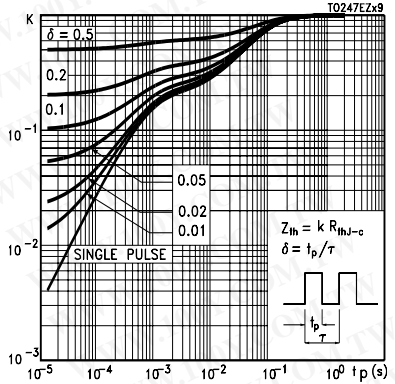


Figure 7: Transfer Characteristics

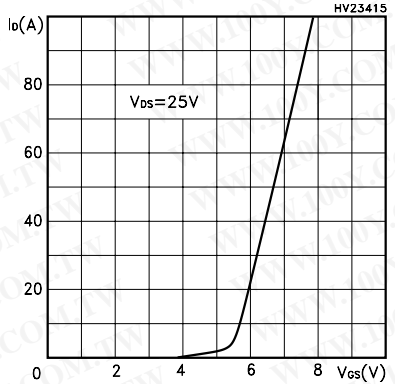


Figure 8: Static Drain-source On Resistance

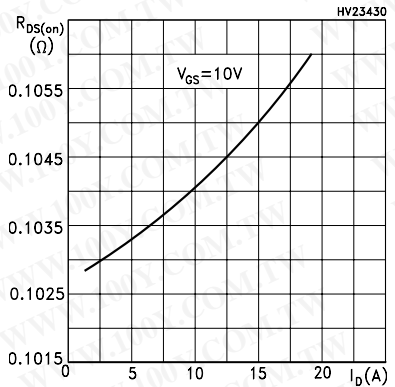


Figure 9: Gate Charge vs Gate-source Voltage

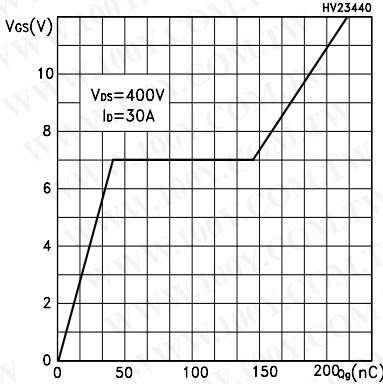


Figure 10: Normalized Gate Threshold Voltage vs Temperature

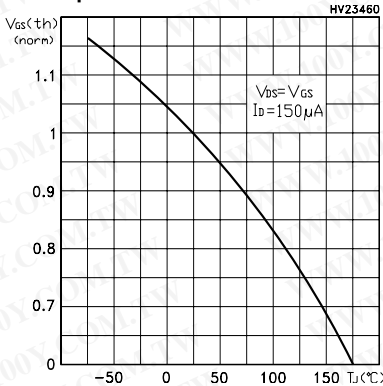


Figure 11: Dource-Drain Diode Forward Characteristics

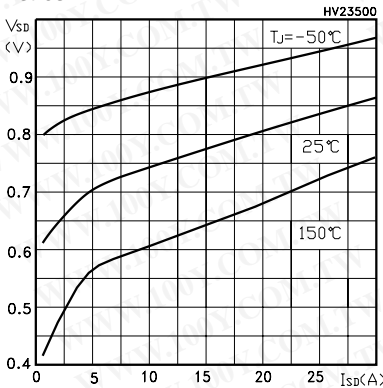


Figure 12: Capacitance Variations

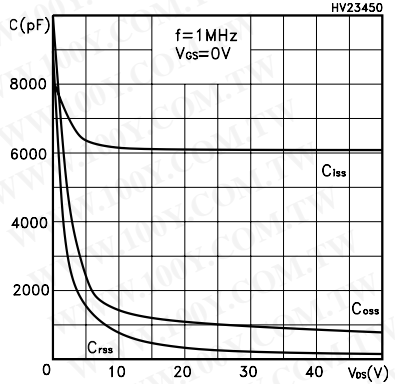


Figure 13: Normalized On Resistance vs Temperature

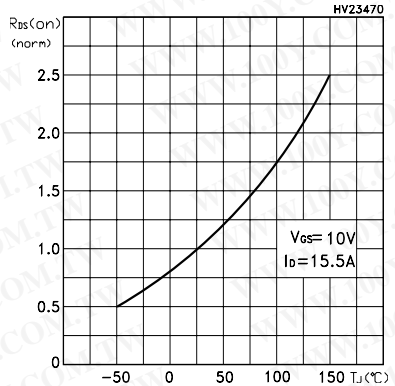


Figure 14: Normalized BV_{DSS} vs Temperature

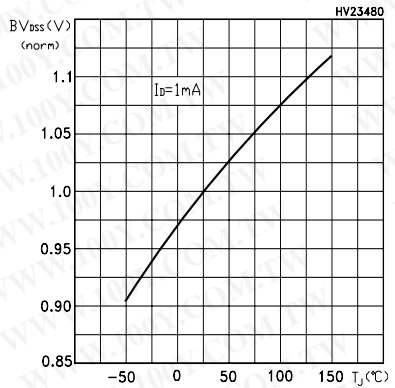


Figure 15: Maximum Avalanche Energy vs Temperature

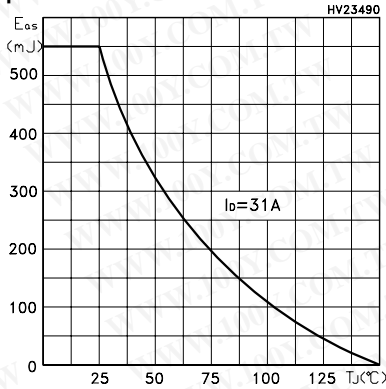


Figure 16: Unclamped Inductive Load Test Circuit

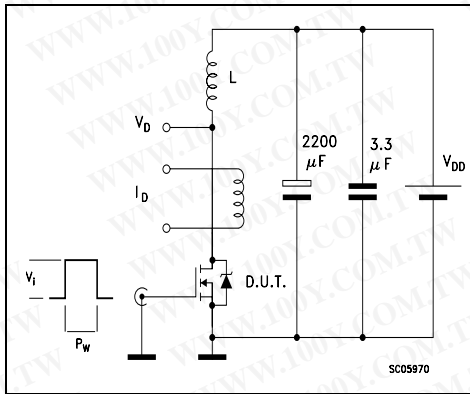


Figure 17: Switching Times Test Circuit For Resistive Load

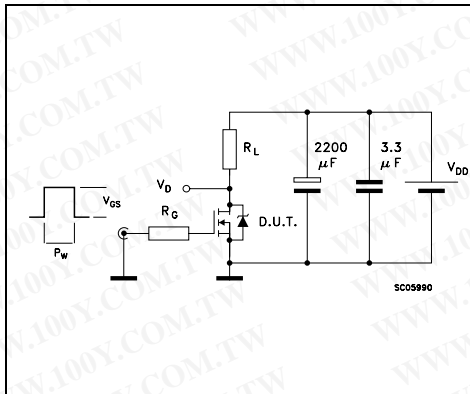


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

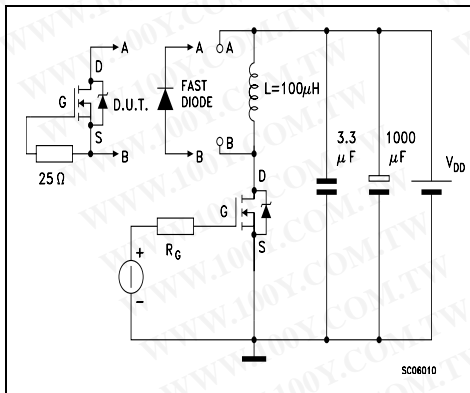


Figure 19: Unclamped Inductive Waferform

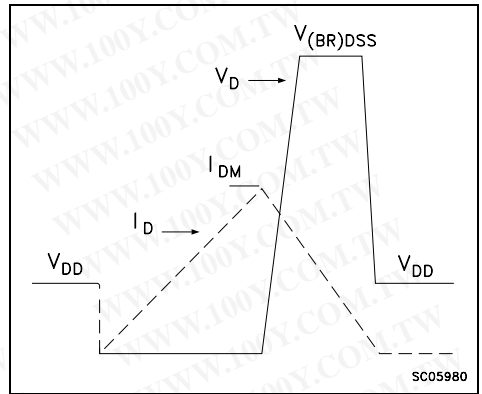
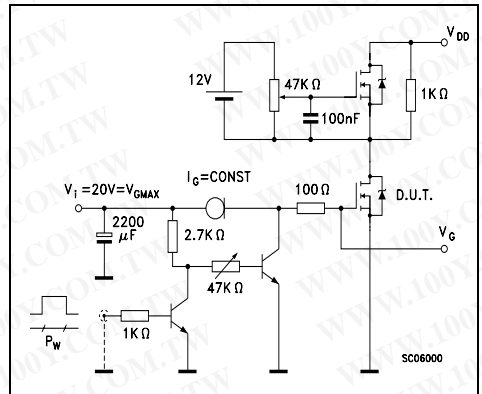
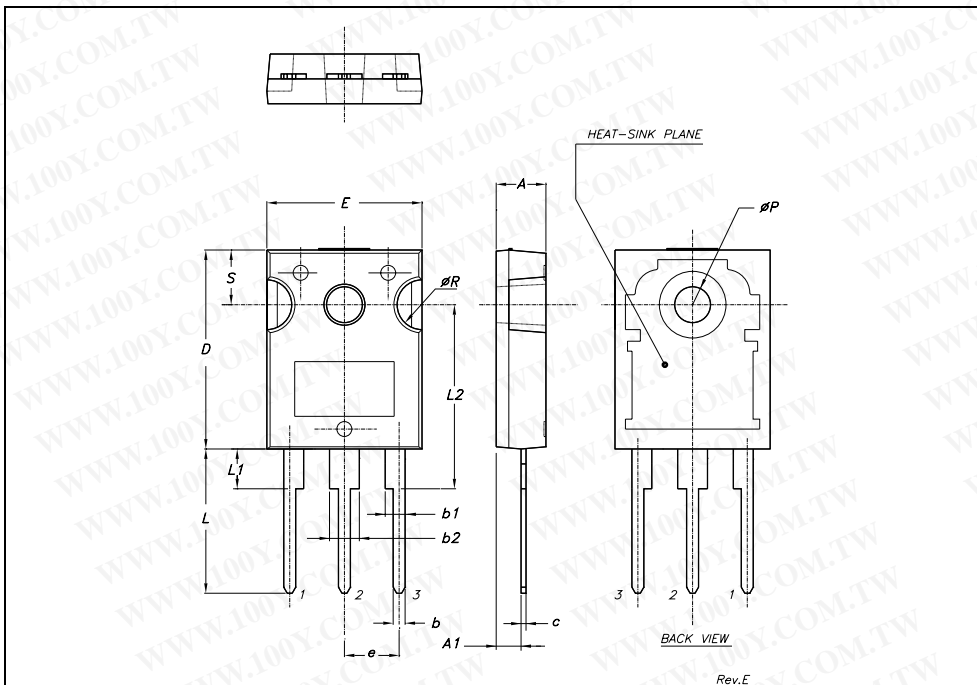


Figure 20: Gate Charge Test Circuit



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



Rev.E

Table 10: Revision History

Date	Revision	Description of Changes
19-Oct-2004	1	First Release.

勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

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