



## STY60NM60

### N-CHANNEL 600V - 0.050Ω - 60A Max247 Zener-Protected MDmesh™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STY60NM60	600V	< 0.055Ω	60 A

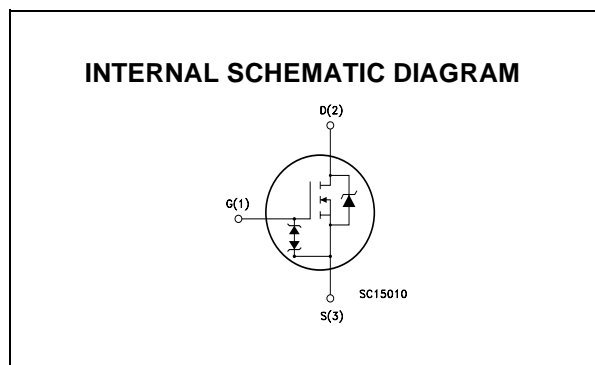
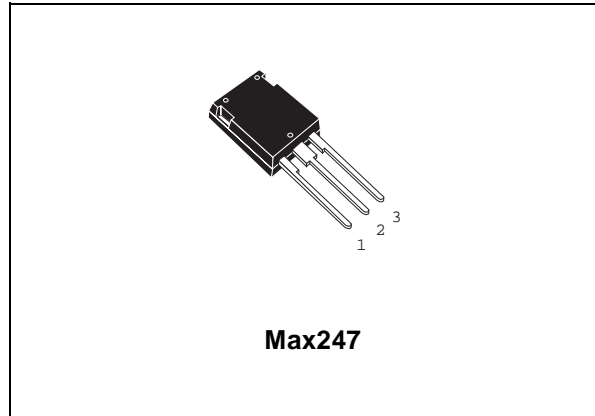
- TYPICAL R<sub>DS(on)</sub> = 0.050Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

#### DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

#### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



#### ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STY60NM60	Y60NM60	Max247	TUBE

## STY60NM60

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	600	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	600	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	60	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	37.8	A
I <sub>DM</sub> (*)	Drain Current (pulsed)	240	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	560	W
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=15KΩ)	6	KV
	Derating Factor	4.5	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(\*)Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 60A, di/dt ≤ 400 A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

### THERMAL DATA

R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	0.22	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	30	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	30	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 35 V)	1.4	J

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>gs</sub> =± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25\text{ °C}$  UNLESS OTHERWISE SPECIFIED)  
 ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu A, V_{GS} = 0$	600			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125\text{ °C}$			10 100	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\ V, I_D = 30\ A$		0.050	0.055	$\Omega$

**DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = I_{D(on)} \times R_{DS(on)max},$ $I_D = 30\ A$		35		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\ V, f = 1\ \text{MHz}, V_{GS} = 0$		7300 2000 40		pF pF pF
$R_G$	Gate Input Resistance	$f = 1\ \text{MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.8		$\Omega$

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 300\ V, I_D = 30\ A$ $R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see test circuit, Figure 3)		55 95		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 470\ V, I_D = 60\ A,$ $V_{GS} = 10\ V$		178 44.5 95	266	nC nC nC

**SWITCHING OFF**

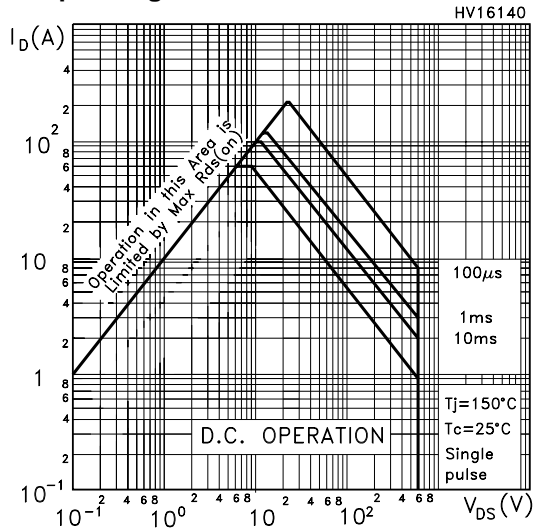
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 400\ V, I_D = 60\ A,$ $R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see test circuit, Figure 5)		130 76 105		ns ns ns

**SOURCE DRAIN DIODE**

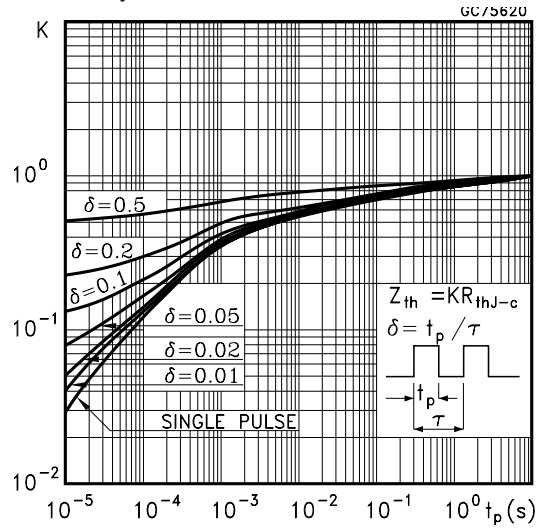
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				60 240	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 60\ A, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 60\ A, di/dt = 100\ A/\mu s,$ $V_{DD} = 30\ V, T_j = 150\text{ °C}$ (see test circuit, Figure 5)		600 14 48		ns $\mu C$ A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
 2. Pulse width limited by safe operating area.

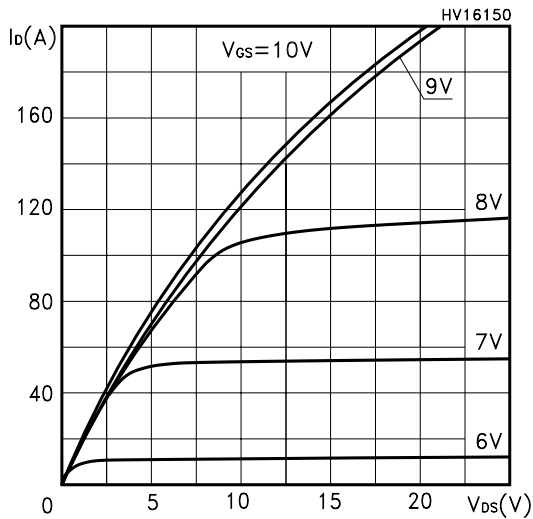
Safe Operating Area



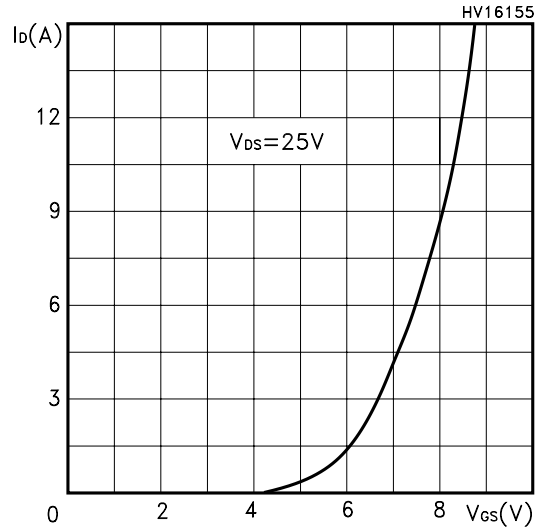
Thermal Impedance



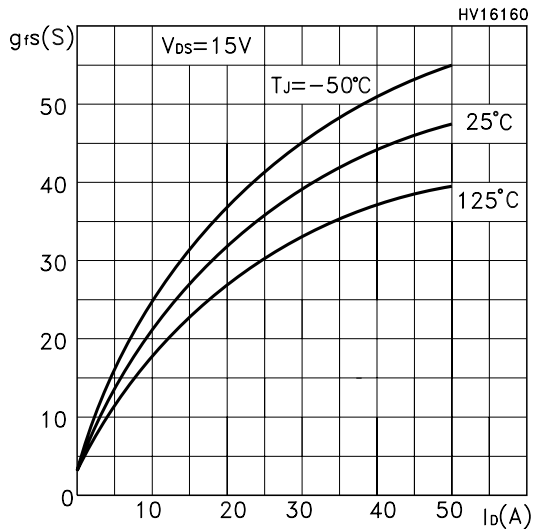
Output Characteristics



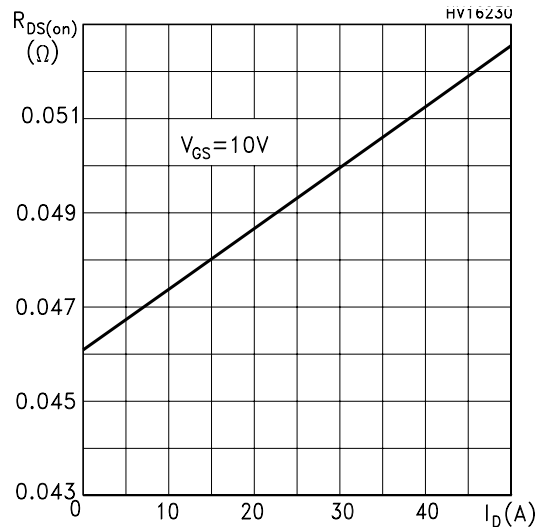
Transfer Characteristics



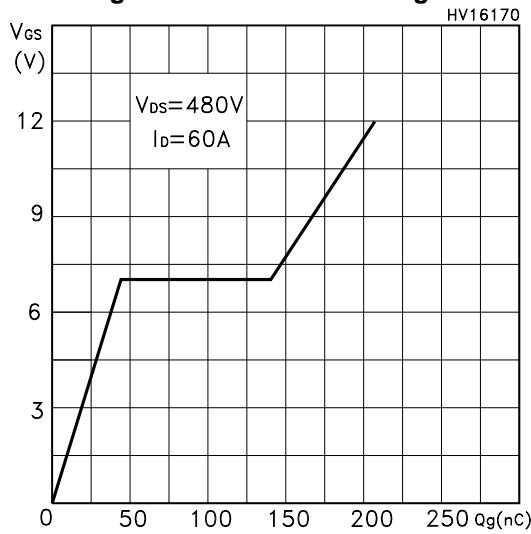
Transconductance



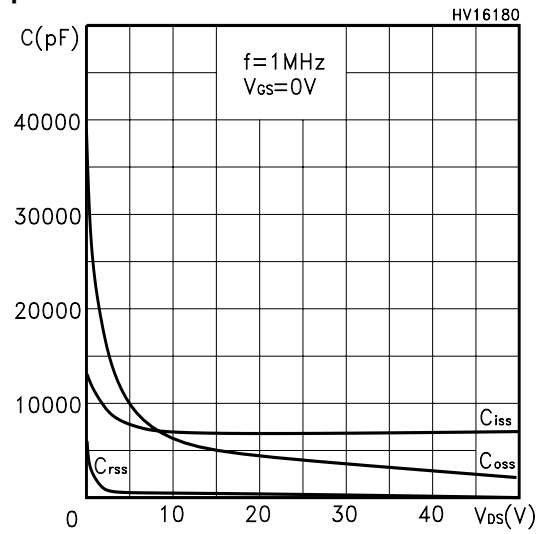
Static Drain-source On Resistance



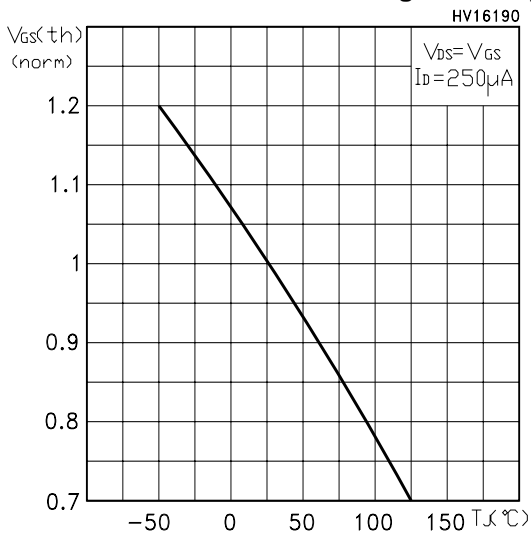
**Gate Charge vs Gate-source Voltage**



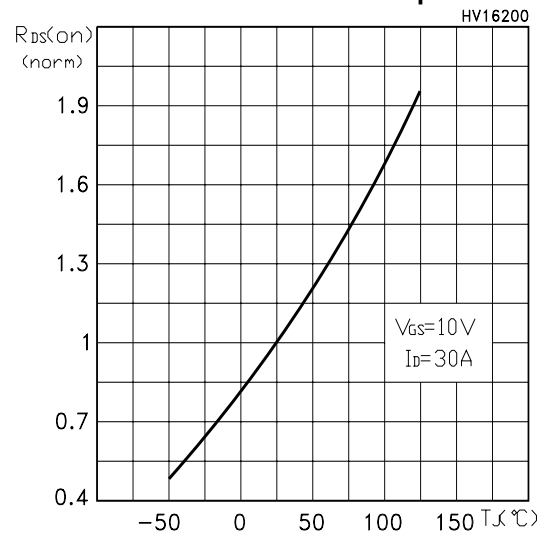
**Capacitance Variations**



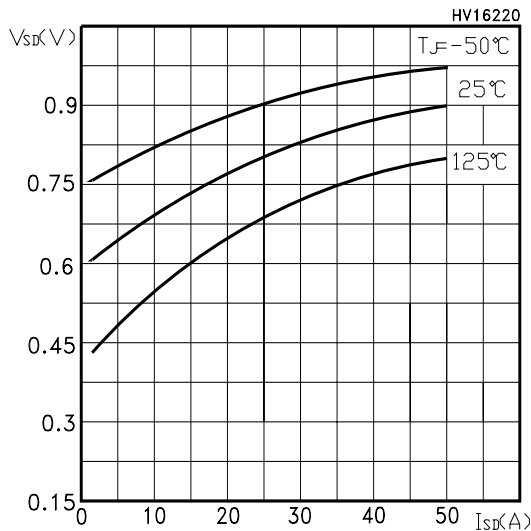
**Normalized Gate Threshold Voltage vs Temp.**



**Normalized On Resistance vs Temperature**



**Source-drain Diode Forward Characteristics**



**Normalized BVDSS vs Temperature**

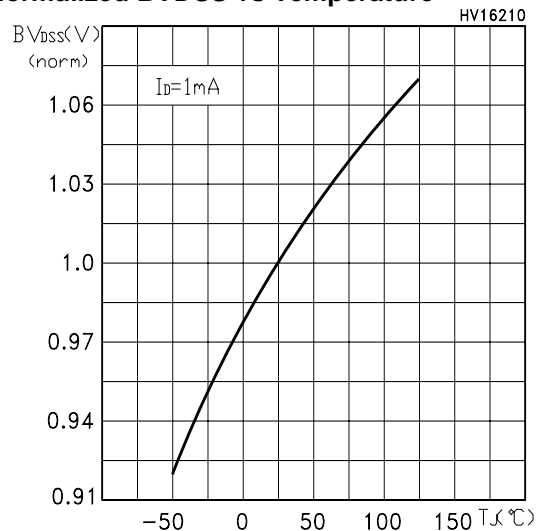


Fig. 1: Unclamped Inductive Load Test Circuit

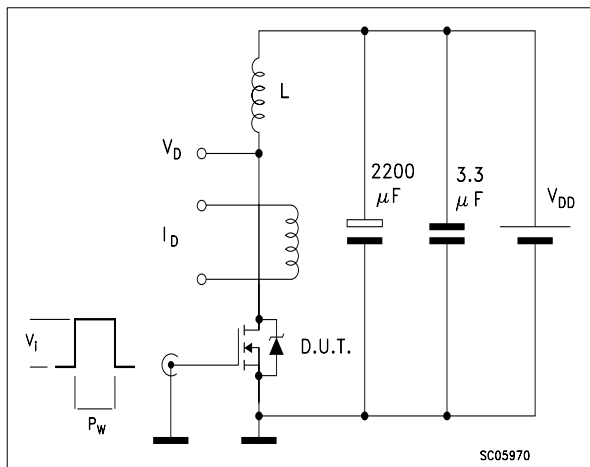


Fig. 2: Unclamped Inductive Waveform

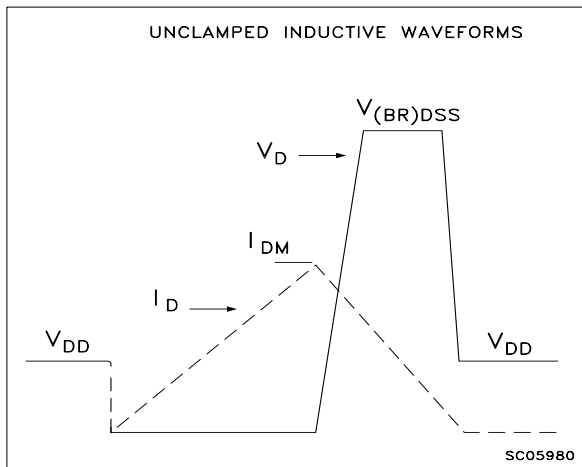


Fig. 3: Switching Times Test Circuit For Resistive Load

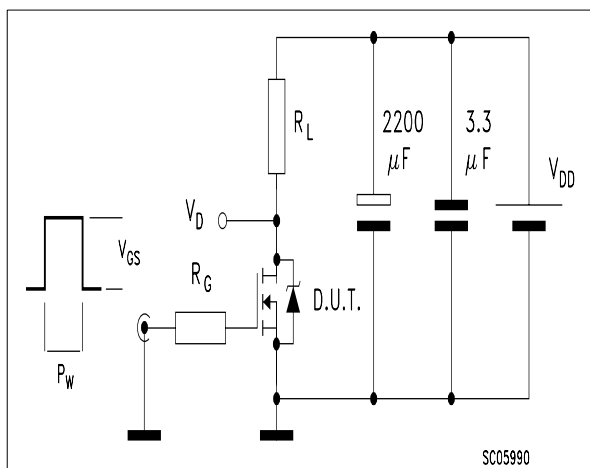


Fig. 4: Gate Charge test Circuit

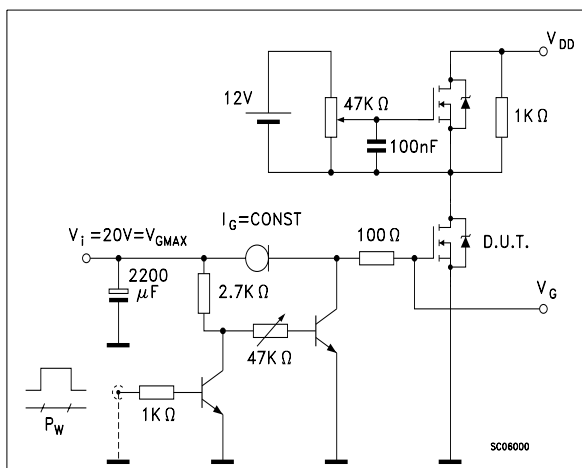
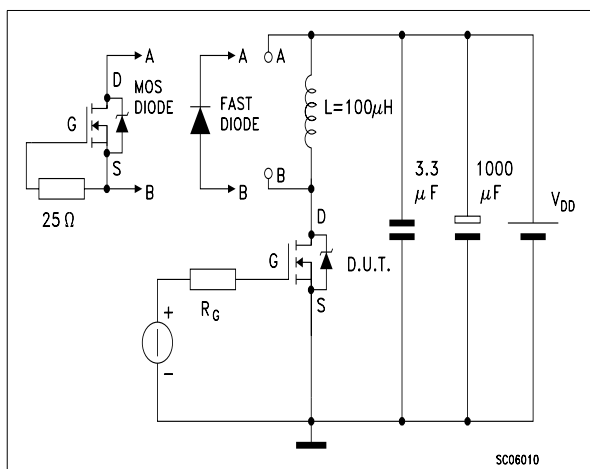
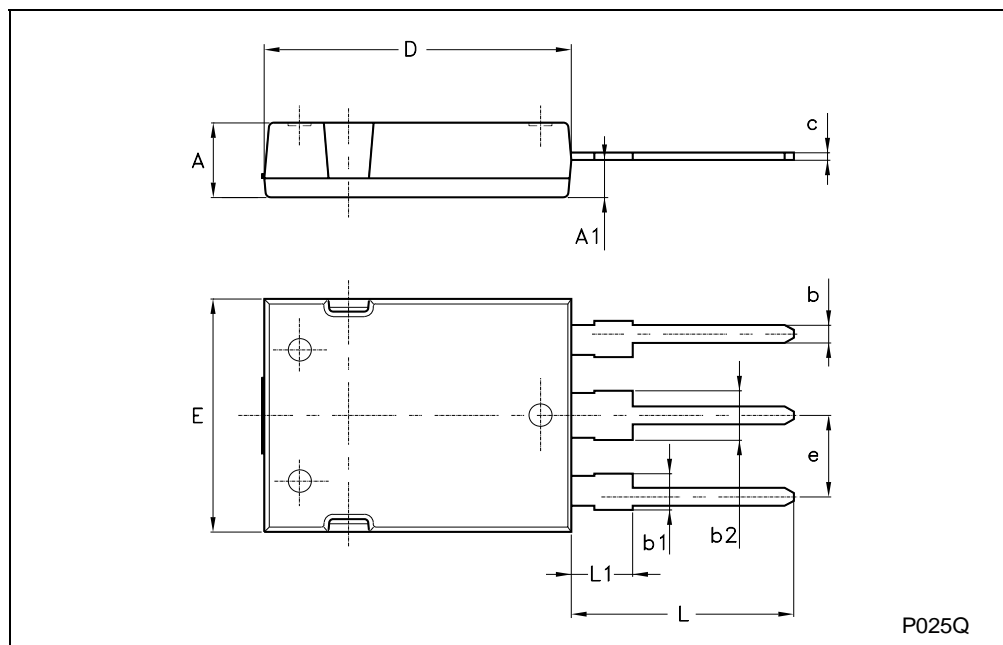


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**Max247 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



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