

FDMS8320L

N-Channel PowerTrench® MOSFET

40 V, 100 A, 1.1 mΩ

Features

- Max $r_{DS(on)}$ = 1.1 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 32\text{ A}$
- Max $r_{DS(on)}$ = 1.5 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 27\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

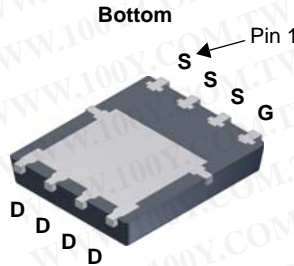


General Description

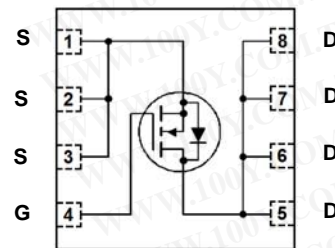
This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion



Power 56



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	100	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	238	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	36	
	-Pulsed	150	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	264	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	104	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8320L	FDMS8320L	Power 56	13"	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 32\ \text{A}$		0.8	1.1	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 27\ \text{A}$		1.0	1.5	
		$V_{GS} = 10\ \text{V}, I_D = 32\ \text{A}, T_J = 125^\circ\text{C}$		1.2	1.7	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 32\ \text{A}$		206		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		8350	11110	pF
C_{oss}	Output Capacitance			2840	3780	pF
C_{rss}	Reverse Transfer Capacitance			169	295	pF
R_g	Gate Resistance		0.1	1.3	2.6	Ω

Switching Characteristics

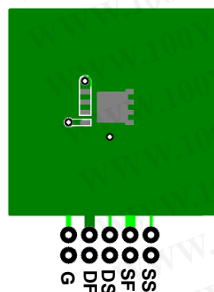
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\ \text{V}, I_D = 32\ \text{A}, V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		17	30	ns
t_r	Rise Time			19	35	ns
$t_{d(off)}$	Turn-Off Delay Time			68	110	ns
t_f	Fall Time			17	30	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V to } 10\ \text{V}$	$V_{DD} = 20\ \text{V}, I_D = 32\ \text{A}$	121	170	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V to } 4.5\ \text{V}$		58	117	nC
Q_{gs}	Gate to Source Charge			19.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			16.5		nC

Drain-Source Diode Characteristics

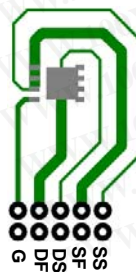
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.1\ \text{A}$ (Note 2)		0.65	1.1	V
		$V_{GS} = 0\ \text{V}, I_S = 32\ \text{A}$ (Note 2)		0.74	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 32\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		68	108	ns
Q_{rr}	Reverse Recovery Charge			59	95	nC
t_{rr}	Reverse Recovery Time	$I_F = 32\ \text{A}, di/dt = 300\ \text{A}/\mu\text{s}$		53	85	ns
Q_{rr}	Reverse Recovery Charge			104	167	nC

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Starting $T_J = 25^\circ\text{C}$; N-ch: L = 0.3 mH, $I_{AS} = 42\ \text{A}$, $V_{DD} = 36\ \text{V}$, $V_{GS} = 10\ \text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

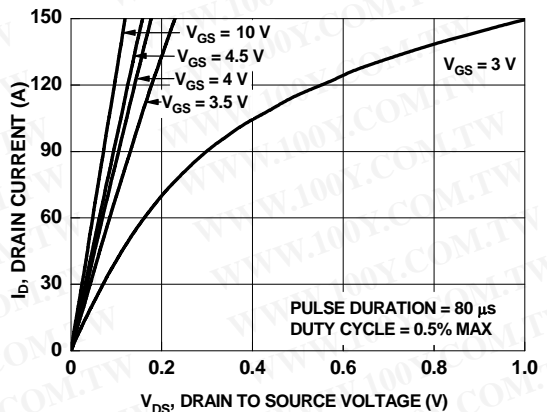


Figure 1. On Region Characteristics

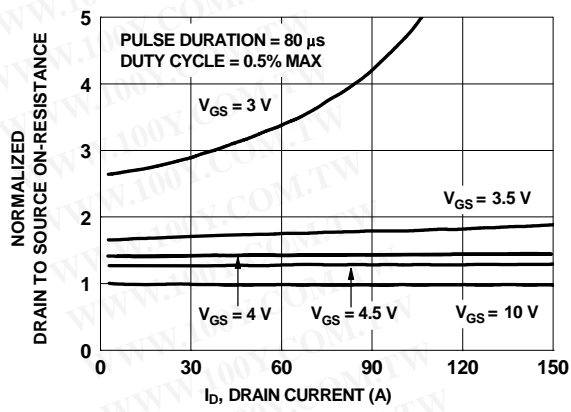


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

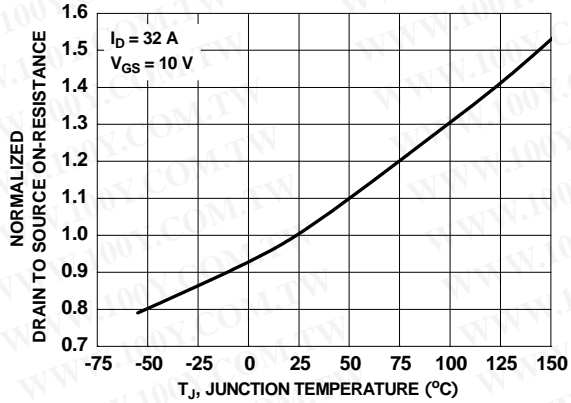


Figure 3. Normalized On Resistance vs Junction Temperature

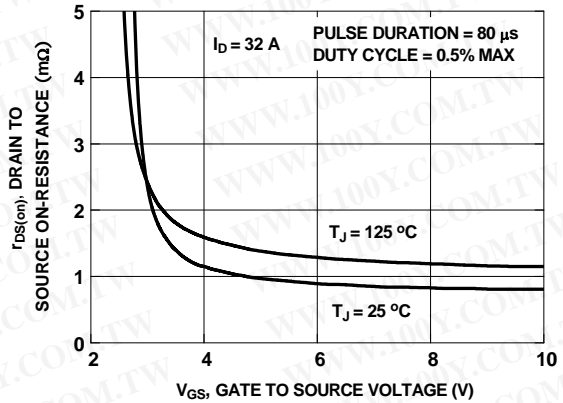


Figure 4. On-Resistance vs Gate to Source Voltage

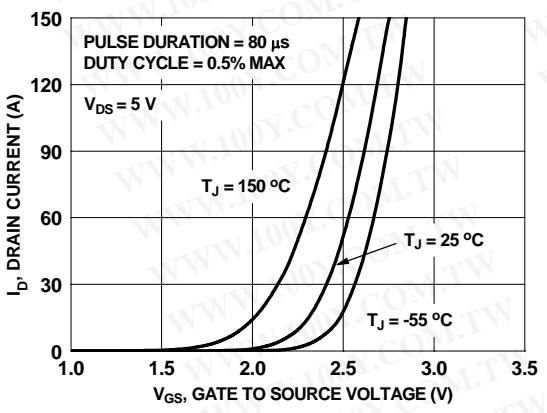


Figure 5. Transfer Characteristics

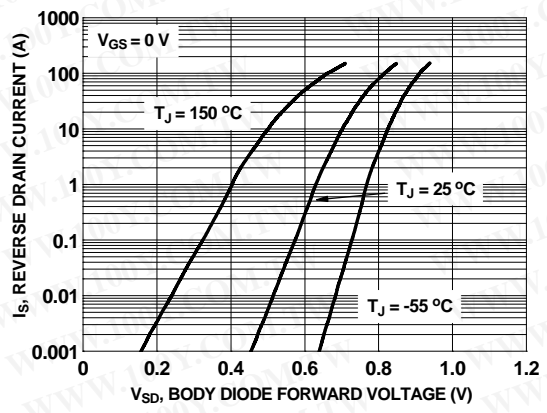


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

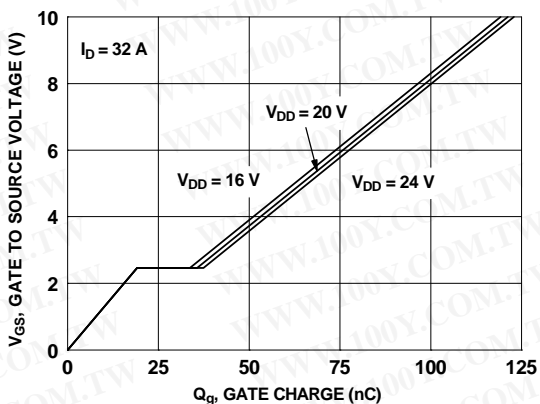


Figure 7. Gate Charge Characteristics

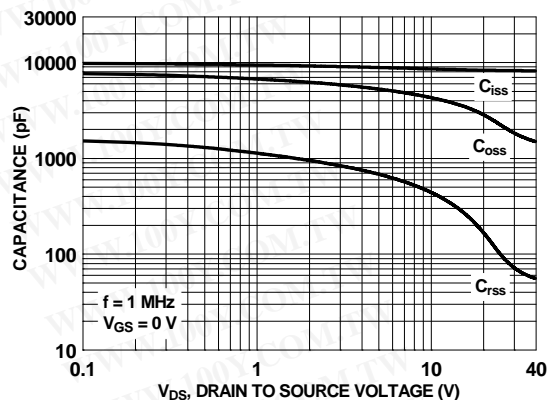


Figure 8. Capacitance vs Drain to Source Voltage

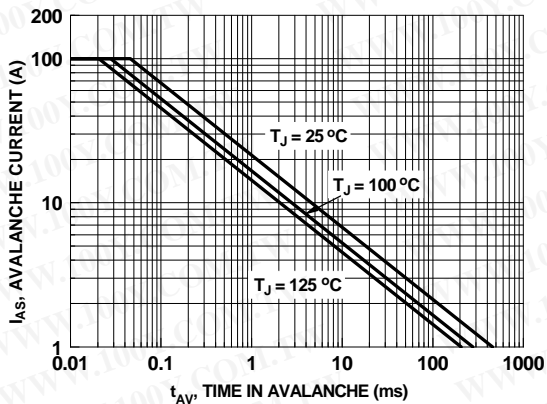


Figure 9. Unclamped Inductive Switching Capability

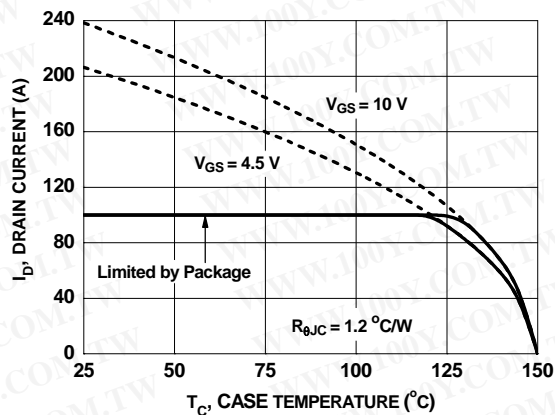


Figure 10. Maximum Continuous Drain Current vs Case Temperature

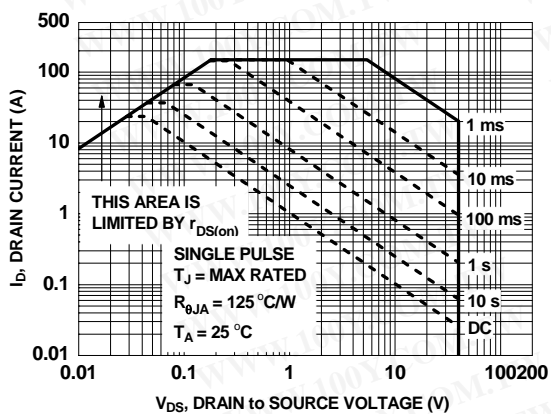


Figure 11. Forward Bias Safe Operating Area

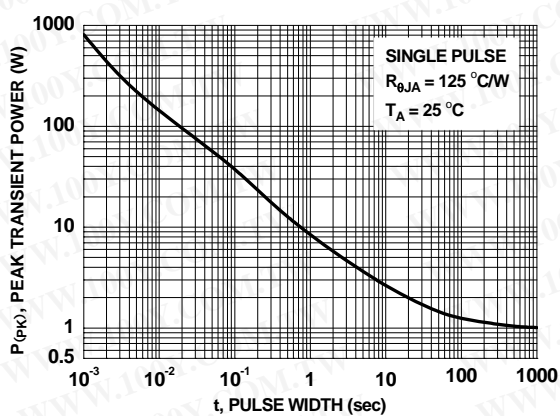


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

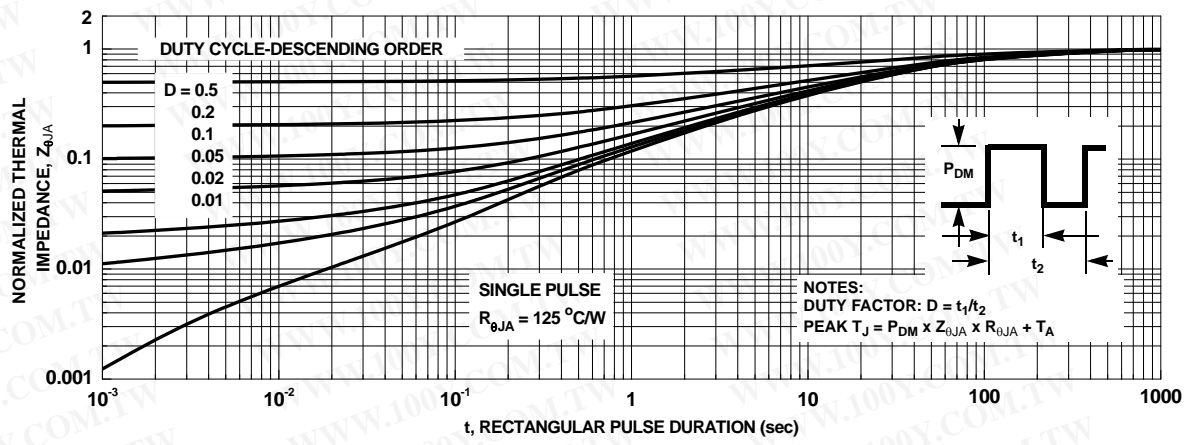
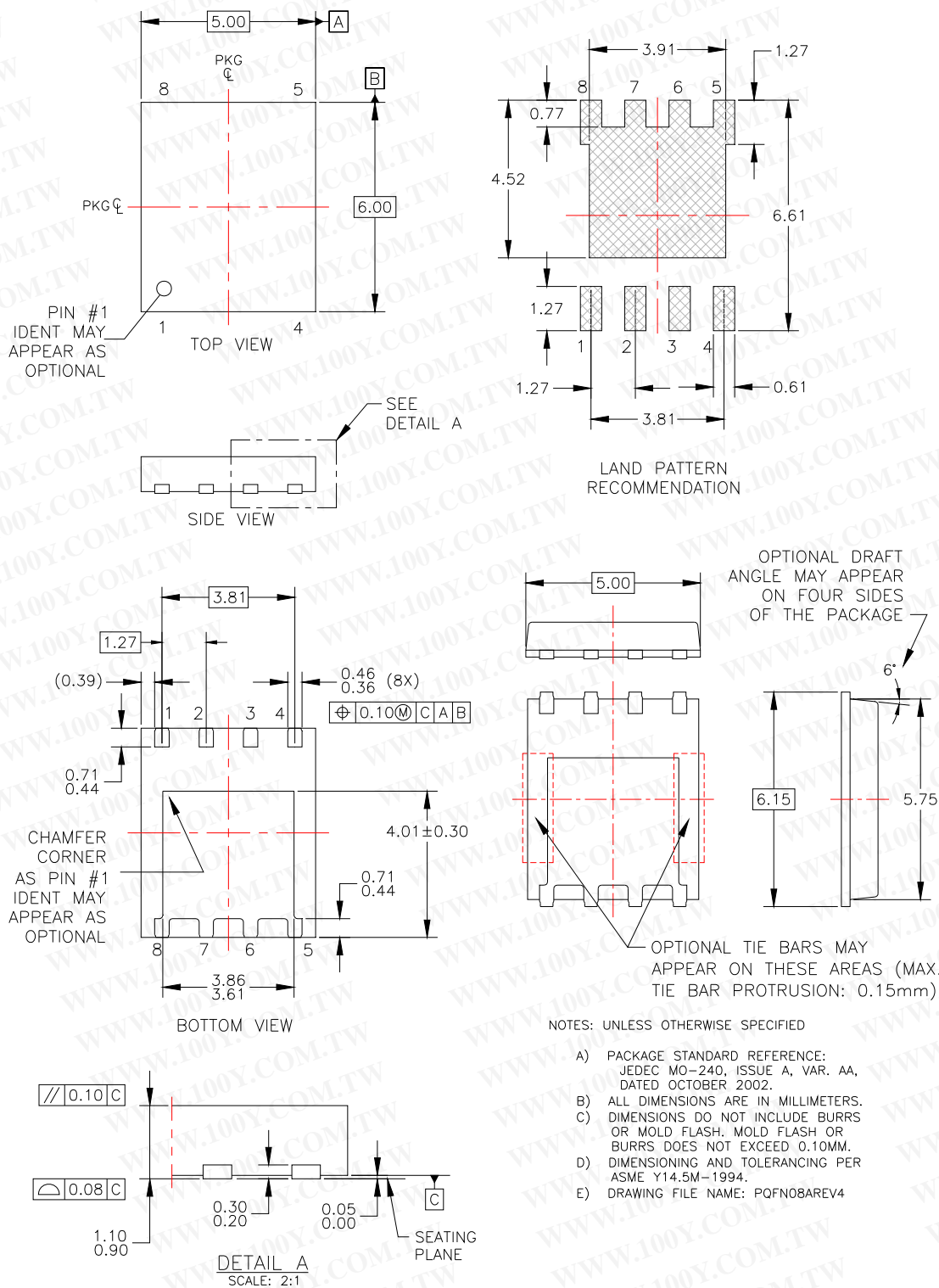


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08AREV4

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