FAIRCHILD SEMICONDUCTOR®

FDS86141

N-Channel PowerTrench® MOSFET

100 V, 7 A, 23 mΩ

Features

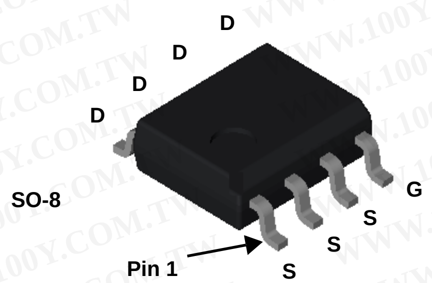
- Maximum $R_{DS(on)}$ = 23 mΩ at V_{GS} = 10 V, I_D = 7 A
- Maximum $R_{DS(on)}$ = 36 mΩ at V_{GS} = 6 V, I_D = 5.5 A
- High-Performance Trench Technology; Extremely Low $R_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

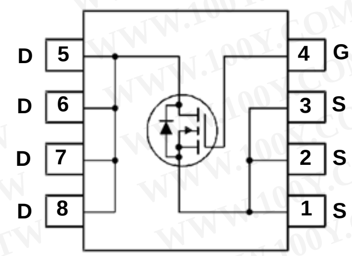
General Description

This N-channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and maintain superior switching performance.

Applications

- DC-DC Conversion





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous			7	A
	-Pulsed			30	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
P_D	Power Dissipation	T_A = 25 °C	(Note 1a)	5.0	W
	Power Dissipation	T_A = 25 °C	(Note 1b)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS86141	FDS86141	SO-8	13 ''	12 mm	2500 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		67		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.1	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A		19	23	mΩ
		V_{GS} = 6 V, I_D = 5.5 A		27	37	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C		33	40	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7 A		19		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		703	934	pF
C_{oss}	Output Capacitance			186	247	pF
C_{rss}	Reverse Transfer Capacitance			8.6	13	pF
R_g	Gate Resistance			0.5		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8.3	17	ns
t_r	Rise Time			3.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14.3	26	ns
t_f	Fall Time			3.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 7 A		11.8	16.5	nC
	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 7 A		6.7	9.4	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 7 A		3.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.1		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-to-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs		43	69	ns
Q_{rr}	Reverse Recovery Charge			39	62	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.

b) 125 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0 %.
3. Starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 9 A, V_{DD} = 100 V, V_{GS} = 10 V.

Typical Characteristics T_J = 25 °C unless otherwise noted.

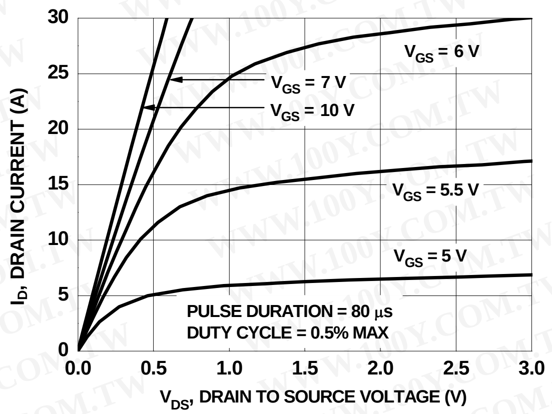


Figure 1. On-Region Characteristics

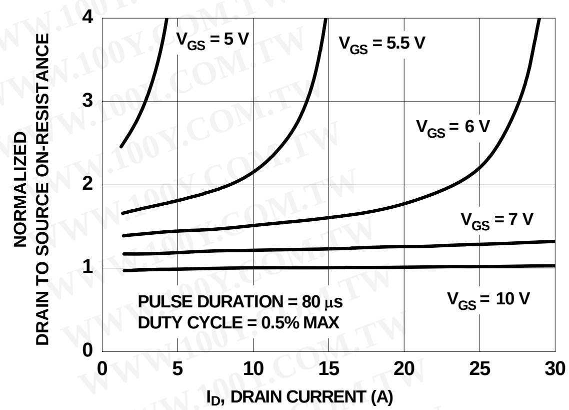


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

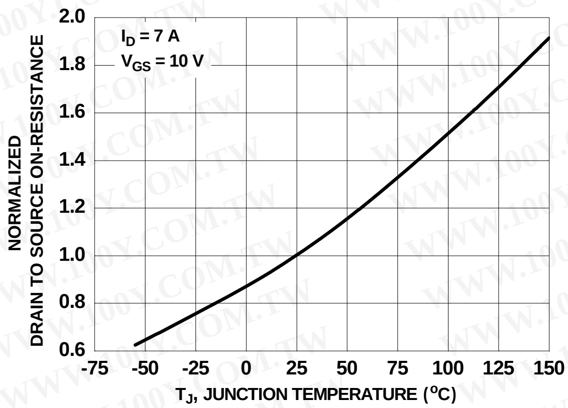


Figure 3. Normalized On-Resistance vs. Junction Temperature

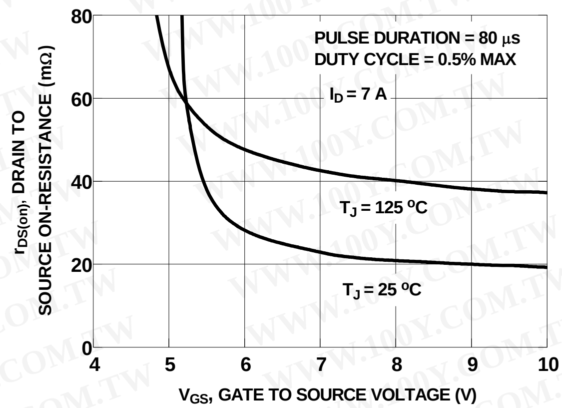


Figure 4. On-Resistance vs. Gate-to-Source Voltage

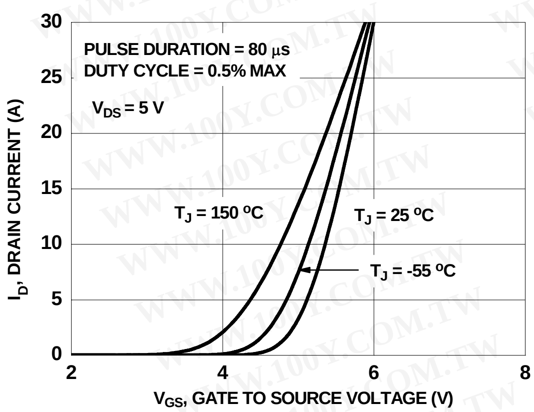


Figure 5. Transfer Characteristics

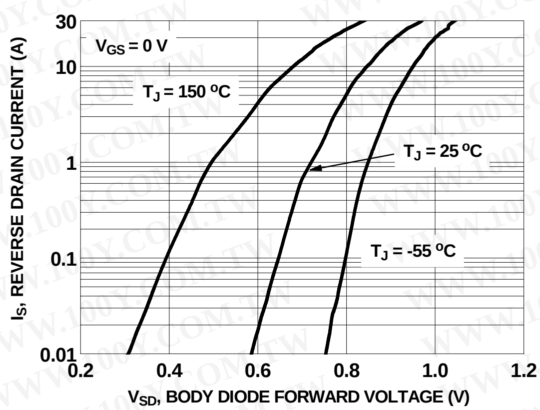


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

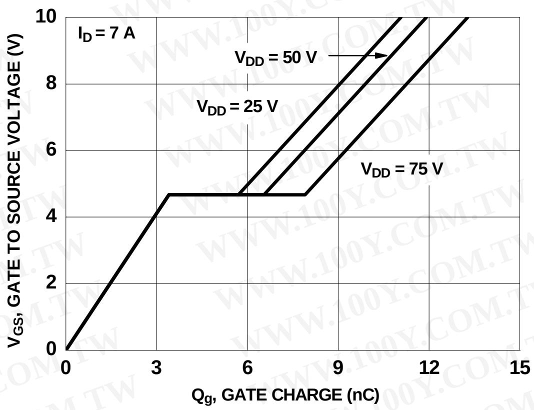


Figure 7. Gate Charge Characteristics

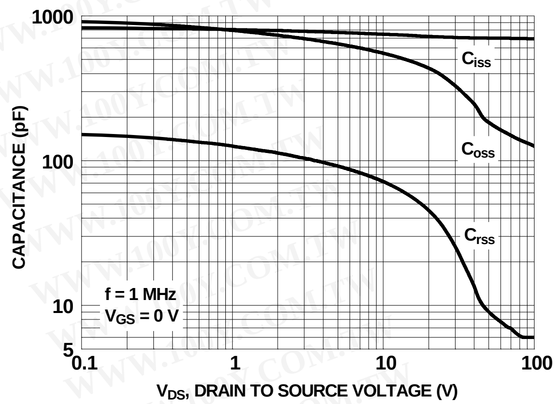


Figure 8. Capacitance vs. Drain-to-Source Voltage

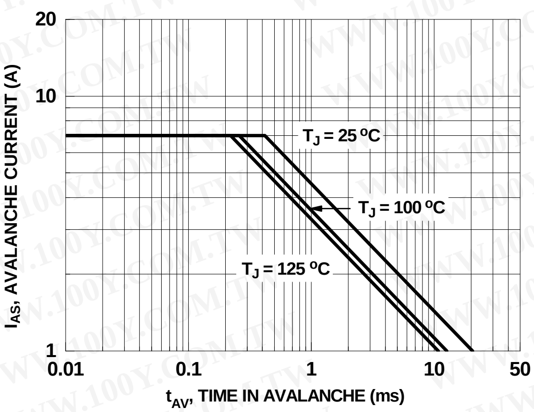


Figure 9. Unclamped Inductive Switching Capability

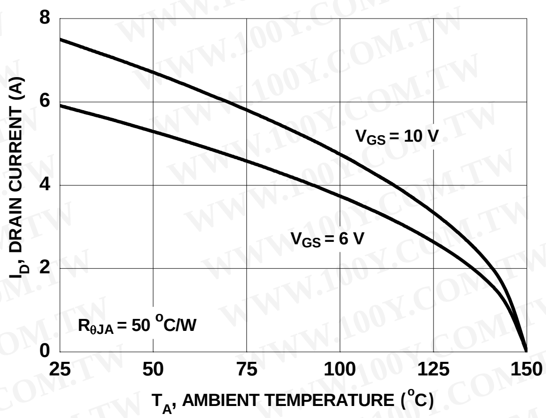


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

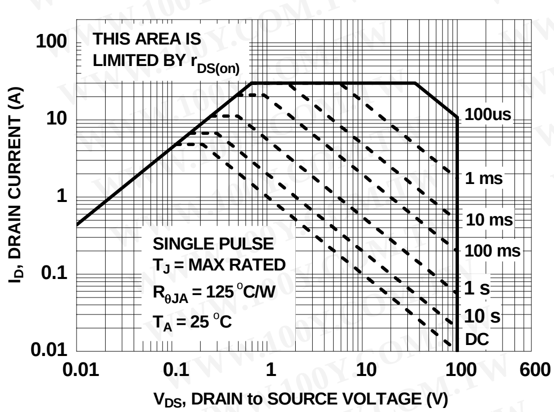


Figure 11. Forward Bias Safe Operating Area

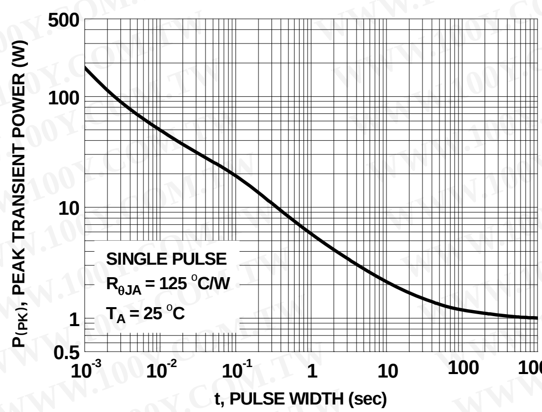


Figure 12. Single-Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

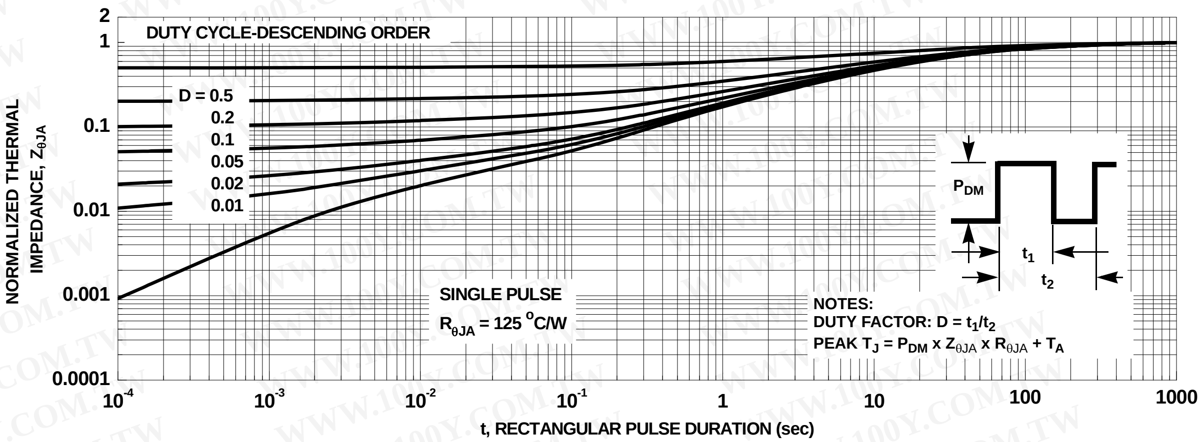


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Physical Dimensions

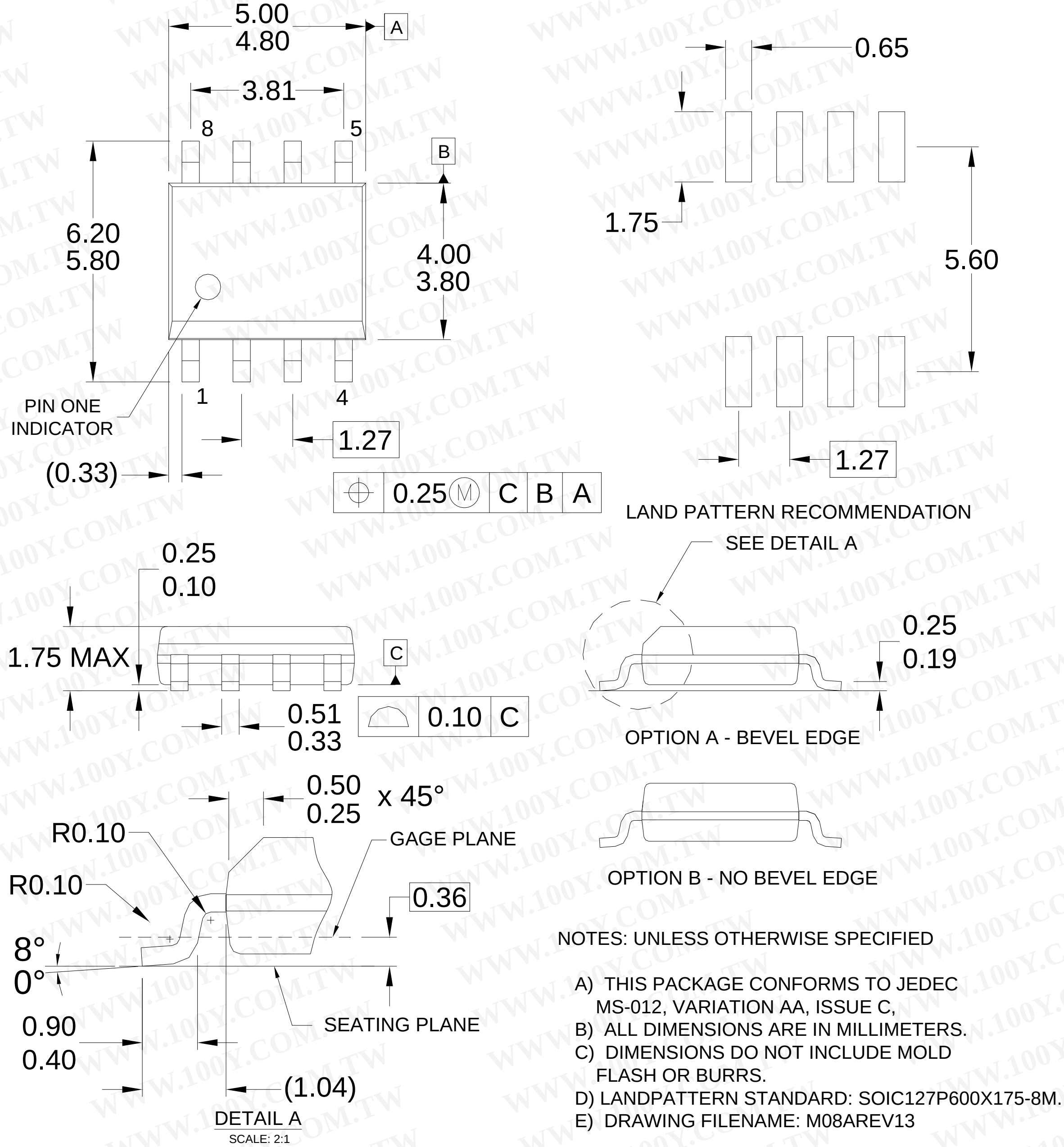


Figure 1. 8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150" Narrow Body

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