

FAIRCHILD
SEMICONDUCTOR®

FDW2511NZ

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

Features

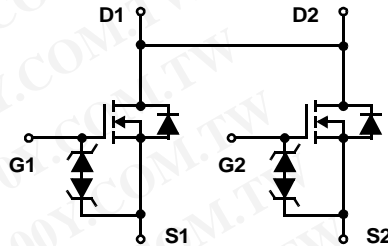
- 7.1A, 20V $r_{DS(ON)} = 0.020\Omega$, $V_{GS} = 4.5V$
 $r_{DS(ON)} = 0.025\Omega$, $V_{GS} = 2.5V$
- Extended V_{GS} range ($\pm 12V$) for battery applications
- HBM ESD Protection Level of 3.5kV Typical (note 3)
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low profile TSSOP-8 package

Applications

- Load switch
- Battery charge
- Battery disconnect circuits

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.



FDW2511NZ Dual N-Channel 2.5V Specified PowerTrench® MOSFET

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DSS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 12	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	7.1	A
	Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 2.5\text{V}$, $R_{\theta JA} = 77^\circ\text{C/W}$)	4.0	A
	Pulsed	Figure 4	A
P_D	Power dissipation	1.6	W
	Derate above 25°C	13	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 1)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 2)	114	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
2511NZ	FDW2511NZ	TSSOP-8	13"	12 mm	2500 units
2511NZ	FDW2511NZ_NL (Note 4)	TSSOP-8	13"	12 mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 100^\circ\text{C}$	-	-	5	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}$	-	-	± 10	μA
		$V_{GS} = \pm 4.5\text{V}$	-	-	± 250	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	0.6	0.8	1.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 7.1\text{A}$, $V_{GS} = 4.5\text{V}$	-	0.015	0.020	Ω
		$I_D = 6.9\text{A}$, $V_{GS} = 4.0\text{V}$	-	0.015	0.021	Ω
		$I_D = 6.5\text{A}$, $V_{GS} = 3.1\text{V}$	-	0.016	0.024	Ω
		$I_D = 6.3\text{A}$, $V_{GS} = 2.5\text{V}$	-	0.017	0.025	Ω

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	1000	-	pF	
C_{OSS}	Output Capacitance		-	250	-	pF	
C_{RSS}	Reverse Transfer Capacitance		-	175	-	pF	
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$	-	2.8	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	$V_{GS} = 0\text{V}$ to 4.5V	$V_{DD} = 10\text{V}$ $I_D = 7.1\text{A}$ $I_g = 1.0\text{mA}$	-	11.5	17.3	nC
$Q_{g(2.5)}$	Total Gate Charge at 2.5V	$V_{GS} = 0\text{V}$ to 2.5V		-	7.6	11.4	nC
Q_{gs}	Gate to Source Gate Charge			-	1.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	3.5	-	nC

Switching Characteristics ($V_{GS} = 4.5V$)

t_{ON}	Turn-On Time	$V_{DD} = 10V, I_D = 7.1A$ $V_{GS} = 4.5V, R_{GS} = 6.8\Omega$	-	-	146	ns
$t_{d(ON)}$	Turn-On Delay Time		-	13	-	ns
t_r	Rise Time		-	84	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	41	-	ns
t_f	Fall Time		-	55	-	ns
t_{OFF}	Turn-Off Time		-	-	144	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 1.3A$	-	0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 7.1A, di_{SD}/dt = 100A/\mu s$	-	-	27	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 7.1A, di_{SD}/dt = 100A/\mu s$	-	-	16	nC

Notes:

- $R_{\theta JA}$ is 77 °C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
- $R_{\theta JA}$ is 114 °C/W (steady state) when mounted on a minimum copper pad on FR-4.
- The diode connected to the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- FDW2511NZ_NL is lead free product. FDW2511NZ_NL marking will appear on the reel label.

Typical Characteristic $T_A = 25^\circ\text{C}$ unless otherwise noted

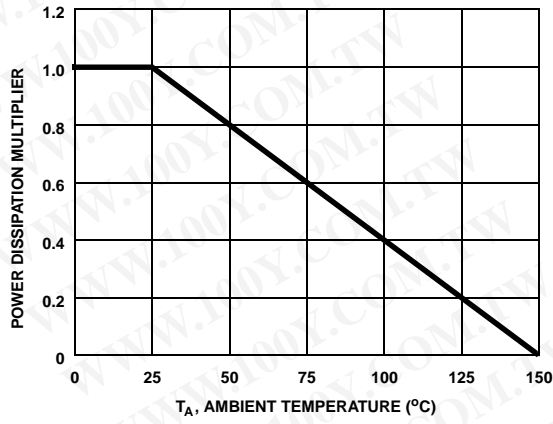


Figure 1. Normalized Power Dissipation vs Ambient Temperature

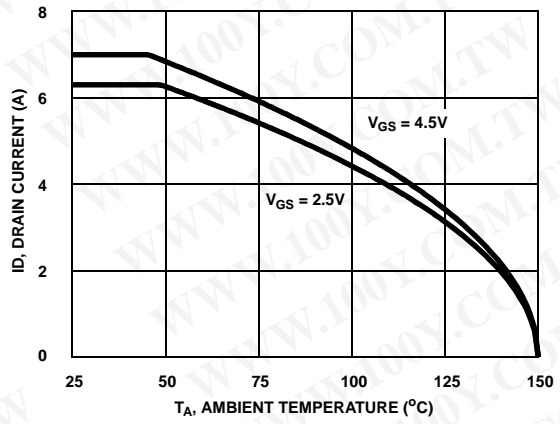


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

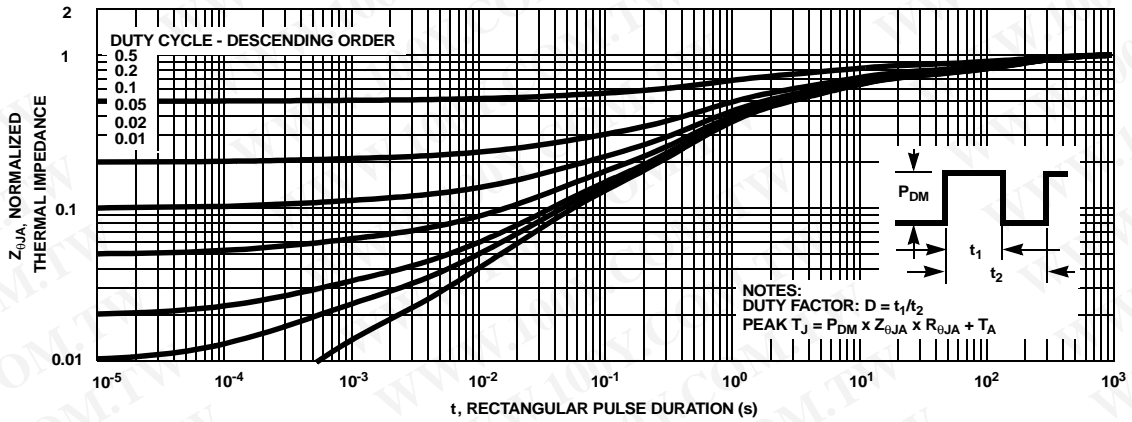


Figure 3. Normalized Maximum Transient Thermal Impedance

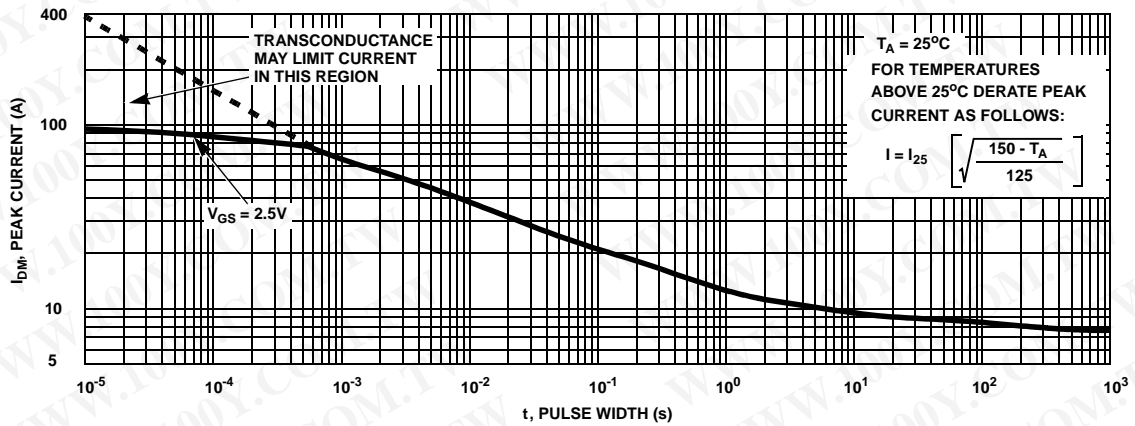


Figure 4. Peak Current Capability

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

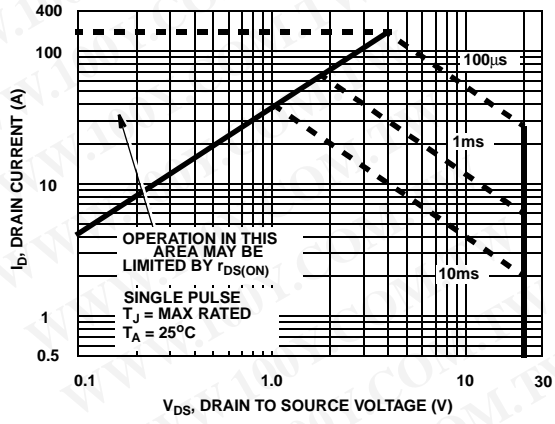


Figure 5. Forward Bias Safe Operating Area

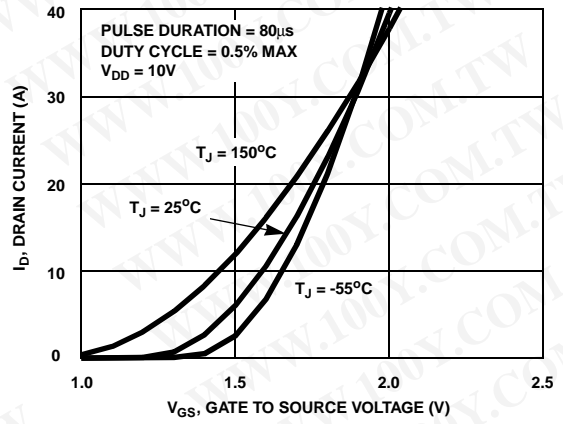


Figure 6. Transfer Characteristics

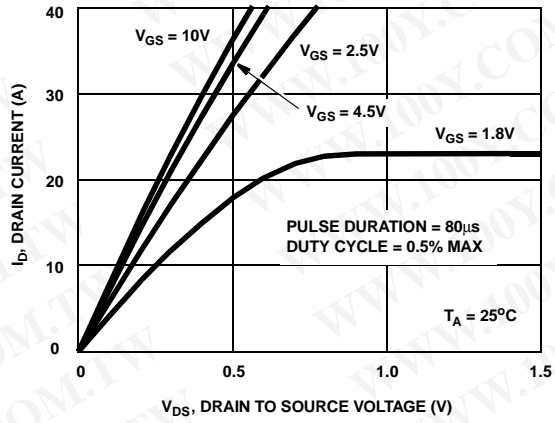


Figure 7. Saturation Characteristics

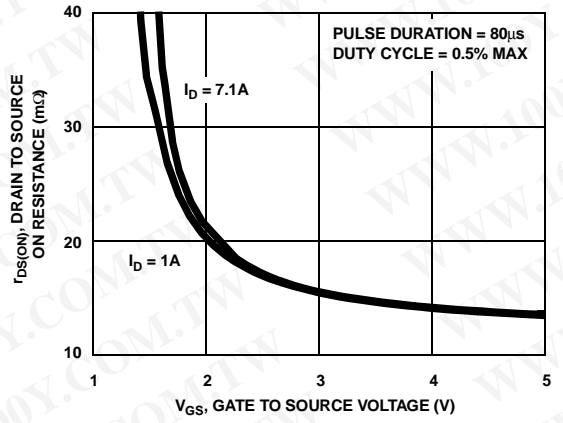


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

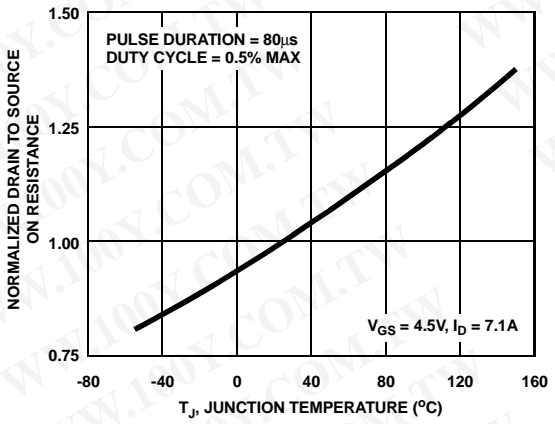


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

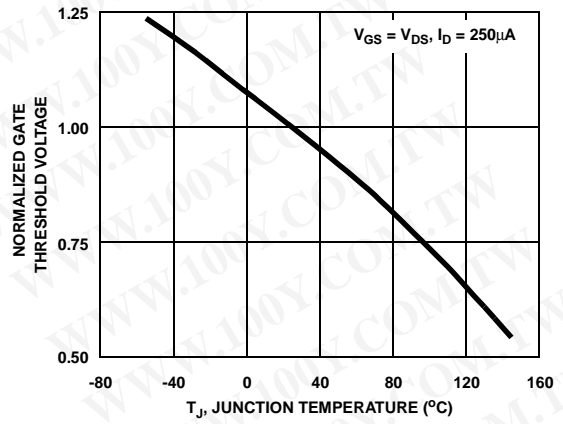


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristic (Continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

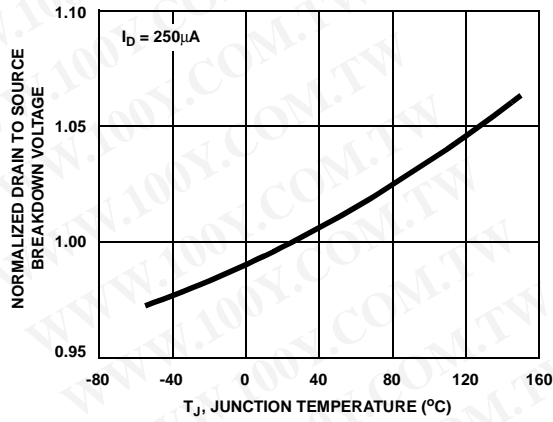


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

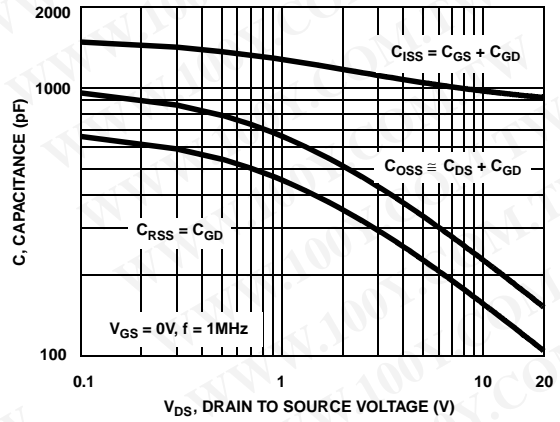


Figure 12. Capacitance vs Drain to Source Voltage

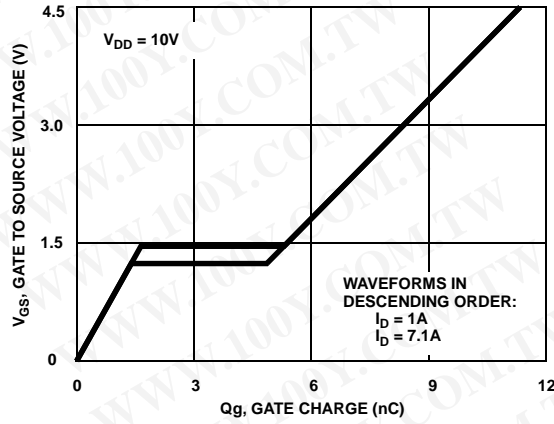


Figure 13. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

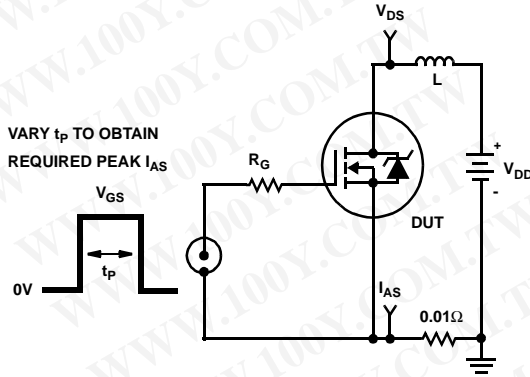


Figure 14. Unclamped Energy Test Circuit

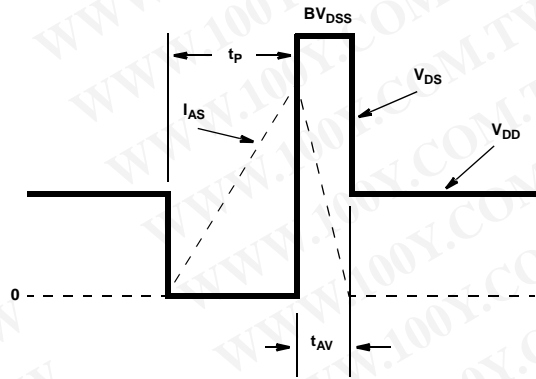


Figure 15. Unclamped Energy Waveforms

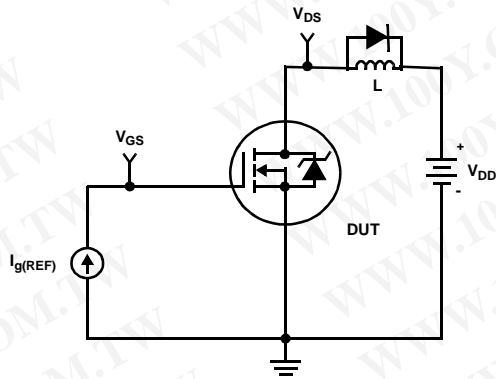


Figure 16. Gate Charge Test Circuit

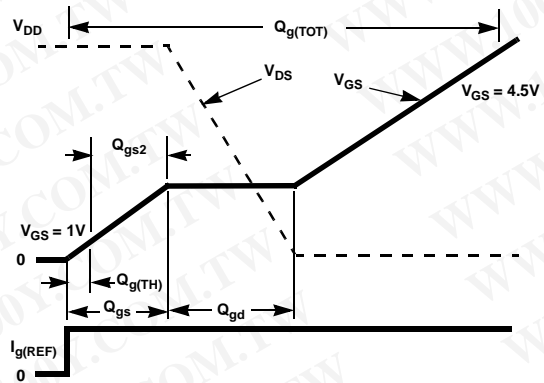


Figure 17. Gate Charge Waveforms

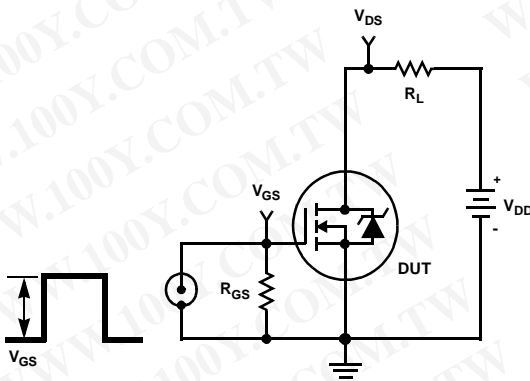


Figure 18. Switching Time Test Circuit

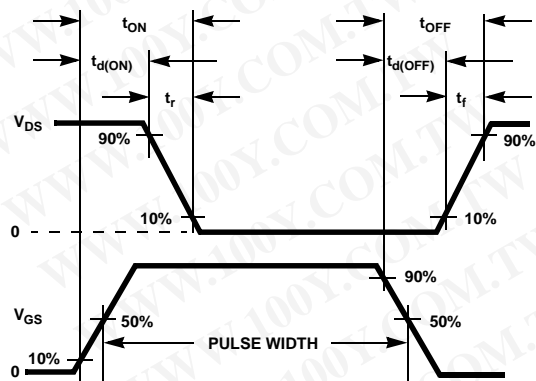


Figure 19. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDW2511NZ 2 1 3 ; rev July 2004

Ca 12 8 1.1e-9
 Cb 15 14 1.1e-9
 Cin 6 8 0.8e-9

Dbody 7 5 DbodyMOD
 Dbreak 5 11 DbreakMOD
 DESD2 91 9 DESD2MOD
 DESD1 91 7 DESD1MOD
 Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 24
 Eds 14 8 5 8 1
 Egs 13 8 6 8 1
 Esg 6 10 6 8 1
 Evthres 6 21 19 8 1
 Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 9.1e-10
 Rldrain 2 5 1e-9
 Lsource 3 7 2.1e-10

RLgate 1 9 9.1
 RLdrain 2 5 10
 RLsource 3 7 2.1

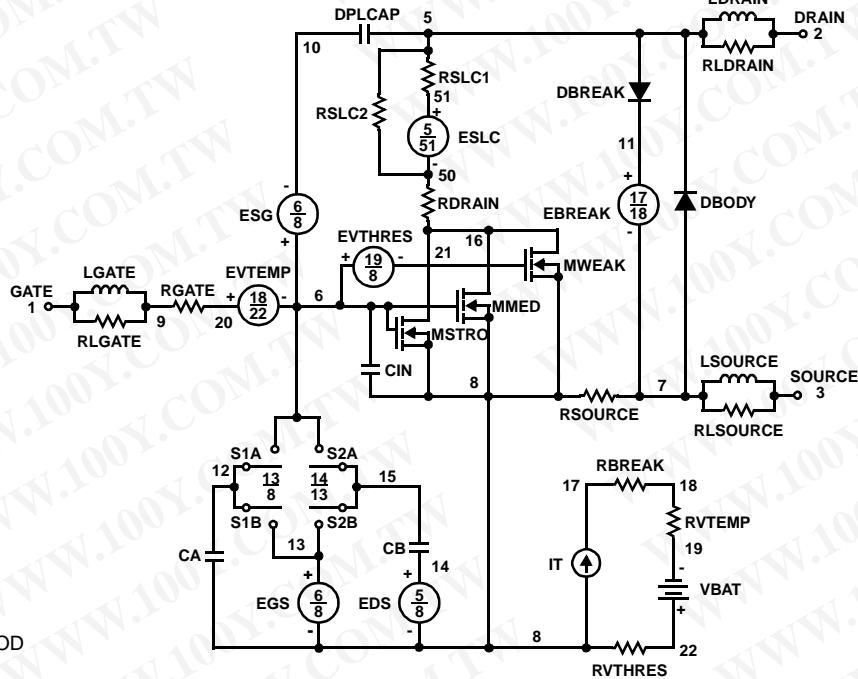
Mmed 16 6 8 8 MmedMOD
 Mstro 16 6 8 8 MstroMOD
 Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
 Rdrain 50 16 RdrainMOD 1.0e-2
 Rgate 9 20 2.75
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 Rsource 8 7 RsourceMOD 1.7e-3
 Rvthres 22 8 Rvthresmod 1
 Rvtemp 18 19 RvtempMOD 1
 S1a 6 12 13 8 S1AMOD
 S1b 13 12 13 8 S1BMOD
 S2a 6 15 14 13 S2AMOD
 S2b 13 15 14 13 S2BMOD
 Vbat 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*120),2.5))}
 MODEL DbodyMOD D (IS=3.5E-11 RS=1.08e-2 IKF=.5 N= TRS1=8e-4 TRS2=6e-6 XTI=.1
 +CJO=3.2e-10 TT=1.07e-8 M=0.68 TIKF=0.001)
 .MODEL DbreakMOD D (RS=1e-1 TRS1=9e-3 TRS2=-2.0e-5)
 .MODEL DESD1MOD D (BV=15.0 RS=1)
 .MODEL DESD2MOD D (BV=14.3 RS=1)
 .MODEL DplcapMOD D (CJO=0.70e-9 IS=1e-30 N=10 M=0.3)
 MODEL Mstro NMOS (VTO=1.21 KP=147 IS=1e-30 N=10 TOX=1 L=1u W=1u)
 .MODEL MweakMOD NMOS (VTO=0.752 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=27.5 RS=.1)
 MODEL RbreakMOD RES (TC1=5.0e-4 TC2=8e-7)
 .MODEL RdrainMOD RES (TC1=2.1e-3 TC2=3.4e-6)
 .MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-5)
 .MODEL RsourceMOD RES (TC1=5e-3 TC2=1e-6)
 .MODEL RvtempMOD RES (TC1=-.9e-3 TC2=1e-7)
 .MODEL RvthresMOD RES (TC1=-1.1e-3 TC2=-4.0e-6)
 MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6 VOFF=-1.5)
 .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-6)
 .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)
 .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)
 ENDS

*\$

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV July 2004
 FDW2511NZ_JA Junction Ambient
 Minimum copper pad area

CTHERM1 Junction c2 5.7e-4
 CHERM2 c2 c3 5.72e-4
 CHERM3 c3 c4 5.8e-4
 CHERM4 c4 c5 4.7e-3
 CHERM5 c5 c6 5.1e-3
 CHERM6 c6 c7 0.02
 CHERM7 c7 c8 0.2
 CHERM8 c8 Ambient 6

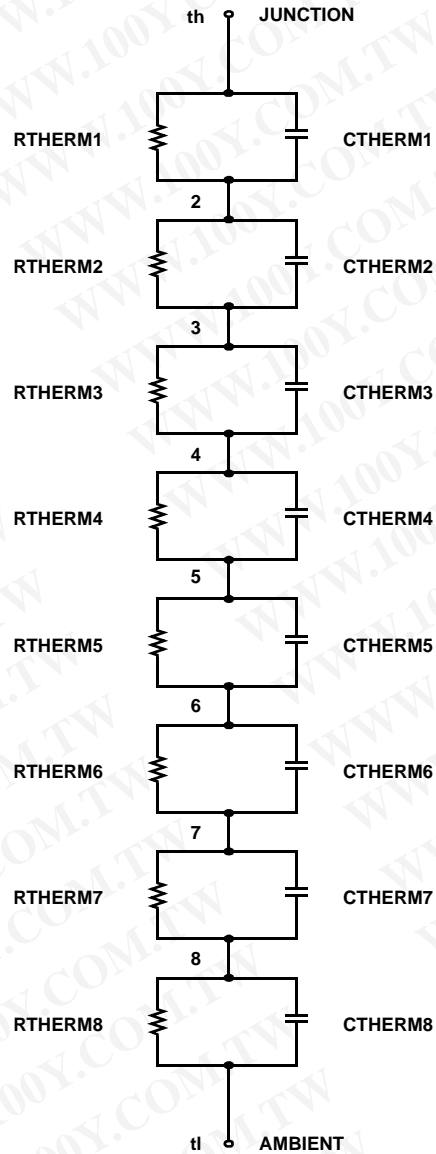
RHERM1 Junction c2 0.003
 RHERM2 c2 c3 0.25
 RHERM3 c3 c4 1.0
 RHERM4 c4 c5 1.1
 RHERM5 c5 c6 7.5
 RHERM6 c6 c7 33.6
 RHERM7 c7 c8 33.7
 RHERM8 c8 Ambient 33.8

SABER Thermal Model

SABER thermal model FDW2511NZ
 Minimum copper pad area
 template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th c2 = 5.7e-4
    ctherm.ctherm2 c2 c3 = 5.72e-4
    ctherm.ctherm3 c3 c4 = 5.8e-4
    ctherm.ctherm4 c4 c5 = 4.7e-3
    ctherm.ctherm5 c5 c6 = 5.1e-3
    ctherm.ctherm6 c6 c7 = 0.02
    ctherm.ctherm7 c7 c8 = 0.2
    ctherm.ctherm8 c8 tl = 6
}
```

```
rtherm.rtherm1 th c2 = 0.003
rtherm.rtherm2 c2 c3 = 0.25
rtherm.rtherm3 c3 c4 = 1.0
rtherm.rtherm4 c4 c5 = 1.1
rtherm.rtherm5 c5 c6 = 7.5
rtherm.rtherm6 c6 c7 = 33.6
rtherm.rtherm7 c7 c8 = 33.7
rtherm.rtherm8 c8 tl = 33.8
}
```



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Bottomless™	FASTr™	ISOPLANAR™	PowerEdge™	SuperSOT™-3
CoolFET™	FPS™	LittleFET™	PowerSaver™	SuperSOT™-6
CROSSVOLT™	FRFET™	MICROCOUPLER™	PowerTrench®	SuperSOT™-8
DOVE™	GlobalOptoisolator™	MicroFET™	QFET®	SyncFET™
EcoSPARK™	GTO™	MicroPak™	QS™	TinyLogic®
E ² C MOS™	HiSeC™	MICROWIRE™	QT Optoelectronics™	TINYOPTO™
EnSigna™	I ² C™	MSX™	Quiet Series™	TruTranslation™
FACT™	i-Lo™	MSXPro™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCX™	RapidConnect™	UltraFET®
The Power Franchise®		OCXPro™	µSerDes™	UniFET™
Programmable Active Droop™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
		OPTOPLANAR™	SMART START™	
		PACMAN™	SPM™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.