

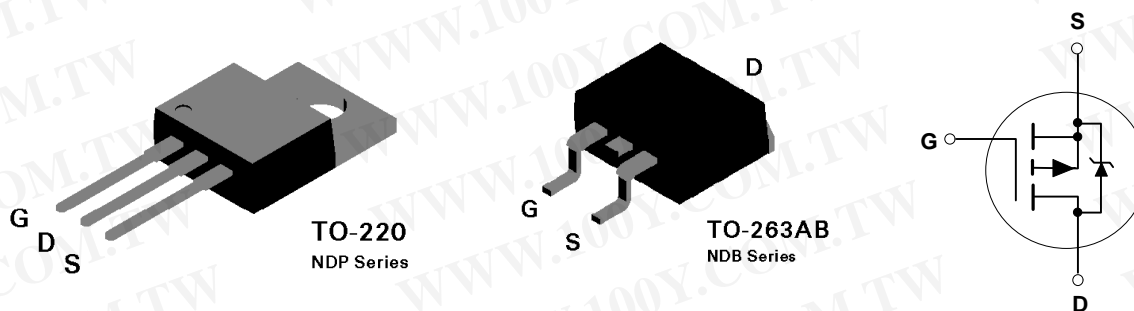
**NDP6020P / NDB6020P**  
**P-Channel Logic Level Enhancement Mode Field Effect Transistor**

**General Description**

These logic level P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

**Features**

- -24 A, -20 V.  $R_{DS(ON)} = 0.05 \Omega @ V_{GS} = -4.5 \text{ V}$ .  
 $R_{DS(ON)} = 0.07 \Omega @ V_{GS} = -2.7 \text{ V}$ .  
 $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = -2.5 \text{ V}$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.



**Absolute Maximum Ratings**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	NDP6020P	NDB6020P	Units
$V_{DSS}$	Drain-Source Voltage		-20	V
$V_{GSS}$	Gate-Source Voltage - Continuous		±8	V
$I_D$	Drain Current	- Continuous	-24	A
		- Pulsed	-70	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	60		W
		0.4		
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 175		°C

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**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$	
			$T_J = 55^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
<b>ON CHARACTERISTICS</b> (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$		-0.4	-0.7	-1	V
			$T_J = 125^\circ\text{C}$	-0.3	-0.56	-0.7	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -12\text{ A}$			0.041	0.05	$\Omega$
			$T_J = 125^\circ\text{C}$			0.06	0.08
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -2.7\text{ V}, I_D = -10\text{ A}$			0.059	0.07	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -2.5\text{ V}, I_D = -10\text{ A}$			0.064	0.075	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-24			A	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -12\text{ A}$		14		S	
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1590		pF	
$C_{oss}$	Output Capacitance			725		pF	
$C_{rss}$	Reverse Transfer Capacitance			215		pF	
<b>SWITCHING CHARACTERISTICS</b> (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -20\text{ V}, I_D = -3\text{ A},$ $V_{GS} = -5\text{ V}, R_{G\text{EN}} = 6\ \Omega$		15	30	nS	
$t_r$	Turn - On Rise Time			27	60	nS	
$t_{D(off)}$	Turn - Off Delay Time			120	250	nS	
$t_f$	Turn - Off Fall Time			70	150	nS	
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V},$ $I_D = -24\text{ A}, V_{GS} = -5\text{ V}$		25	35	nC	
$Q_{gs}$	Gate-Source Charge			5		nC	
$Q_{gd}$	Gate-Drain Charge			10		nC	

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**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-24	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current				-80	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -12\text{ A}$ (Note 1)		-1.1	-1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = -24\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		60		ns
$I_{rr}$	Reverse Recovery Current			-1.7		A
<b>THERMAL CHARACTERISTICS</b>						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	$^\circ\text{C}/\text{W}$

Note:

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

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## Typical Electrical Characteristics

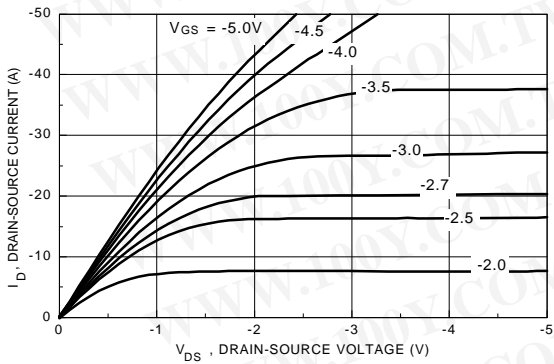


Figure 1. On-Region Characteristics.

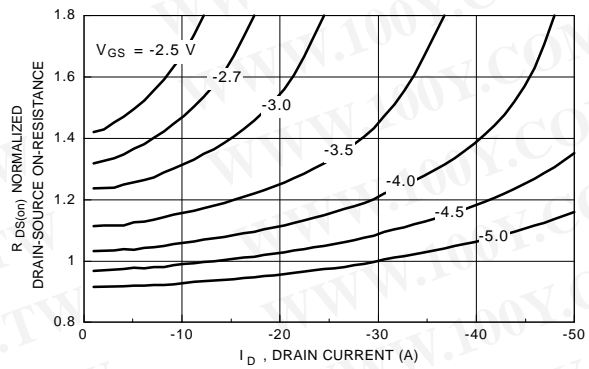


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

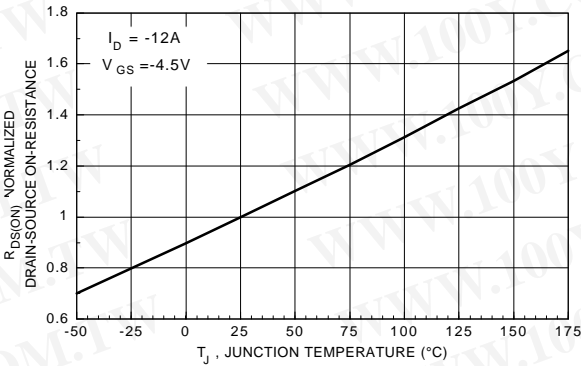


Figure 3. On-Resistance Variation with Temperature.

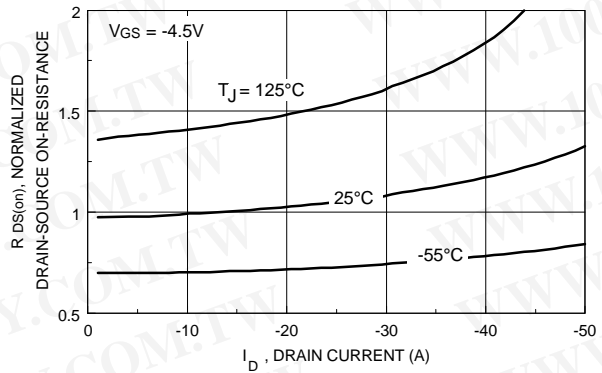


Figure 4. On-Resistance Variation with Drain Current and Temperature.

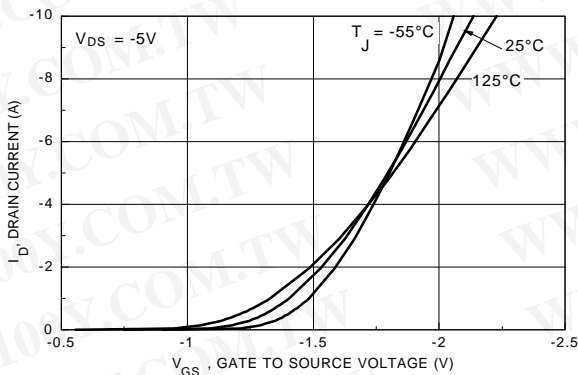


Figure 5. Transfer Characteristics.

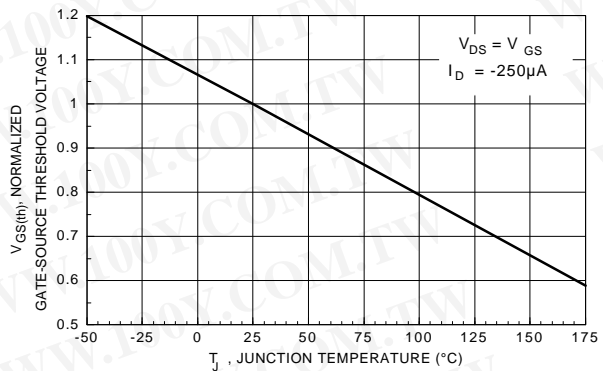


Figure 6. Gate Threshold Variation with Temperature.

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## Typical Electrical Characteristics (continued)

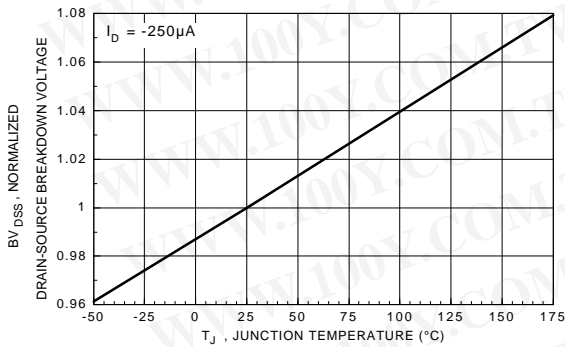


Figure 7. Breakdown Voltage Variation with Temperature.

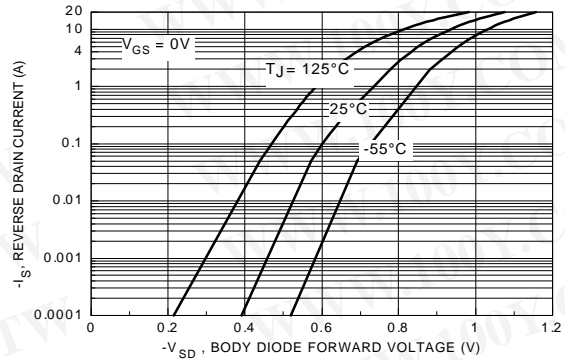


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

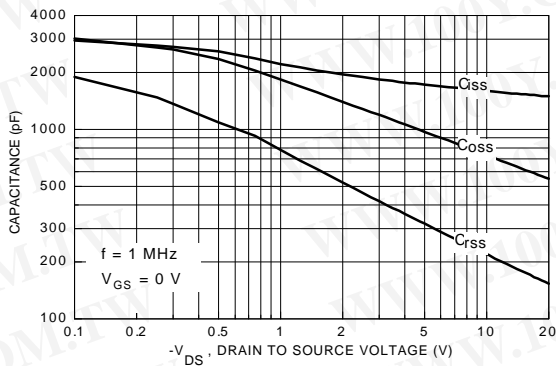


Figure 9. Capacitance Characteristics.

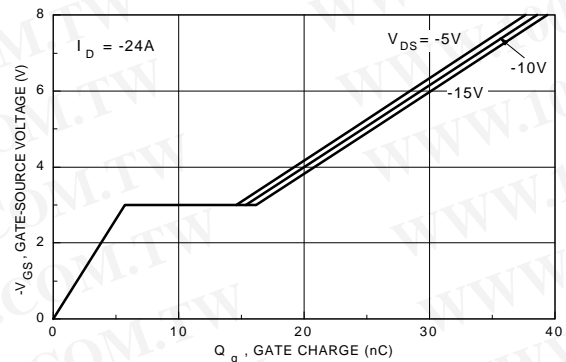


Figure 10. Gate Charge Characteristics.

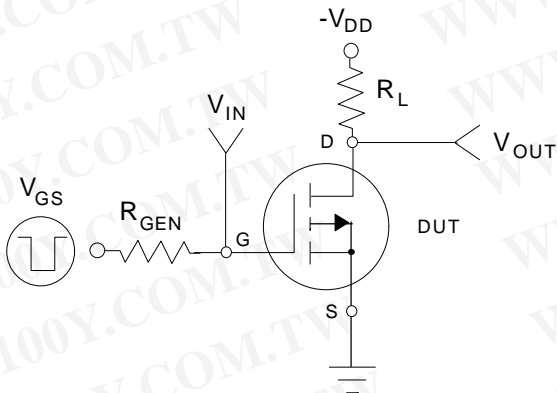


Figure 11. Switching Test Circuit.

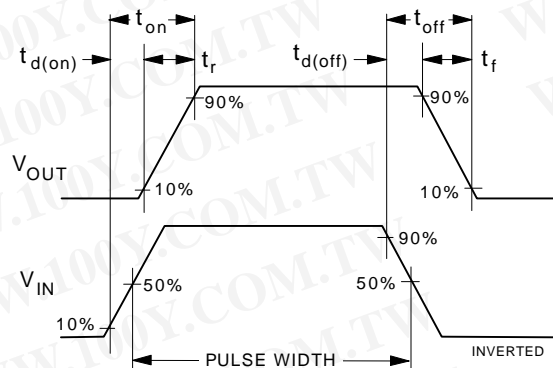


Figure 12. Switching Waveforms.

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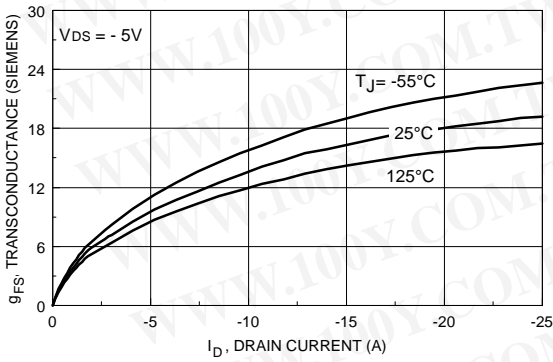


Figure 13. Transconductance Variation with Drain Current and Temperature.

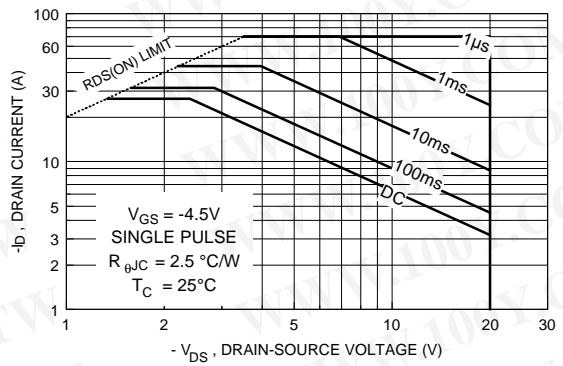


Figure 14. Maximum Safe Operating Area.

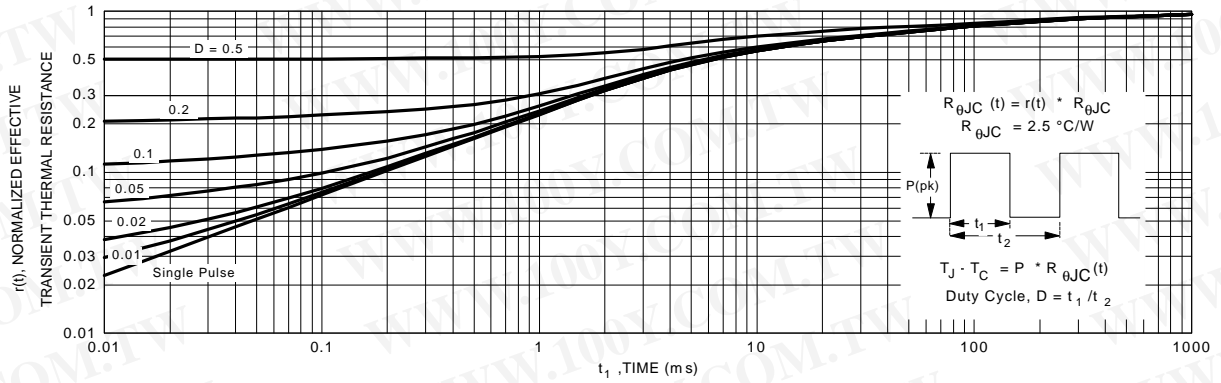


Figure 15. Transient Thermal Response Curve.

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