FAIRCHILD SEMICONDUCTOR TM

August 1998

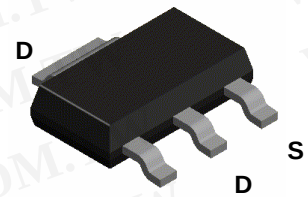
# NDT3055L
# N-Channel Logic Level Enhancement Mode Field Effect Transistor

## General Description

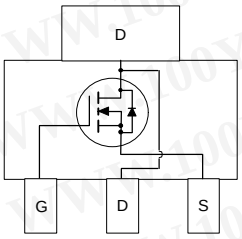
These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance, and withstand high energy pulse in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

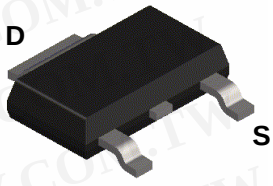
## Features

- 4 A, 60 V. $R_{DS(ON)}$ = 0.100 Ω @ $V_{GS}$ = 10 V,
  $R_{DS(ON)}$ = 0.120 Ω @ $V_{GS}$ = 4.5 V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.

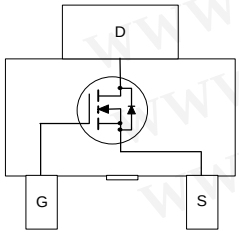




SOT-223




SOT-223* (J23Z)




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | NDT3055L | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 60 | V |
| $V_{GSS}$ | Gate-Source Voltage - Continuous | ±20 | V |
| $I_D$ | Maximum Drain Current - Continuous (Note 1a) | 4 | A |
| | - Pulsed | 25 | |
| $P_D$ | Maximum Power Dissipation (Note 1a) | 3 | W |
| | (Note 1b) | 1.3 | |
| | (Note 1c) | 1.1 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | -65 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 42 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 1) | 12 | °C/W |

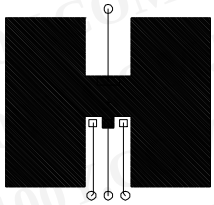
* Order option J23Z for cropped center drain lead.

## Electrical Characteristics ($T_A$ = 25 °C unless otherwise noted )

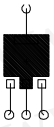
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 60 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | 55 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ =125°C | | | 50 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1 | 1.6 | 2 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | -4 | | mV /°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 4 A | | 0.07 | 0.1 | Ω |
| | | $T_J$ =125°C | | 0.125 | 0.18 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 3.7 A | | 0.103 | 0.12 | |
| $I_{D(ON)}$ | On-State Drain Current | $V_{GS}$ = 5 , $V_{DS}$ = 10 V | 10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 4 A | | 7 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25, $V_{GS}$ = 0 V, f = 1.0 MHz | | 345 | | pF |
| $C_{oss}$ | Output Capacitance | | | 110 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 30 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = 25, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 5 | 20 | ns |
| $t_r$ | Turn - On Rise Time | | | 7.5 | 20 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 20 | 50 | ns |
| $t_f$ | Turn - Off Fall Time | | | 7 | 20 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 40 V, $I_D$ = 4 A, $V_{GS}$ = 10 V | | 13 | 20 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 1.7 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.2 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.5 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.5 A (Note 2) | | 0.8 | 1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 $in^2$ pad of 2oz Cu.



b. 95°C/W when mounted on a 0.066 $in^2$ pad of 2oz Cu.

c. 110°C/W when mounted on a 0.00123 $in^2$ pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%

## Typical Electrical Characteristics

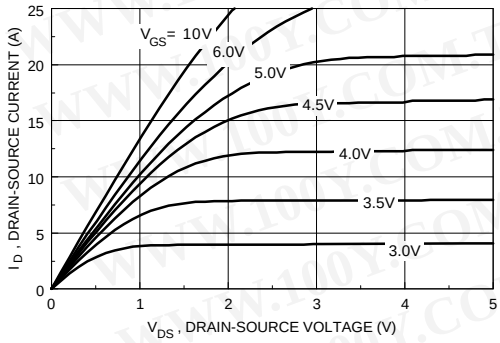



**Figure 1. On-Region Characteristics.**

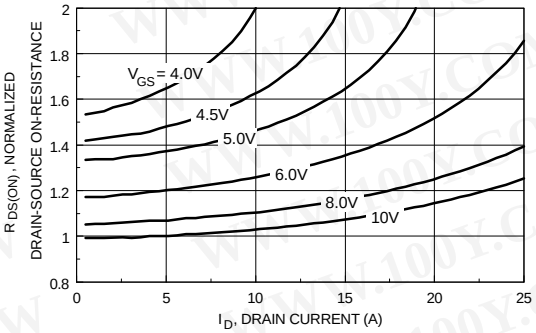



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

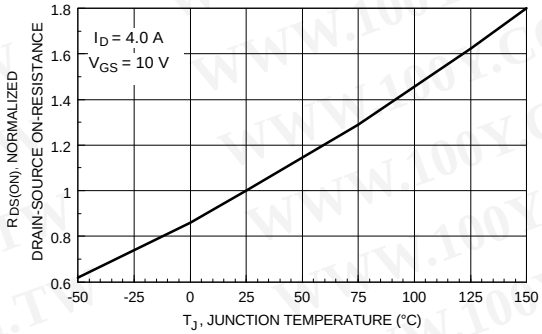



**Figure 3. On-Resistance Variation with Temperature.**

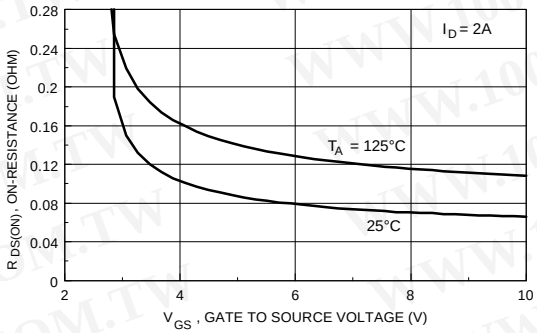



**Figure 4. On-Resistance Variation with Gate-to- Source Voltage.**

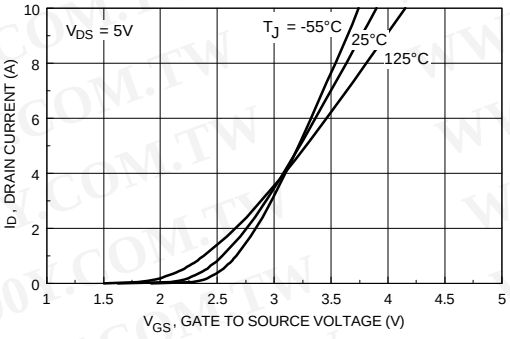



**Figure 5. Transfer Characteristics.**

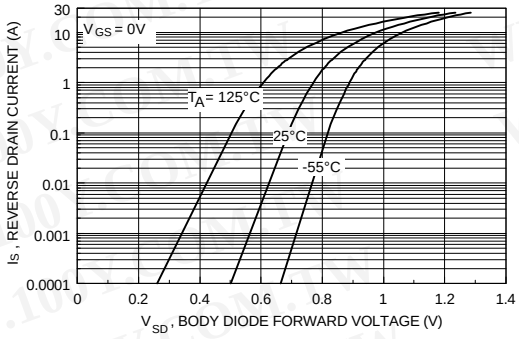



**Figure 6. Body Diode Forward Voltage Variation with Current and Temperature.**

## Typical Electrical Characteristics (continued)

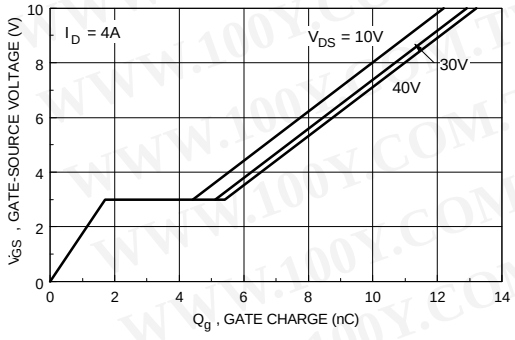



**Figure 7. Gate Charge Characteristics.**

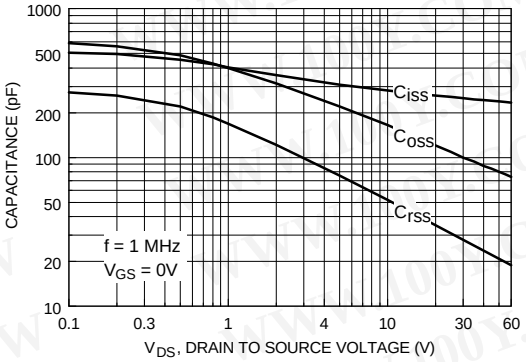



**Figure 8. Capacitance Characteristics.**

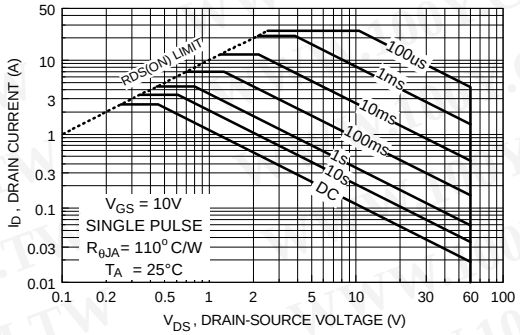



**Figure 9. Maximum Safe Operating Area.**

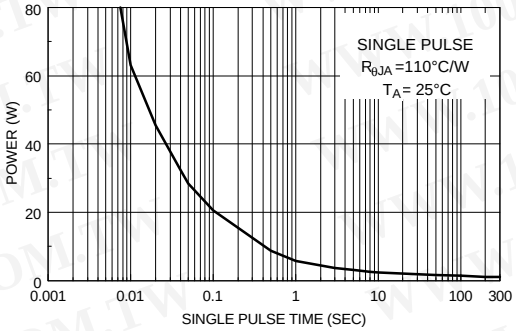



**Figure 10. Single Pulse Maximum Power Dissipation.**

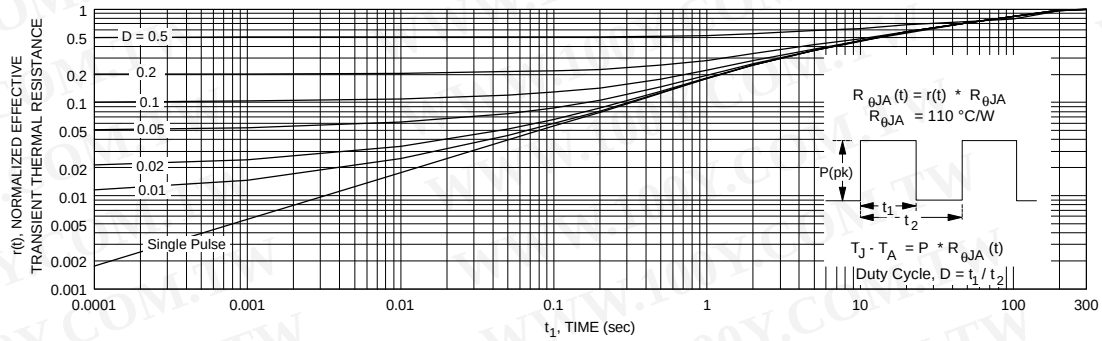



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1c.
Transient thermal response will change depending on the circuit board design.

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