International
IOR Rectifier

REPETITIVE AVALANCHE AND dv/dt RATED
HEXFET TRANSISTORS
THRU-HOLE (TO-204AA/AE)

IRF460
500V, N-CHANNEL

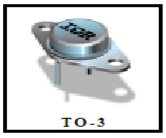
Product Summary

Part Number	BVDSS	RDS(on)	ID
IRF460	500V	0.27Ω	21

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.


TO-3

Features:
- n Repetitive Avalanche Ratings
- n Dynamic dv/dt Rating
- n Hermetically Sealed
- n Simple Drive Requirements
- n Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
ID @ VGS = 0V, TC = 25°C	Continuous Drain Current	21	A
ID @ VGS = 0V, TC = 100°C	Continuous Drain Current	14	
IDM	Pulsed Drain Current ①	84	
PD @ TC = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	1200	mJ
IAR	Avalanche Current ①	21	A
EAR	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.5	V/ns
TJ TSTG	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5(typical)	g

For footnotes refer to the last page

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Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	500	—	—	V	VGS = 0V, ID = 1.0mA
ΔBVDSS/ΔTJ	Temperature Coefficient of Breakdown Voltage	—	0.78	—	V/°C	Reference to 25°C, ID = 1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.27	Ω	VGS = 10V, ID = 14A ④
		—	—	0.31		VGS = 10V, ID =21A ④
VGS(th)	Gate Threshold Voltage	2.0	—	4.0	V	VDS = VGS, ID =250μA
gfs	Forward Transconductance	13	—	—	S (℧)	VDS > 15V, IDS = 14A ④
IDSS	Zero Gate Voltage Drain Current	—	—	25	μA	VDS=400V,VGS=0V
		—	—	250		VDS =400V VGS = 0V, TJ = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	VGS = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100		VGS = -20V
Qg	Total Gate Charge	84	—	190	nC	VGS = 10V, ID=21A VDS = 250V
Qgs	Gate-to-Source Charge	12	—	27		
Qgd	Gate-to-Drain ('Miller') Charge	60	—	135		
td(on)	Turn-On Delay Time	—	—	35	ns	VDD =250V, ID =21A, RG =2.35Ω
tr	Rise Time	—	—	120		
td(off)	Turn-Off Delay Time	—	—	130		
tf	Fall Time	—	—	98		
LS + LD	Total Inductance	—	6.1	—	nH	Measured from drain lead (6mm/0.25in. package) to source lead (6mm/0.25in. fro package)
Ciss	Input Capacitance	—	4300		pF	VGS = 0V, VDS = 25V f = 1.0MHz
Coss	Output Capacitance	—	1000	—		
Crss	Reverse Transfer Capacitance	—	250	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
IS	Continuous Source Current (Body Diode)	—	—	21	A	
ISM	Pulse Source Current (Body Diode) ①	—		84		
VSD	Diode Forward Voltage	—	—	1.8	V	Tj = 25°C, IS = 21A, VGS = 0V ④
trr	Reverse Recovery Time	—	—	580	nS	Tj = 25°C, IF = 21A, di/dt ≤ 100A/μs
QRR	Reverse Recovery Charge	—	—	8.1	μC	VDD ≤ 50V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS +				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
RthJC	Junction to Case	—	—	0.42	°C/W	
RthJA	Junction to Ambient	—	—	30		Typical socket mount

For footnotes refer to the last page

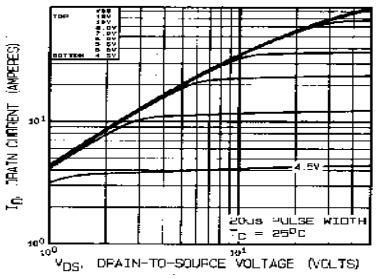


Fig 1. Typical Output Characteristics

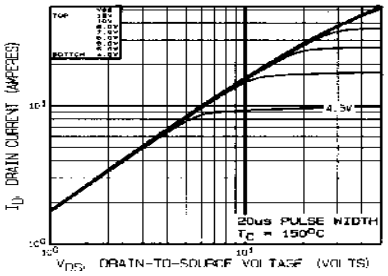


Fig 2. Typical Output Characteristics

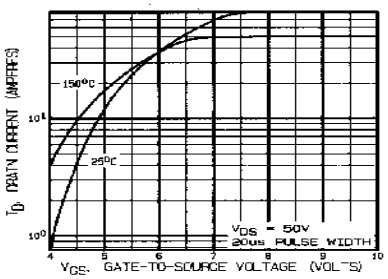


Fig 3. Typical Transfer Characteristics

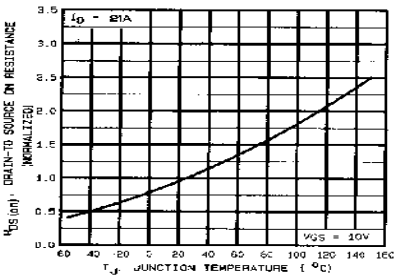


Fig 4. Normalized On-Resistance Vs. Temperature

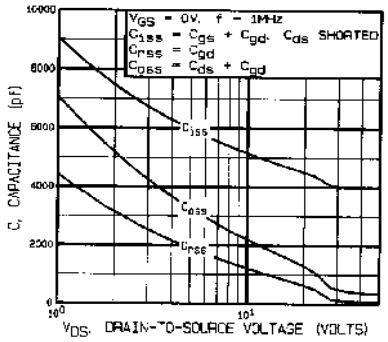


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

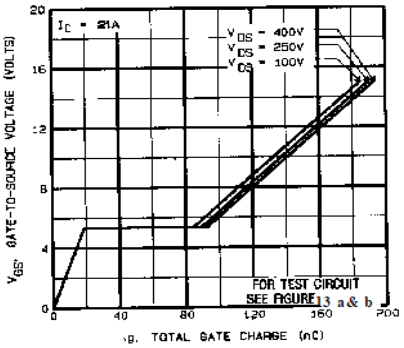


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

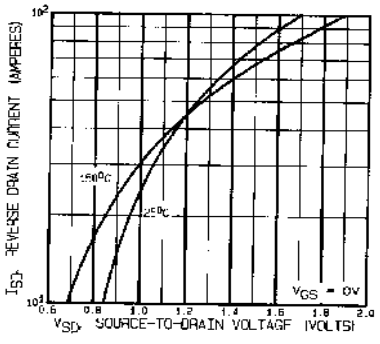


Fig 7. Typical Source-Drain Diode Forward Voltage

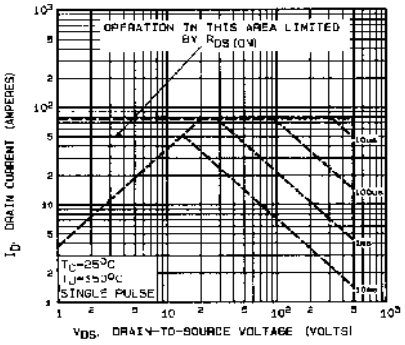


Fig 8. Maximum Safe Operating Area

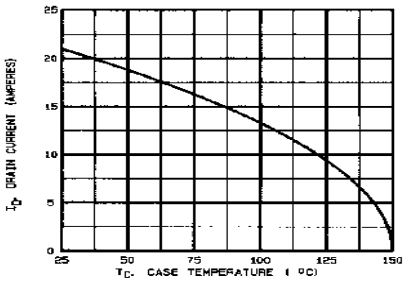


Fig 9. Maximum Drain Current Vs. Case Temperature

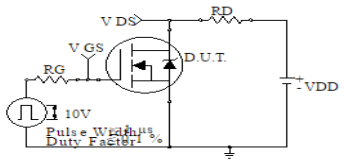


Fig 10a. Switching Time Test Circuit

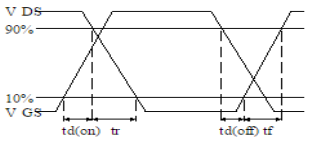


Fig 10b. Switching Time Waveforms

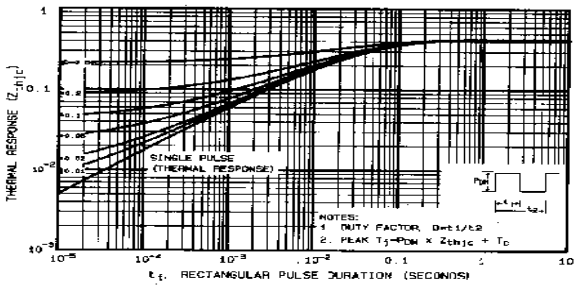


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

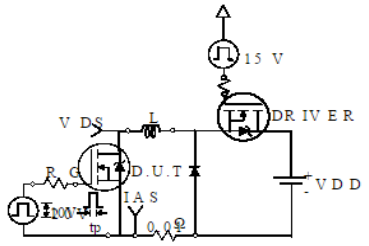


Fig 12a. Unclamped Inductive Test Circuit

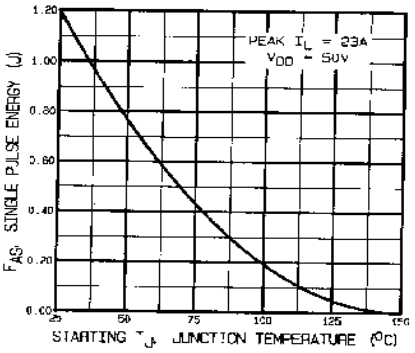


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

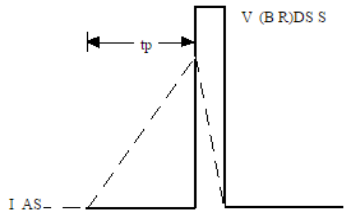


Fig 12b. Unclamped Inductive Waveforms

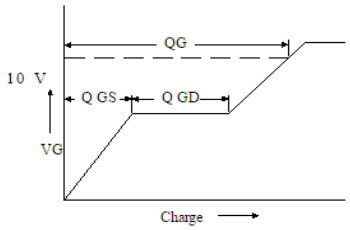


Fig 13a. Basic Gate Charge Waveform

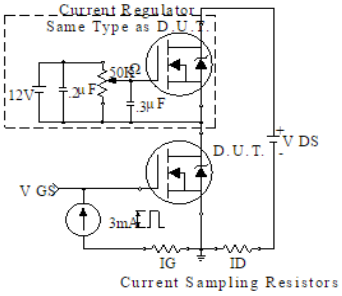
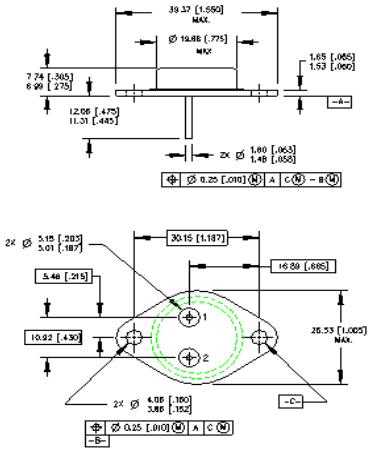


Fig 13b. Gate Charge Test Circuit

Foot Notes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② VDD = 50V, starting TJ = 25°C, Peak IL = 21A,
③ ISD ≤ 21A, di/dt ≤ 160A/μs, VDD ≤ 500V, TJ ≤ 150°C Suggested RG = 2.5Ω
④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

Case Outline and Dimensions —TO-204AE (Modified TO-3)



PIN ASSIGNMENTS

1 – SOURCE
2 – GATE
3 – DRAIN (CASE)

NOTES

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-204AE.