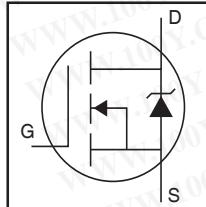


IRFB4115PbF

HEXFET® Power MOSFET

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	150V
R_{DS(on)} typ.	9.3mΩ
	max. 11mΩ
I_D (Silicon Limited)	104A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	104	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	74	
I _{DM}	Pulsed Drain Current ①	420	
P _D @ T _C = 25°C	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	18	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	830	mJ
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Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	0.40	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient ⑦⑧	—	62	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 3.5\text{mA}$ ①
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	9.3	11	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 62\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250	—	$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	—	$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	2.3	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	97	—	—	S	$V_{DS} = 50V, I_D = 62\text{A}$
Q_g	Total Gate Charge	—	77	120	nC	$I_D = 62\text{A}$
Q_{gs}	Gate-to-Source Charge	—	28	—	—	$V_{DS} = 75V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	26	—	—	$V_{GS} = 10V$ ④
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	51	—	—	$I_D = 62\text{A}, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 98V$
t_r	Rise Time	—	73	—	—	$I_D = 62\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	41	—	—	$R_G = 2.2\Omega$
t_f	Fall Time	—	39	—	—	$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	5270	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	490	—	—	$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	105	—	—	$f = 1.0 \text{ MHz, See Fig. 5}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	460	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑥, See Fig. 11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	530	—	—	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	104	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	420	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 62\text{A}, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	86	—	ns	$T_J = 25^\circ\text{C} \quad V_R = 130V,$
		—	110	—	—	$T_J = 125^\circ\text{C} \quad I_F = 62\text{A}$
Q_{rr}	Reverse Recovery Charge	—	300	—	nC	$T_J = 25^\circ\text{C} \quad \text{di/dt} = 100\text{A}/\mu\text{s}$ ④
		—	450	—	—	$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Recommended max EAS limit, starting $T_J = 25^\circ\text{C}$, $L = 0.17\text{mH}, R_G = 25\Omega, I_{AS} = 100\text{A}, V_{GS} = 15V$.
- ③ $I_{SD} \leq 62\text{A}, \text{di/dt} \leq 1040\text{A}/\mu\text{s}, V_{DD} \leq V_{(\text{BR})\text{DSS}}, T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C .

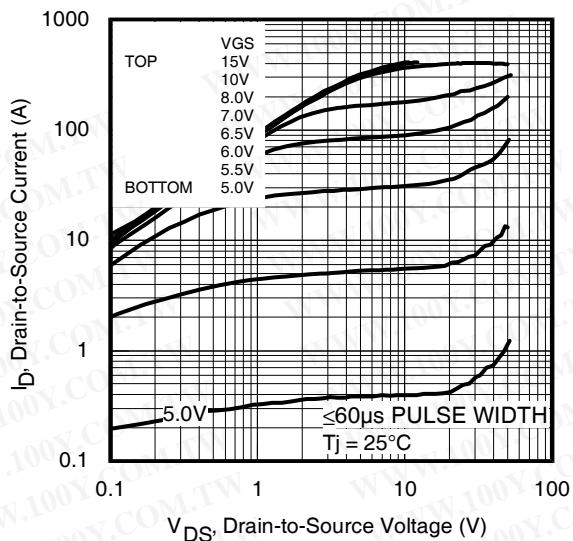


Fig 1. Typical Output Characteristics

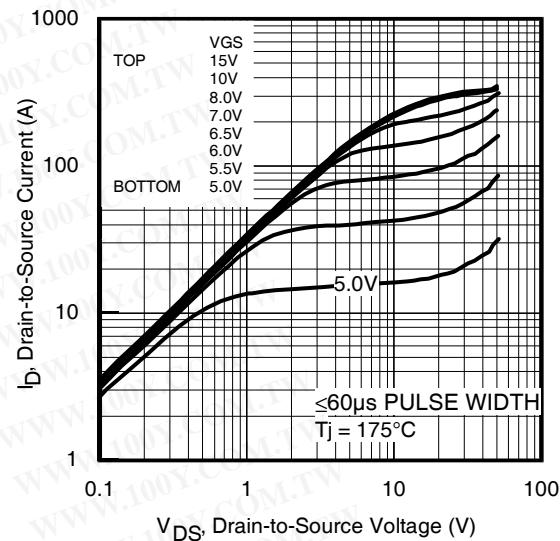


Fig 2. Typical Output Characteristics

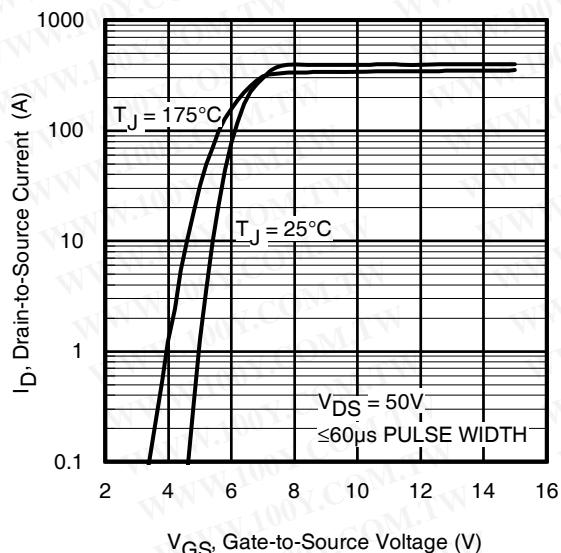


Fig 3. Typical Transfer Characteristics

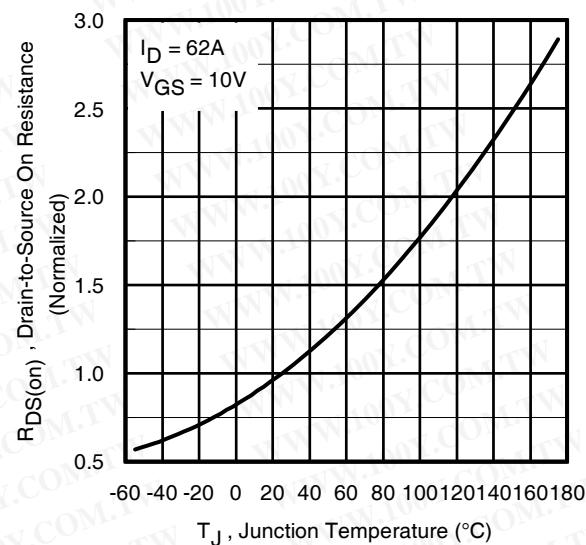


Fig 4. Normalized On-Resistance vs. Temperature

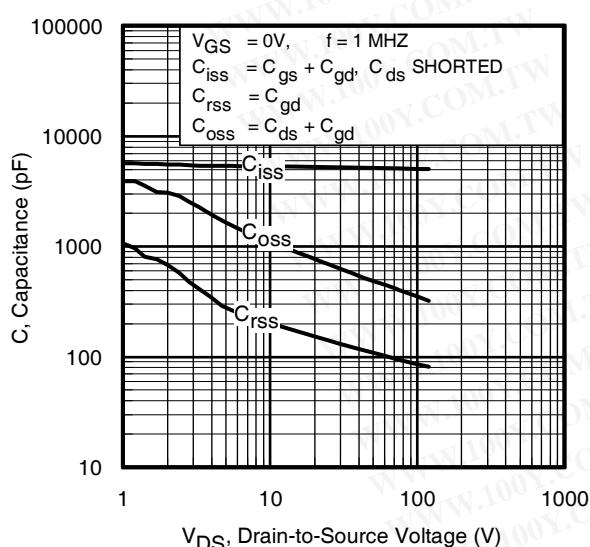


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

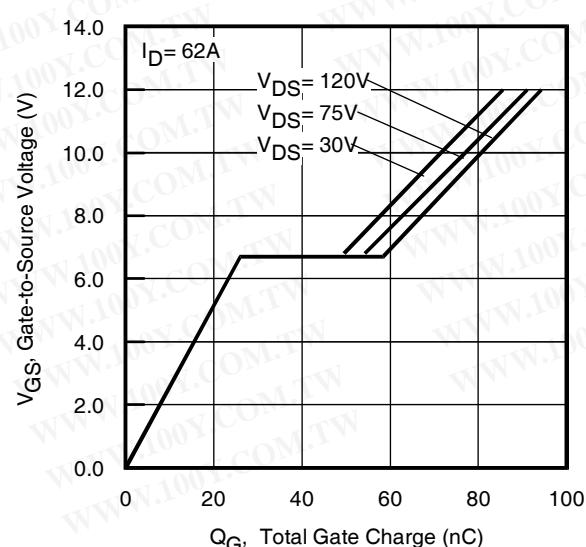


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

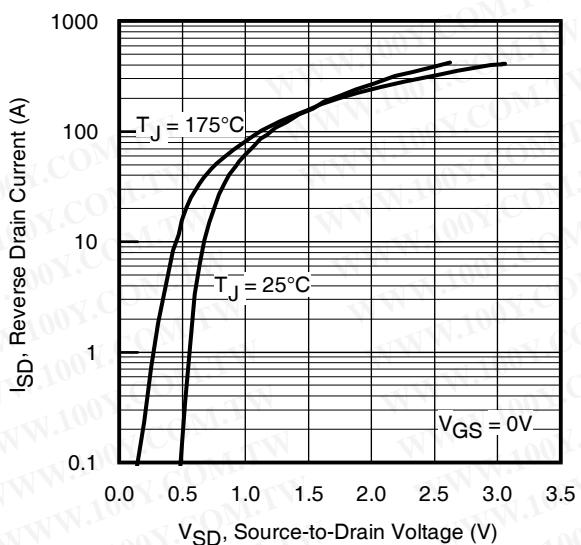


Fig 7. Typical Source-Drain Diode Forward Voltage

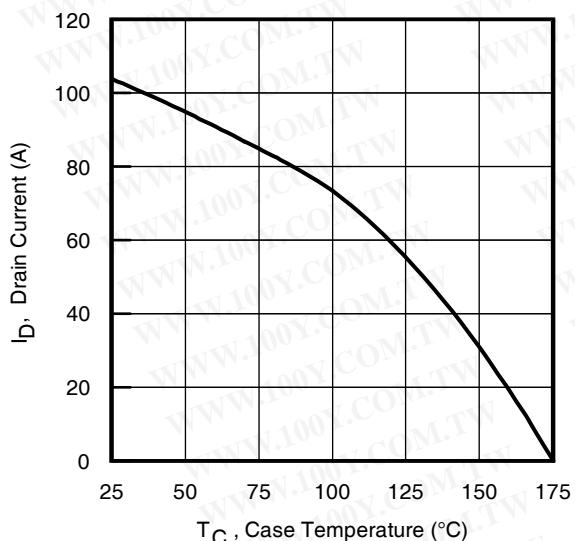


Fig 9. Maximum Drain Current vs. Case Temperature

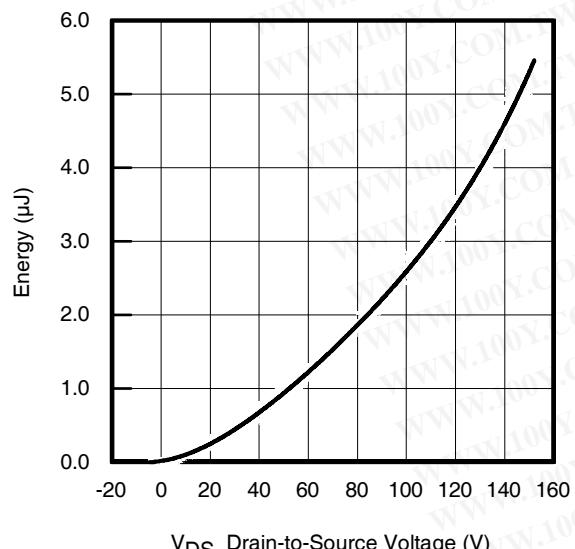


Fig 11. Typical C_{oss} Stored Energy

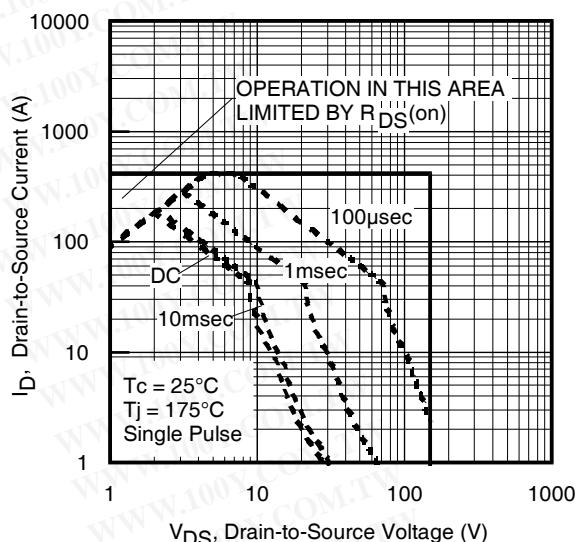


Fig 8. Maximum Safe Operating Area

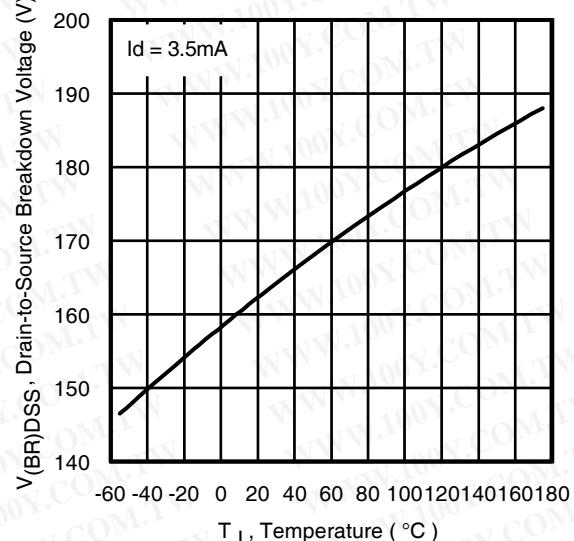


Fig 10. Drain-to-Source Breakdown Voltage

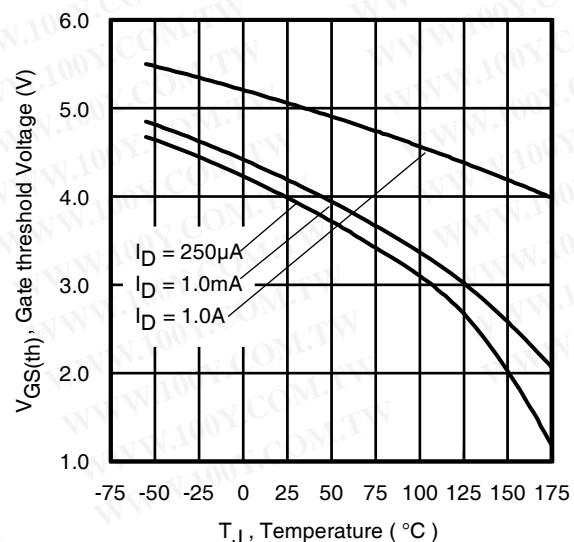


Fig 12. Threshold Voltage vs. Temperature

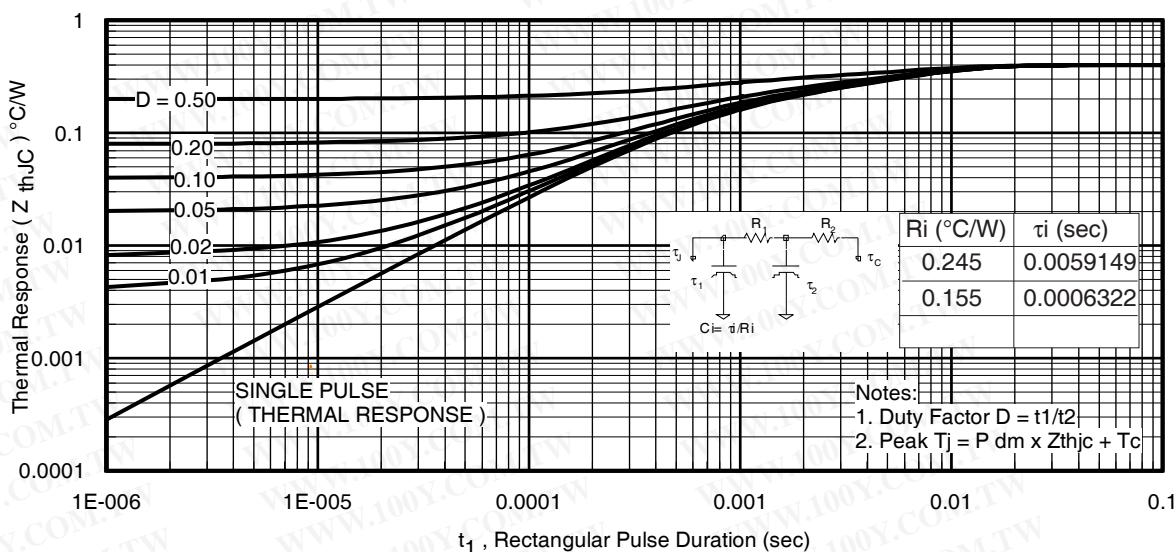


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

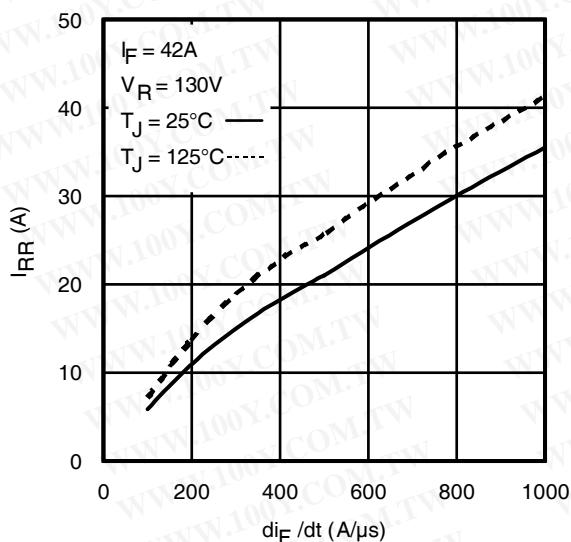


Fig 14. - Typical Recovery Current vs. di_F/dt

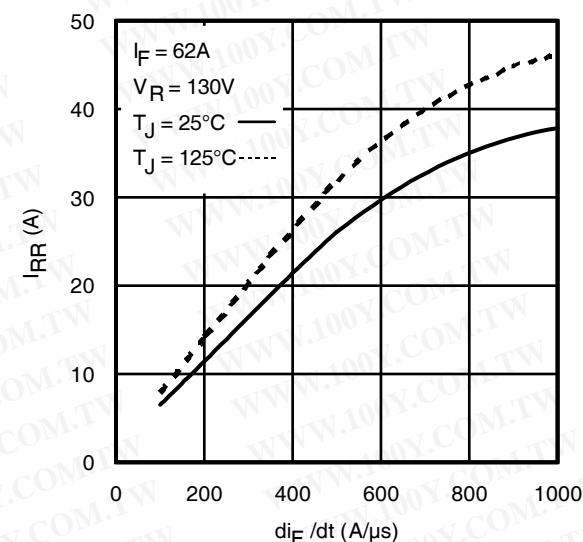


Fig 15. - Typical Recovery Current vs. di_F/dt

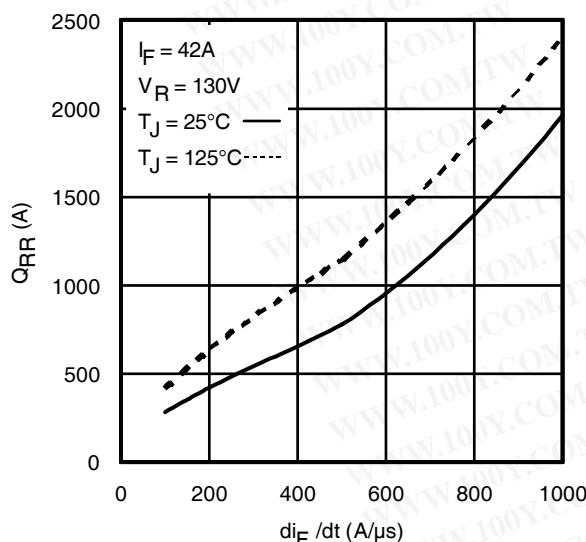


Fig 16. - Typical Stored Charge vs. di_F/dt

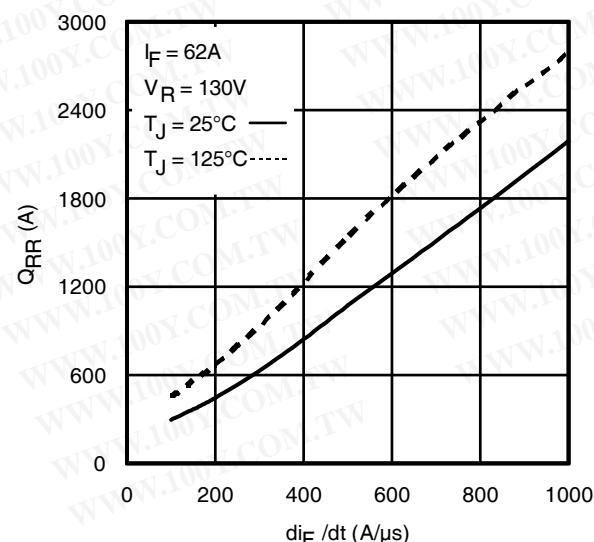


Fig 17. - Typical Stored Charge vs. di_F/dt

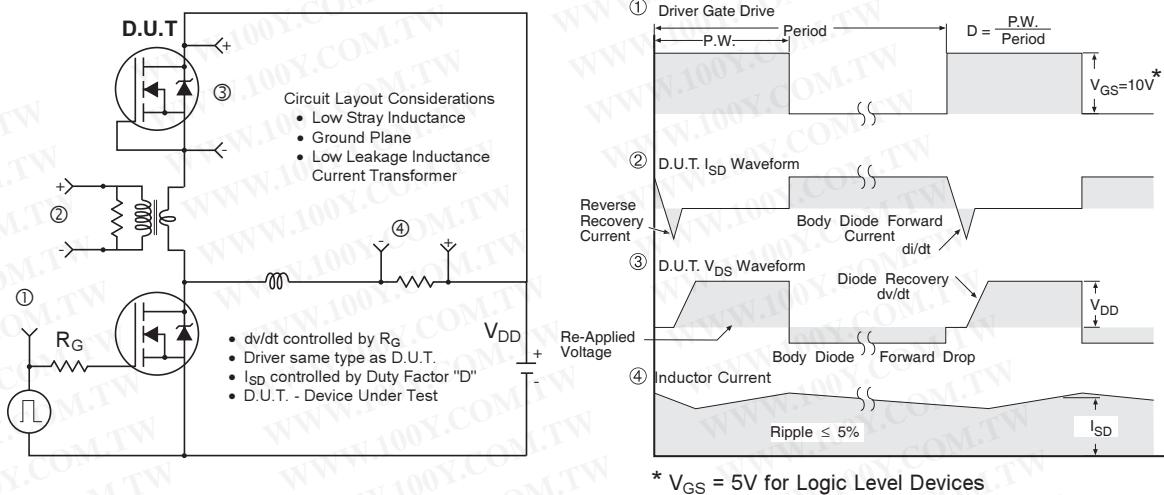


Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

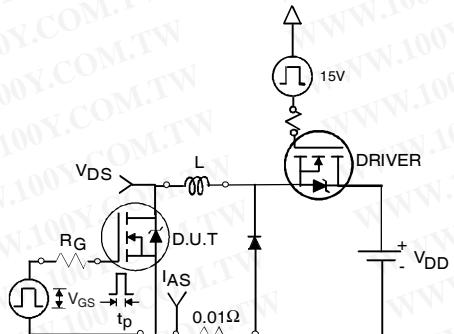


Fig 19a. Unclamped Inductive Test Circuit

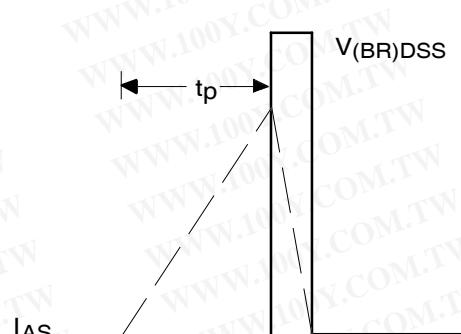


Fig 19b. Unclamped Inductive Waveforms

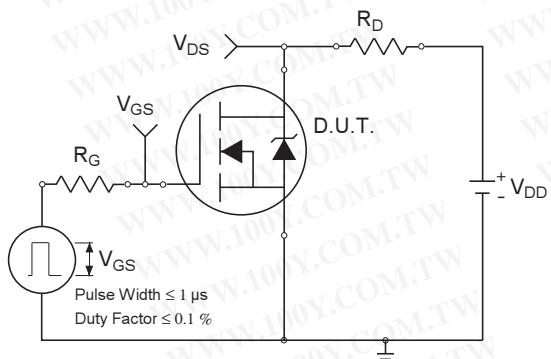


Fig 20a. Switching Time Test Circuit

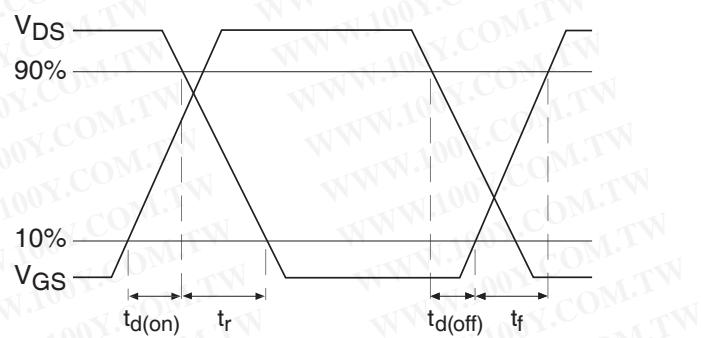


Fig 20b. Switching Time Waveforms

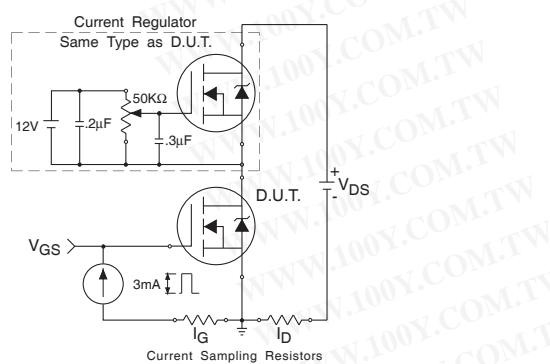


Fig 21a. Gate Charge Test Circuit

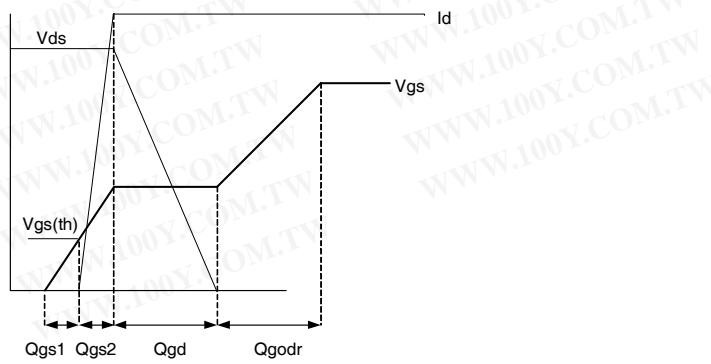
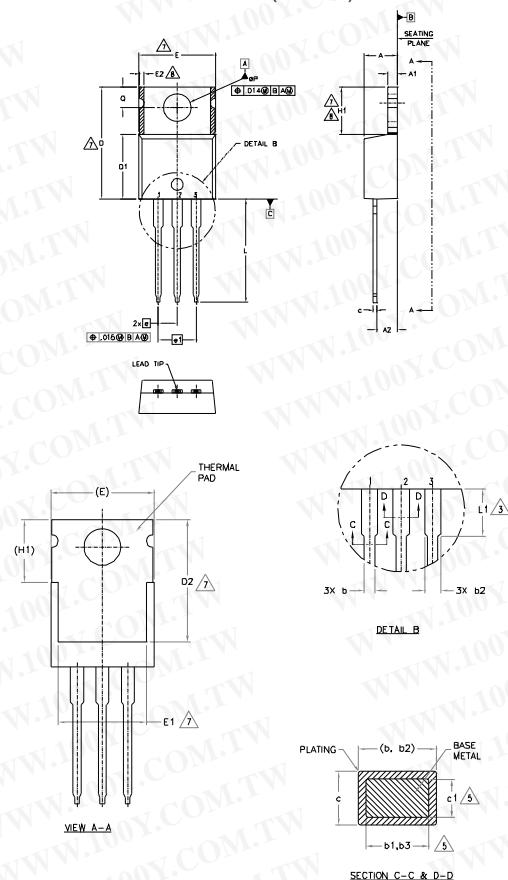


Fig 21b. Gate Charge Waveform

International
Rectifier

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



勝特力材料 886-3-5753170
勝特力电子(上海) 86-21-34970699
勝特力电子(深圳) 86-755-83298787
[Http://www.100y.com.tw](http://www.100y.com.tw)

IRFB4115PbF

NOTES:

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b2 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION = INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, H1, D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SUGGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (mm.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	—	0.76	—	.030	8
e	2.54 BSC	—	.100 BSC	—	
e1	5.08 BSC	—	.200 BSC	—	
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
OP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

LEAD ASSIGNMENTS

HEXIDE

- 1.- GATE
- 2.- CRAIN
- 3.- SOURCE

IGBTs, CAPAC

- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter

DIODES

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

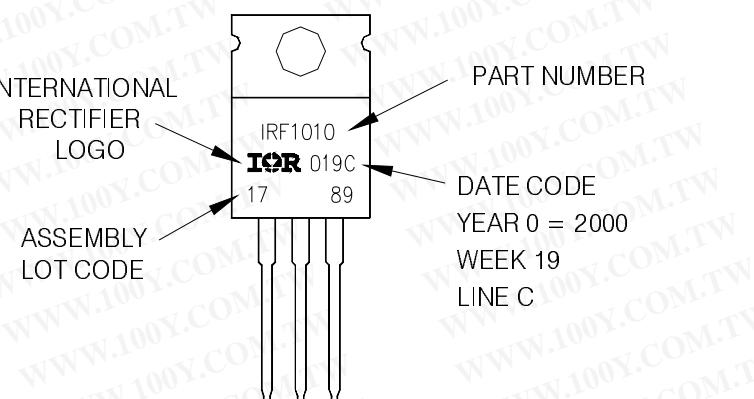
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010

LOT CODE 1789

ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.

Qualification Standards can be found on IR's Web site.

International
Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 07/2011